

Description

Background of the invention

The present invention relates to memory systems and more particularly to an apparatus for simplifying the construction and expansion of such systems.

Prior art

It is well known that modular memory systems permit ready expansion of user memory system or memory space. In order to accommodate such expansion, memory system manufacturers have been required to construct a number of different memory systems having different memory capacities or different size increments of memory. This, in turn, has necessitated the construction of a number of different types of memory units.

One prior art system disclosed in U.S. Patent No. 4,001,790 assigned to the same assignee as named herein employs an arrangement which can utilize the same memory board construction for any one of a number of memory modules which connected, to a memory controller. In the arrangement, one type of memory board (mother board) includes the control logic circuits and another type of memory board (daughter board) contains the memory module.

It is required that the memory module be capable of being plugged into any one of a number of different positions.

In this type of arrangement, it is possible to upgrade and expand the capacity of a memory system utilizing the two types of memory boards mentioned above. The memory increment or memory size in this case corresponds to the capacity of the daughter board.

To reduce the number of different types of memory boards, the prior art system disclosed in U.S. Patent No. 4,296,467 employs a number of memory modules identical to layout and construction. Each board includes rotating chip selection circuits which include a set of switches and an arithmetic unit. By altering the set of switches, the arithmetic unit is conditioned to generate a desired logical row address for enabling chips physically positioned at an initial row location in response to different address values.

While the arrangement reduces the number of different types of memory boards to a minimum, the system is required to include address configuration circuits. Such circuits normally contain a further set of switches and comparison logic circuits for generating signals representative of the addressable memory space or memory increment being provided by a particular board. Also, expansion beyond the maximum capacity of the board still requires utilization of different board types.

U.S. Patent No. 4,303,993, assigned to the same assignee as named herein, discloses a memory subsystem which utilizes memory module boards of identical construction. Each board includes a set of switches which couple to the memory present circuits. By altering the set of switches,

the memory present circuits can be conditioned to generate an output signal indicating the same increment of memory or memory module board is present when a different memory segment is being addressed.

Arrangements of the type described above requires field or installation personnel to set up the set of switches on each memory board to define the size, segment or memory space which is being added or installed in the system. This tends to complicate the assembly or maintenance procedures, particularly when the memory system can be configured to provide a variety of different addressing ranges. The problem is further complicated where memory boards can be constructed from a variety of different types of memory parts and with different densities of memory chips.

In U.S. 4,281,392 which discloses a memory subsystem having a plurality of memory modules each connected to the memory address generating circuits for receiving module address signals, the use of the aforesaid switches is avoided, and automatic memory reconfiguration is obtained, by the provision of a feedback signal from each memory module, representing the memory size of the respective module. The feedback signals of all the modules are used by the control circuits of the memory address generating circuits to reconfigure the address space. The arrangement, however, restricts the memory module to one of two sizes of memory module and will not cater for the use of daughter boards having variable chip populations.

The memory system of the present invention, in common with U.S. 4,281,392, includes one or more memory modules, each identical in construction, and a single address section comprising a plurality of address registers responsive to a first portion of each address code so as to generate addresses of locations within the memory modules and a decoder circuit responsive to a part of the address code comprising at least a second portion thereof in dependence upon said feedback signals, also referred to as "module parameter signals", so as to generate address signals adapted to the address structure of the memory section. It is characterised in that each memory module is a daughter board which plugs into a single mother board containing said address section. Each daughter board is populated with a number of rows of discrete memory chips of preselectable and addressable memory size and has an identification section containing circuits for generating said module parameter signal in form of at least two logic signals indicating characteristics of the board. These logic signals comprise at least one representing the chip population density and at least one representing the size of the said chips. The logic signals of all the daughter boards are combined at the input of the decoder circuit such that it is conditioned by the module parameter signals of all the daughter boards so as to interpret the address signals connected thereto and to bring

about the generation of row select signals in the appropriate sequence in dependence upon the population density and chip size in respect of each daughter board.

In an embodiment described herein the mother board control circuits include a number of decoder circuits which couple to the identification section and to the memory section of each memory module board. The decoder circuits are connected to receive different combinations of address bits of a predetermined multibit address portion of each memory request address used to access the contents of a memory location. In response to signals generated by the identification sections of the installed memory boards, the decoder circuits are selectively enabled to decode those bit combinations of the address portion identified by the sections. This in turn produces the desired sequence of row address select signals which are selectively applied to the memory boards installed in the system for enabling the successive addressing of all of the blocks of locations within the rows of memory chips contained in the board's memory sections.

In the preferred embodiment, the memory module boards can be constructed from either of two types of memory chips and have either of two densities. When the memory section is completely populated, the memory module board has a high density of chips termed "double density". When the memory section is half populated, the memory module board has a lower density termed "normal density". Through the inclusion of an identification section within each module board, the system of the present invention is able to generate automatically the desired sequence of row address select signals for addressing any location within the memory system. This obviates the need to employ additional set up steps in assembling or replacing memory module boards within the system. It also improves system reliability.

Moreover, the blocks or rows of addresses provided by the memory module boards installed in the system are established automatically and without requiring additional switches or logic circuits. Also, normal density memory module boards can be replaced with double density memory module boards and memory module boards constructed with one type of memory part (e.g. 64K RAM chips) can be replaced with memory module boards constructed with another type of memory part (e.g. 256K RAM chip) without requiring changes to the system.

The novel features which are believed to be characteristic of the invention both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying drawings. It is to be expressly understood, however, that each of the drawings are given for the purpose of illustration and description only and are not intended as a definition of the limits of the present invention.

Brief description of the drawings

Figure 1 is a block diagram of a memory system which incorporates the method and apparatus of the present invention.

Figures 2a through 2c shows different embodiments of the decoding apparatus of Figure 1 constructed according to the teachings of the present invention.

Figures 3 through 5 show in greater detail different ones of the blocks of Figure 1.

Figure 6 illustrates the format of a memory address word used in accessing a memory location.

Figure 7 illustrates the different types of memory module boards usable in the system of Figure 1.

Figures 8a through 8d illustrate the construction of the module boards of Figure 1 according to the teachings of the present invention.

Description of the preferred embodiment

Figure 1 shows in block diagram form a preferred embodiment of the memory system of the present invention. As shown, the memory system includes a single computer main/mother board 10 and a pair of pluggable memory module daughter boards 20-1 and 20-2. The daughter boards 20-1 and 20-2 connect to board 10 via 80 pin I/O connectors 22-1 and 22-2.

The board 10 includes all of the memory control logic circuits of the system. These circuits include the address register circuits of block 18, the memory timing and control circuits of block 14, and the chip type and memory density circuits of block 12. The address register circuits of block 18, shown in greater detail in Figure 4, receive for storage the address portion of each memory request or command applied via a system bus. The register circuits apply different ones of these address signals to daughter boards 20-1 and 20-2 and to the circuits of block 12.

The circuits of block 14, shown in greater detail in Figure 3, generate the required sequence of timing strobe signals for performing a memory read or write cycle of operations. As shown, these circuits apply timing signals to the daughter boards 20-1 and 20-2.

The chip type and memory density decoder circuits of block 12, shown in greater detail in Figures 2a through 2c, generate a number of row address decode signals in response to selected combinations of address signals received from the circuits of block 18 as a function of the signals received from daughter boards 20-1 and 20-2. The circuits of block 12 apply selected different ones of these signals to daughter boards 20-1 and 20-2.

Each of the daughter boards 20-1 and 20-2 is identical in design and construction. Accordingly, it will be necessary only to describe one daughter board in detail. The single memory daughter board of the present invention is constructed to be used with different types of memory parts as described herein. To accomplish this, the board is designed (etched) to accommodate the maximum size memory chip. Those areas requiring different

arrangements of signals such as addressing are configured or wired in place on the board.

As seen from Figure 1, each daughter board includes a memory section (i.e., sections 24-1 and 24-2), a chip type and density identification section (i.e., sections 26-1 and 26-2) and an input/output connector (i.e., connectors 22-1 and 22-2). The memory section contains up to four rows of 64K or 256K (1K=1,024) bit dynamic RAM chips.

Each memory section provides a maximum of 256K or 1,024K words of memory storage organized as four blocks of 64K or 256K words which include 16 data bits and six EDAC check bits. The 64K or 256K bit MOS dynamic RAM chips are conventional in design. They may take the form of the 65,536 word or 262,144 word by 1-bit chips, respectively, designated as 2164, manufactured by Intel Corporation, and MSM37256, manufactured by Oki Semiconductor Corporation.

Each board identification section is wired or configured to identify the chip type and density characteristics of its associated memory section. Since the memory boards are identical, the output terminals of both sections are connected in common (i.e., wired ORed).

Single Board Computer 10

The different portions of memory board 10 pertinent to the present invention will now be considered in greater detail. Such portions are shown in Figures 2a through 4.

Chip type and density decoder circuits—12

Figures 2a through 2c show different embodiments of the decoder circuits of the present invention. Referring first to Figure 2a, there is shown a plurality of decoder circuits 12-4 through 12-8 with associated input circuits including NAND gate 12-2, AND gate 12-20 and pull up load resistors 12-40 and 12-42 and output circuits including NAND gates 12-22 through 12-36 arranged as shown. This arrangement of decoder circuits provides the required sequence of decode row address strobe signals for addressing the maximum amount of memory (i.e., 2^{20}).

The one megaword or two megabytes of addressable memory corresponds to four rows of 256K RAM chips. Thus, in this case, only one daughter board will be installed in the system when the daughter board is fully populated (all four rows) with 256K RAM chips.

In addition to constructing a daughter board with different memory parts, the board can be constructed to have one of two densities, normal/standard density or double density. A memory module board which is populated to contain twice the number of chips (i.e., chips in four rows) as a board having normal density (i.e., chips in two rows) is termed "double density". Stated differently, "standard or normal density" refers to a half populated memory module board while "double density" refers to a fully populated daughter board.

The decoder circuits 12-4 of Figure 2a provides

row decode output signals for two normal density daughter boards constructed from 64K RAM memory chips. The decoder circuit 12-6 provides row decode output signals for two double density daughter boards constructed from 64K RAM memory chips. The last decoder circuit 12-8 of Figure 2a provides row decode output signals for two normal density daughter boards constructed from 256K RAM memory chips. Additionally, the same circuit provides row decode output signals for a single double density daughter board constructed from 256K RAM chips.

Each of the decoder circuits 12-4 through 12-8 receive selected ones of the signals MDDBEN100, MDDBEN200, M256PR100 and M256PR200 from the identification sections of daughter boards 20-1 and 20-2 and different combinations of address signals MMAD03010 through MMAD06010 from the address register circuits of block 18.

As shown in Figure 2a, signals MDDBEN100 and MDDBEN200 are wire ORed together. The resulting signal MDDBEN000 identifies the density of both memory boards. That is, when signal MDDBEN000 is at ground potential representative of a binary ZERO, this indicates that each of the memory module daughter boards installed in the system is double density (i.e., has four blocks/rows of memory). Conversely, when signal MDDBEN000 is at a +V voltage potential representative of a binary ONE, this indicates that each of the installed daughter boards is normal density (i.e., has two blocks/rows of memory).

Similarly, signals M256PR100 and M256PR200 are wire ORed together. The resulting signal M256PR000 identifies the type of memory chips contained on both memory module boards. When signal M256PR000 is at ground potential, a binary ZERO, this indicates that each installed daughter board contains 256K RAM chips. When signal M256PR000 is at a +V voltage potential, a binary ONE, this indicates that each of the installed daughter boards contains 64K RAM chips.

As seen from Figure 2a, the NAND gate 12-2 combines both identification signals MDDBEN000 and M256PR000 to generate enabling signal 64KRAM000. When NAND gate 12-2 forces signal 64KRAM000 to a binary ZERO, decoder circuit 12-4 is enabled for decoding a first combination of input address signals MMAD06010 and MMAD05010 applied to its select input terminals. As a function of the coding of these address signals, decoder circuit 12-4 is conditioned to force one of its four output terminals Y0 through Y3 to a binary ZERO.

Each of the four decoder output terminals of circuit 12-4 is connected as an input to a different corresponding one of the NAND gates 12-22 through 12-28. Thus, when decoder circuit 12-4 forces signal 64KDC0000 to a binary ZERO, NAND gate 12-22 is conditioned to force row decode signal DRAST0010 to a binary ONE.

A plurality of enabling input terminals G1 through G2A of decoder circuit 12-6 are connected to receive identification signals MDDBEN000 and M256PR000, as shown. When

signal MDDBEN000 is a binary ZERO and signal M256PR000 is a binary ONE, decoder circuit 12-6 is enabled for decoding a second combination of input address signals MMAD06010 through MMAD04010 applied to its selected input terminals. As a function of the coding of these address signals, decoder circuit 12-6 is conditioned to force one of its eight output terminals Y0 through Y7 to a binary ZERO.

Each of the eight decoder output terminals of circuit 12-6 is connected as an input to a different corresponding one of the NAND gates 12-22 through 12-36, as shown. Thus, when decoder circuit 12-6 forces signal D64DC0000 to a binary ZERO, NAND gate 12-22 is conditioned to force row decode signal DRAST0010 to a binary ONE.

The enabling input terminal of decoder circuit 12-8 is connected to receive signal M256PR000. When this signal is a binary ZERO, decoder circuit 12-8 is enabled for decoding a third combination of input address signals MMAD04010 and MMAD03010 applied to its select input terminals.

Each of the four output terminals of decoder circuit 12-8 is applied as an input to selected ones of the NAND gates 12-22 through 12-32. That is, output terminal Y0 connects to NAND gate 12-22 while output terminal Y1 connects to NAND gate 12-24 similar to the connections of the above discussed decoder circuits. However, output terminal Y2 connects to both NAND gates 12-26 and 12-30 while output terminal Y3 connects to both NAND gates 12-28 and 12-32. This arrangement enables the decoder 12-8 to generate the desired sequence of decode row address strobe signals when two standard density 256K RAM daughter boards or one double density 256K RAM daughter board is installed in the system.

Additionally, each of the NAND gates 12-22 through 12-36 receive as an input, an override decode signal OVRDEC000 from AND gate 12-20. During either a refresh cycle of operation of when the system is initialized, AND gate 12-20 forces signal OVRDEC000 to a binary ZERO. This conditions all of the NAND gates 12-22 and 12-36 to force all of the decode row address strobe signals to binary ONES. Thus, normally, AND gate 12-20 is conditioned to hold signal OVRDEC000 at a binary ONE.

Figures 2b and 2c show arrangements which provide an expanded addressing capability. That is, each provides the required sequence of decode row address strobe signals for addressing a maximum amount of memory which corresponds to two megawords or four megabytes. In this case, two double density memory module daughter boards containing 246K RAM chips can be installed in the system. To provide this additional addressing capability, the number of memory address bits is increased by one bit.

Referring first to Figure 2b, it is seen that a fourth decoder circuit 12-10 together with associated input NAND gates 12-12 and 12-14 have

been added to the embodiment of Figure 2a. The same reference numerals used in Figure 2a are used in Figure 2b and 2c for identifying the same elements.

A plurality of enabling input terminals G1 through G2A of decoder circuit 12-10 are connected to receive identification signals M256PR000 and 256RAM000. Signal M256PR000 is applied directly to enabling terminals G2A and G2B while signal MDDBEN000 is combined with the complement of signal M256PR000 in NAND gate 12-14. The resulting signal 256RAM000 is applied to the enabling terminal G1. Additionally, the same signal is used as the enabling signal for decoder circuit 12-8 as explained herein.

When signal M256PR000 is forced to a binary ZERO and NAND gate 12-14 forces signal 256RAM000 to a binary ONE in response to signal MDDBEN000 being at a binary ZERO, decoder circuit 12-10 is enabled for decoding a fourth combination of input address signals MMAD04010 through MMAD02010 applied to its select input terminals. As a function of the coding of these address signals, decoder circuit 12-10 is conditioned to force one of its eight output terminals Y0 through Y7 to a binary ZERO.

Each of the eight decoder output terminals of circuit 12-10 is connected as an input to a different corresponding one of the NAND gates 12-22 through 12-36 as shown. Thus, when decoder circuit 12-10 forces signal D256DC000 to a binary ZERO, NAND gate 12-22 is conditioned to force row decode signal DRAST0010 to a binary ONE.

With the expanded memory address capability, each of the output terminals of decoder circuit 12-8 now connect to different corresponding one of the NAND gates 12-22 through 12-28. That is, output terminals Y2 and Y3 no longer connect to NAND gates 12-30 and 12-32, respectively. When signal 256RAM000 is forced to a binary ZERO by signal M256PR000 being a binary ZERO and signal MDDBEN000 being a binary ONE, decoder circuit 12-8 is enabled to decode the same third combination of address signals MMAD04010 and MMAD03010 in the same manner as discussed above.

Figure 2c shows another embodiment for providing the expanded address capability. The embodiment reduces the number of decoder circuits by one-half and utilizes an address multiplexer circuit 12-46 for selecting the different desired combinations of address signals applied to the select input terminals of the decoder circuits under the control of chip types identification signal M256PR000. As seen in Figure 2c, the arrangement includes a normal density decoder circuit 12-48 and a double density decoder circuit 12-610. Each of the output terminals of both decoder circuits connects to a different corresponding one of the NAND gates 12-22 through 12-36 as shown.

The enabling input terminal of decoder circuit 12-48 receives the complement or inversion of signal MDDBEN000 via an input NAND gate 12-44. This signal NORBEN000 is also applied to the

G1 input terminal of decoder 12-610. Additionally, the G2A and G2B input terminals of decoder circuit 12-610 receive signal MDDBEN000. The select input terminals of decoder circuit 12-48 and the first two select input terminals of decoder circuit 12-610 are connected to receive signals MSELA1000 and MSELA2000 from multiplexer circuit 12-46. The third select input terminal of decoder circuit 12-610 is connected to also receive signal MSELA4000 from multiplexer circuit 12-46.

The multiplexer circuit 12-46 has its select input terminal connected to receive signal M256PR000 while its first three pairs of input terminals are connected to receive different combinations of address signals MMAD02010 through MMAD06010 as shown. Since its enable input terminal connects to ground, the circuit 12-46 is always enabled for operation.

When normal density signal NORBEN000 is a binary ZERO, decoder signal 12-48 is enabled for decoding a first or second combination of address signals selected as a function of the state of chip type signals M256PR000. That is, when signal M256PR000 is a binary ZERO, the decoder circuit 12-48 decodes address signals MMAD04010 and MMAD03010. Conversely, when signal M256PR000 is a binary ONE, decoder circuit 12-48 decodes address signals MMAD06010 and MMAD05010.

However, when normal density signal NORBEN000 is a binary ONE, in which case signal MMBEN000 is a binary ZERO, decoder circuit 12-610 is enabled for decoding third or fourth combinations of address signals selected as a function of the state of chip type signal M256PR000. That is, when signal M256PR000 is a binary ZERO, decoder circuit 12-610 decodes address signals MMAD02010 through MMAD04010. Conversely, when signal M256PR000 is a binary ONE, decoder circuit 12-610 decodes address signals MMAD04010 through MMAD06010. It will be appreciated that while the arrangement reduces the amount of chips considerably, there is some increase in circuit delay produced by selecting combinations of signals using address multiplexer circuit 12-46.

Memory timing and control circuits — 14

Figure 3 shows in greater detail, a portion of the memory timing and control circuits of block 14. These circuits generate the row address strobe and column address strobe timing signals MRASTS010 and MCASTS010 which are applied to each of the chips of the rows of chips contained within the memory sections of daughter boards 20-1 and 20-2. Additionally, these circuits generate the address register control signals MCASI0000 and MRASI000 which enable the memory address signals of a memory request to be applied to the rows of chips of daughter boards 20-1 and 20-2.

As seen from Figure 3, the circuits of block 14 include a delay line timing generator 14-2, conventional in design, and a plurality of buffer-inverter circuits 14-4 through 14-8, each of which

is connected to receive a different one of a plurality of timing signals DLY020000 through DLY100000 from generator 14-2.

The circuits of block 14 further include a plurality of AND gates 14-10 through 14-14, a pair of NAND gates 14-16 and 14-18 and an inverter circuit 14-20, each of which connect to the output terminal of one of the buffer-inverter circuits 14-4 through 14-8 as shown.

In greater detail, buffer and inverter circuit 14-4 in response to a negative going timing pulse signal DLY02000 conditions AND gate 14-10 to generate row address strobe signal MRASTS010. The signal MRASTS010 is a positive going pulse signal which is generated at the beginning of a memory cycle (i.e., at time 0) in response to signal MCYCLE010, generated by tie breaking circuits, not shown, included within the system. In general, it has a pulse width from 240 to 260 nanoseconds.

The buffer and inverter circuit 14-6 in response to negative going timing pulse signal DLY100000 conditions AND gate 14-12 in the absence of a memory refresh cycle (i.e., when signal RFRNT100 is a binary ONE), to generate column address strobe signal MCASTS010. The signal MCASTS010 is a positive going pulse signal which is generated approximately 65—75 nanoseconds after the start of a memory cycle or after the start of row address strobe signal MRASTS010. It has a pulse width from 210 to 230 nanoseconds.

The buffer and inverter circuit 14-8 in the absence of negative going timing pulse signal DLY060000 conditions inverter circuit 14-20 to force row address time signal RASTME010 to a binary ONE. Signal RASTME010 conditions NAND gate 14-18 to force signal MRASTI0000 to a binary ZERO. This enables the address register circuits of block 18 to apply the row address signals to the rows of RAM chips on daughter boards 20-1 and 20-2. At that time, signals IOGRNT010 and RFRNT100 generated by the memory tie breaking circuits are both binary ONES.

When circuits 14-8 forces signal DLY060110 to a binary ONE in response to negative going timing pulse signal DLY060000, AND gate 14-14 is conditioned to force column address time signal CASTME010 to a binary ONE in the absence of a refresh cycle (i.e., signal RFRNT100 is a binary ONE). At that time, signal RASTME010 is forced to a binary ZERO. Signal CASTME010 conditions NAND gate 14-16 to force signal MCASI0000 to a binary ZERO. This enables the address register circuits of block 18 to apply the column address signals to the rows of RAM chips on daughter boards 20-1 and 20-2. At this time, signal IOGRNT010 is a binary ONE.

Additionally, the circuits of block 14 provide signals IOGRNT000, RFRNT010 and MEACKR710 as further inputs to the circuits of block 18. Signals IOGRNT000 and RFRNT010 are also generated by the memory tie breaking circuits, while memory acknowledgement signal

MEACKR710 is generated by the memory response circuits, not shown. For the purpose of the present invention signals IOGRNT010, RFRGNT100 and MEACKR710 can be assumed to be binary ONES during a memory cycle of operation at which time signal MYCYCLE010 is forced to a binary ONE. For further information about how these signals are generated, reference may be made to the copending application of David A. Boudreau and Edward R. Salas, titled "Priority Resolver with Lowest Priority Level Having Shortest Logic Path", bearing Serial Number 449,703, filed on December 14, 1982 and assigned to the same assignee as named herein.

The last signal shown in Figure 3 is a read/write signal WTMODE100. This signal is derived from the type of memory request received by the system. That is, in the case of a memory request specifying a memory read cycle of operation, signal WTMODE100 is forced low to a binary ZERO. However, when the request specifies a write cycle of operation, signal WTMODE100 is forced high to a binary ONE. For the purpose of the present invention, the circuits generating signal WTMODE100 can be considered conventional in design.

Address register circuits — 18

Figure 4 shows in greater detail, a portion of the address register circuits of block 18. As shown, these circuits include three 8-bit D-type address registers 18-2 through 18-6, a multiplexer circuit 18-8 and a flip-flop circuit 18-9. Each of the registers 18-2 through 18-6 receive different portions of the memory request address from the system bus. More specifically, address register 18-2 receives address bits 15-22 which correspond to the row address part of the memory address which has the format shown in Figure 6. Address register 18-4 receives address bits 7-14 which correspond to the column address part of the memory address. The third address register 18-6 receives address bits 2-6 of the memory address. The memory address bit 2 is only included in the case of a memory system which has an expanded memory addressing capability (i.e., two megawords).

As seen from Figure 4, each of the three registers receive memory acknowledge signal MEACKR710 as an input clocking signal. Address register 18-2 stores the row address signals applied to its input terminals when signal MEACKR710 goes positive. The address contents of register 18-2 are applied to its output terminals when output enable signal MRAST10000 is forced to a binary ZERO by the circuits of block 14.

Similarly, address register 18-4 is conditioned for storing the column address signals applied to its input terminals when signal MEACKR710 goes positive. The register 18-4 applies its address contents to its output terminals when signal MCASI0000 is forced to a binary ZERO by the circuits of block 14. Lastly, address register 18-6 is conditioned on the positive going edge of signal MEACKR710 to store the memory block or seg-

ment address signals. When signal IOGRNT000 is forced to a binary ZERO by circuits 14, register 18-6 applies the stored address signals to its output terminals.

The multiplexer circuit 18-8 and flip-flop 18-9 together provide the value of the ninth address bit for each row and column address used to address daughter boards containing rows of 256K RAM chips. The multiplexer circuit 18-8 when enabled by signal M256PR000 being forced to a binary ZERO generates signal MADD08010 as a function of the states of signals CASTME010 and RFRGNT010. That is, during row address time, in the absence of a refresh cycle, both signals CASTME010 and RFRGNT010 are binary ZEROS. Therefore, multiplexer circuit 18-8 selects signal MMAD06010 applied to data input terminal 0 as the signal to be applied to its output terminal. Thus, address bit 6 is used as the ninth address bit of a 9-bit row address. However, during column address time in the absence of a refresh cycle, signal CASTME010 and signal RFRGNT010 are binary ONE and binary ZERO, respectively. This causes multiplexer circuit 18-8 to select signal MMAD05010 applied to data input terminal 1 as an output. Thus, address bit 5 is used as the ninth address bit of a 9-bit column address.

In the case of a refresh cycle of operation, during row address time, signal CASTME010 is a binary ZERO while signal RFRGNT010 is a binary ONE. This causes multiplexer circuit 18-8 to select signal REFAD8010 applied to data input terminal 2 as an output. Thus, signal REFAD8010 generated by flip-flop 18-9 uses as the ninth bit of the refresh row address signals REFAD0010 through REFAD7010 provided by the memory refresh address circuits, not shown. Flip-flop 18-9 is connected to complement its state upon each occurrence of signal REFAD0010.

For the purpose of the present invention, the refresh address circuits can be considered conventional in design. They operate to provide a desired sequence of address signals for refreshing the rows of RAM chips contained on daughter boards 20-1 and 20-2. During column address time of a refresh cycle of operation, an all ZERO column address is provided. At that time, both signals CASTME010 and RFRGNT010 are binary ZEROS. This causes multiplexer circuit 18-6 to select binary ZERO applied to data terminal 3 as an output. This completes the generation of all ZERO 9-bit column address.

It will be appreciated that the different portions of board 10 can be constructed from standard integrated circuit chips. Examples of these chips are designated within the particular blocks in the different drawings (e.g. Figure 2a — 74S138 — decoder circuit 12-6, Figure 3 — 74S240 — circuits 14-4, etc., and Figure 4 — 74S374 — register 18-2, etc.).

Memory module daughter boards 20-1 and 20-2

Figure 5 shows in greater detail, memory module boards constructed according to the teachings of the present invention. Since each of the

memory module boards is identical in construction as discussed above, only one memory board 20-1 is shown in complete detail.

As seen from Figure 5, each memory module daughter board 20-1 includes I/O connector 22-1 which plugs into the corresponding one of the sockets of board 10. Only those signals which assist in understanding the present invention are shown with specificity.

As discussed above, the board 20-1 also includes a chip type and density identification section 26-1 and a memory section 24-1. As seen from Figure 5, identification section 26-1 includes a pair of jumper connections A00A and A00B used for generating identification signals MddbEN000 and M256PR000. These signals are generated according to the jumper configurations shown in Figure 7.

More specifically, when the daughter board 20-1 is fully populated to provide four blocks or rows of memory chips (i.e., a double density board), the jumper A00A is wired in place. This results in signal MddbEN000 being forced to ground which corresponds to a binary ZERO due to the grounding of one end of the jumper terminal. However, when daughter board 20-1 is half populated to provide two blocks or rows of memory chips (i.e., a single density board), jumper A00A is omitted. Thus, the terminal providing signal MddbEN000 is allowed to float (i.e., no ground). Since the other side of connector 22-1 connects to a voltage +V through pull up register 12-40, signal MddbEN000 assumes a +V value which corresponds to a binary ONE.

It is also seen from Figure 7 that when daughter board 20-1 is populated with 256K RAM chips, jumper A00B is wired into place. In the same manner as discussed above, this results in signal M256PR000 being forced to a binary ZERO. However, when daughter board 20-1 is populated with 64K RAM chips, jumper A00B is omitted. This results in signal M256PR000 being forced to a binary ONE.

The remaining jumper configurations shown in Figure 7 relate to the addressing of 64K and 256K RAM chips. More specifically, they collectively define the value of the ninth address bit relative to refresh operations which corresponds to signal MADE08010. That is, when daughter board 20-1 is populated with 64K RAM chips, jumper A00C is wired in place while jumper A00D is omitted as part of memory section 24-1. This results in signal MADE08110 having a binary ZERO value due to the grounding of one end of jumper A00C. This causes an inverter circuit 246 to force signal MADE08100 high or to a binary ONE. By maintaining the refresh enable terminal (RFE) of each chip high, refresh operations can be externally controlled by the circuits of board 10.

However, when daughter board 20-1 is populated with 256K RAM chips, jumper A00C is omitted while jumper A00D is wired in place. Therefore, signal MADE08010 is allowed to assume the state of signal MADE08010 received from the address register circuits of block 18.

As seen from Figure 5, the main part of memory section 24-1 consists of four rows of memory chips designated as row 0 through row 3. As previously mentioned, the four rows may be constructed from either 64K RAM chips or 256K RAM chips. All of the memory chips of rows 0-3 are connected to receive column address select (CAS) timing signal MCAST0010. This signal is the complement of inversion of signal MCASTS010 received from connector 22-1 via a NAND gate 248.

Additionally, the chips of each row receive a specified one of the decode row address strobe signals DRAST0010 through DRAST5010. As shown, each of the signals DRAST0010 through DRAST5010 is combined with row address select (RAS) timing signal MRASTS010 within a corresponding one of the NAND gates 250 through 258. Each of the resulting signals DRASE0100 through DRASE3100 is applied to RAS input terminals of all of the chips of a specified one of the rows 0-3. That is, signal DRASE0100 is applied to the RAS input terminals of the chips located in row 0, signal DRASE1100 is applied to the RAS input terminals of all of the chips located in row 1, signal DRASE2100 is applied to the RAS input terminals of all of the chips located in row 2 and signal DRASE3100 is applied to the RAS input terminals of all of the chips located in row 3.

All four rows of the memory chips are connected to receive write control signal WTMODE100 from the circuits of block 14. This signal corresponds to signal MREAD0010 and is applied to the WE input terminals of all of the memory chips as shown. The address input terminals 0-7/8 of each RAM chip are connected to receive 8- or 9-bit row and column address portions of each memory address via I/O connector 22-1 from the circuits of block 18. The signals MADD00010 through MADD08010 are inverted via a corresponding number of inverter circuits of blocks 246 and 247 and applied as signals MADE00000-MADE08000 to the chips input address terminals.

Additionally, the 16 data bits and six EDAC check bits of each data word to be written into section memory 24-1 during each memory write cycle of operation are applied via I/O connector 22-1 to the data input (DI) terminals of the memory chips of each row. The 16 data bits and six EDAC check bits of each data word to be read out from memory section 24-1 during each memory read cycle of operation are applied by the data out (DO) terminals of the memory chips of each row to I/O connector 22-1 for transfer to the system bus.

Daughter board 20-1 has the same construction when it is populated for normal density rather than double density as shown in Figure 5. The only difference is that memory section 24-1 will not have chips in rows 2 and 3. Therefore, signals DRAST4010 and DRAST5010 have no effect on memory operations.

The above is true for board 20-2. It will also be noted from Figure 5 that when installed, daughter

board 20-2 is connected to receive signals DRAST2010 through DRAST7010 which are applied to different ones of the NAND gates 250 through 256 of the board. Thus, the identically constructed board responds to the different selected group of decode row strobe signals. When daughter board 20-2 is populated for normal density, memory section 24-2 will not have chips in rows 2 and 3. Therefore, signals DRAST6010 and DRAST7010 have no effect on memory operations.

For the sake of completeness, memory presence signals ONEDTR000 and TWODTR000 are shown. Each of these signals is forced to ground, representative of a binary ZERO, when the daughter board associated therewith is plugged into the system. Both signals are forwarded to the circuits of board 10 where they are used along with the other identification signals to ensure that a valid memory location within the memory system is being addressed. For further information regarding the use of the memory presence signals, reference may be made to the related copending patent application of Daniel A. Boudreau and Edward R. Salas, referenced in the introductory portion of this application.

Description of operation

With reference to Figures 1—7 and the diagrams of Figures 8a through 8d, the operation of the preferred embodiments of the present invention will now be described.

Figure 8a shows the construction of memory module boards 20-1 and 20-2 with normal density using 64K RAM memory chips. As shown, each board includes 64K RAM chips positioned in rows 0 and 1. Both boards provide a memory addressing capability of 256K words. In this arrangement, when board 20-1 is installed, the chips in rows 0 and 1 are connected to receive decode row strobe signals DRAST0010 and DRAST1010, respectively. When board 20-2 is installed, the chips of rows 0 and 1 are connected to receive decode row strobe signals DRAST2010 and DRAST3010, respectively. The identification sections 26-1 and 26-2 are configured to exclude jumpers A00A and A00B according to Figure 7. Hence, the identification sections 26-1 and 26-2 force both signals MDDBEN000 and M256PT000 to binary ONES.

Also, jumper A00C is wired in place while jumper A00D is omitted from memory sections 26-1 and 26-2 of the boards. This permits external control of refresh operations.

By way of example, it is assumed that a series of four memory requests are applied to the memory by the system bus requesting the read out of words from successive segments of blocks of memory. The addresses contained within the requests have the format of Figure 6 and correspond to valid memory locations (i.e., present in the system).

The first such memory request is assumed to have an all ZERO memory address. Different portions of the memory address are loaded into address registers 18-2 through 18-6 of Figure 4 at

the beginning of the memory cycle signalled by signal MEACKR710 going positive in response to the memory system's receipt of a valid request.

Since signal M256PR000 is a binary ONE, multiplexer circuit 18-8 is disabled. Hence, signal MADD08010 which corresponds to the ninth address bit has been effectively omitted.

It can be assumed that signal IOGRNT000 is a binary ZERO at the start of the memory cycle. Hence, address register 18-6 is conditioned to apply memory address bits 2-6 to the decoder circuits of block 12 as signals MMAD02010 through MMAD06010. Referring to Figure 2a, it is seen that since both signals MDDBEN000 and M256PR000 are binary ONES, NAND gate 12-2 is conditioned to force signal 64KRAM000 to a binary ZERO.

Upon being enabled for operation by signal 65KRAM000, decode circuit 12-4 operates to decode address signals MMAD06010 and MMAD05010. Since both these signals are binary ZEROS, decoder circuit 12-4 forces output signal 64KDC0000 to a binary ZERO. This causes NAND gate 12-22 to force row decode signal DRAST0010 to a binary ONE state. As seen from Figures 2a and 5, this signal is applied via I/O connector 22-1 as an input to memory section 24-1.

Also, at the beginning of the memory cycle, the circuits of block 14 operate to force memory row address signal MRASI0000 to a binary ZERO. That is, referring to Figure 3, it is seen that initially, signal DLY060000 is high and goes low during the memory cycle. Therefore, signal DLY060110 is a binary ZERO which causes inverter circuit 14-20 to force signal RASTME010 to a binary ONE. Since both signals IOGRNT010 and RFRGNT100 are binary ONES, NAND gate 14-18 is conditioned by signal RASTME010 to force signal MRASTI0000 to a binary ZERO.

Therefore, at the start of the memory cycle, signal MRASTI0000 causes address register 18-2 of Figure 4 to apply the all ZERO row address bits 15-22 of the memory address to its output terminals as signals MADD00010 through MADD07010. These row address signals are applied via I/O connectors 22-1 and 22-2 to the address input terminals of each of the chips of rows 0 and 1 of both boards 20-1 and 20-2.

Therefore, as soon as the decoder circuits of block 12 force signal DRAST0010 to a binary ZERO, this partially conditions NAND gate 250 of Figure 5. NAND gate 250 is fully conditioned when the circuits of block 14 force row address strobe timing signal MRASTS010 to a binary ONE. As seen from Figure 3, this happens when generator 14-2 generates negative going pulse signal DLY020000.

Upon being fully conditioned, NAND gate 250 of Figure 5 forces signal DRASE0100 to a binary ZERO. This, in turn, causes all of the chips of row 0 of board 20-1 to store the all ZEROS row address signals MADE07010—0010 corresponding to memory address bits 15-22 in row address buffer circuits internal to the chips. This completes the first half of an access cycle.

That is, each 64K memory chip contains a

number of storage arrays organized in a matrix of rows and columns of storage cells (e.g. 256x256, 128x512, etc.). In this embodiment, it will be assumed that the 64K chip matrix is organized to have 256 rows by 256 columns. Accessing one of the 65,536 (64K) storage locations of a chip is accomplished in two steps as discussed herein. In the first step or during a first half of an access cycle, 256 storage locations of a complete row are supplied to 256 columns of sense amplifier circuits located in the chip. In a second step or during a second half of the cycle, one of the 256 columns of sense amplifier circuits is read out to the chip's data out terminal Do. For further information regarding the internal operation of 64K chips, reference may be made to the publication titled "The MOS Memory Data Block" by Texas Instruments Incorporated, Copyright 1980.

The generation of row address strobe signal MRASTS010 is followed 65—75 nanoseconds later by the generation of column address strobe timing signal MCASTS010. As seen from Figure 3, when generator 14-2 forces signal DLY100000 low, this causes in AND gate 14-12 to force signal MCASTS010 to a binary ONE.

However, prior to that, generator 14-2 forces signal DLY060000 low. This causes AND gate 14-14 to force column address strobe timing signal to a binary ONE while at the same time causing inverter circuit 14-20 to force row address timing signal MRASI0000 to a binary ZERO. This results in NAND gate 14-16 forcing memory column address strobe signal MCASI0000 to a binary ZERO while NAND gate 14-18 forces memory row address signal MRASI0000 to a binary ONE.

As seen from Figure 4, signal MCASI0000 when a binary ZERO conditions column address register 18-4 to apply the all ZERO column address bits 7-14 to its output terminals as signals MADD00010 through MADD07010. Since signal M256PR000 is a binary ONE, multiplexer circuit 18-8 remains disabled. Thus, after 75 nanoseconds, the 8-bit row address is replaced by the 8-bit column address. When column address strobe timing signal MCASTS010 is forced to a binary ONE, NAND gate 248 of Figure 5 on each of the boards 20-1 and 20-2 force signal MCAST0010 to a binary ZERO. At that time, the 8-bit all ZEROS column address is latched into the column buffer circuits internal to all of the chips of rows 0—4 of boards 20-1 and 20-2. This completes the second part of the access cycle.

The result that during the read cycle of operation (i.e., when signal MREAD0010 is a binary ONE) bit location 0 of the 64K bit location of each chip is read out to the data out terminal of each of the chips of row 0 of board 20-1. The resulting 22-bit word consisting of 16 data and six EDAC check bits is forwarded to the system bus via I/O connector 22-1.

With the exception of the circuits of block 12, the operation of the circuits of Figure 1 for the most part can be considered the same for processing the remaining memory requests. Therefore, such discussions will be omitted herein. It is

assumed that the remaining memory requests in the series of requests are coded to have all ZERO addresses with the possible exception of address bits 5 and 6. In the next memory request, it is assumed that address bits 6 and 5 have the value "01".

As seen from Figure 2a, decoder circuit 12-4, in response to the "01" values of signals MMAD06010 and MMAD05010, forces signal 64KDC1000 to a binary ZERO. This causes NAND gate 12-24 to force decode row address strobe signal DRAST1010 to a binary ONE.

As seen from Figure 5, upon the generation of memory row address strobe timing signal MRASTS010 by the circuits of block 14, NAND gate 252 is conditioned by signal DRAST1010 to force signal DRASE1100 to a binary ZERO. This causes all of the chips of row 1 of board 20-1 to store the row address signals MADE07010—0010 in row address buffer circuits internal to the chips. Accordingly, at the end of the access cycle, bit location 0 of each of the chips of row 1 is read out and transferred to the system bus via I/O connector 22-1.

When a further memory request is received in which address bits 6 and 5 have the value "10", decoder circuit 12-4 forces signal 64KDC2000 to a binary ZERO. This causes NAND gate 12-26 to force decode row address strobe signal DRAST2010 to a binary ONE.

As seen from Figure 5, NAND gate 250 within memory section 24-2 of board 20-2 forces decode row address strobe signal DRASE0100 to a binary ZERO when the circuits of block 14 force timing signal MRASTS010 to a binary ONE. This causes all of the chips of row 0 of board 20-2 to store the row address signals MADE07010—0010 in internal row address buffer circuits. Accordingly, at the end of the access cycle, the contents of bit location 0 within each of the chips of row 0 are read out and transferred to the system bus.

When a last memory request is received in which address bits 6 and 5 have the value "11", decoder circuit 12-4 forces signal 64KDC3000 to a binary ZERO. This causes NAND gate 12-28 to force decode row address strobe signal DRAST3010 to a binary ONE.

As seen from Figure 5, NAND gate 252 of memory section 24-2 forces decode row address strobe signal DRASE1100 to a binary ZERO in response to signal MRASTS010 being switched to a binary ONE. This causes all of the chips of row 1 of board 20-2 to store row address signals MADE07010—0010 in internal row address buffer circuits. Accordingly, at the end of the access cycle, the contents of bit location 0 within each of the chips of row 1 are read out and transferred to the system bus.

The above shows how a first decoder circuit of Figure 2a operates to address successive rows of chips within normal density boards 20-1 and 20-2 as a function of identification signals M256PR000 and MDDBEN000 generated by identification sections 26-1 and 26-2 in response to the possible different values of a first selected combination of

memory address bits. Addressing proceeds automatically through the different memory segments as indicated by numbers 1 through 4 in Figure 8a, and does not require additional circuits and switches for establishing the segment or block of memory being addressed.

Figure 8b shows the construction of memory module boards 20-1 and 20-2 with double density using 64K RAM chips. As shown, each board includes 64K RAM chips positioned in rows 0 through 3. Both memory boards provide a memory addressing capability of 512K words. When board 20-1 is installed, the chips of rows 0 through 3 are connected to receive decode row strobe signals DRAST0010 through DRAST5010. When board 20-2 is installed, the chips of rows 0 through 3 are connected to receive decode row signals DRAST2010 through DRAST7010. Since the boards are double density with 64K RAM chips, both identification sections 26-1 and 26-2 are configured to include jumper A00A and exclude jumper A00B according to Figure 7. Hence, each of identification sections 26-1 and 26-2 forces signal MDDBEN000 to a binary ZERO and signal M256PR000 to a binary ONE. The remaining jumpers A00C and A00D are wired in the same way as the boards of Figure 8a.

Again, it will be assumed that a series of eight memory requests are applied to the memory requesting the read out of words from successive blocks or rows of memory. Each memory request has an all ZERO address with the possible exception of address bits 4 through 6. In the case of first memory request, it is assumed that bits 4 through 6 have the value "000".

The different portions of the memory request address are stored in registers 18-2 through 18-6 of Figure 4, and applied to the decoder circuits of Figure 2a and the boards 20-1 and 20-2 as explained above. Referring to Figure 2a, it is seen that since signal MDDBEN000 is a binary ZERO and signal M256PR000 is a binary ONE, decoder circuit 12-6 is enabled for decoding address signals MMAD06010 through MMAD04010. Since these signals are binary ZEROS, decoder circuit 12-6 forces output signal D64DC0000 to a binary ZERO. This causes NAND gate 12-22 to force decode row address strobe signal DRAST0010 to a binary ONE state.

In the manner previously described, NAND gate 250 of board 20-1 of Figure 5 forces signal DRASE0100 to a binary ZERO. This enables all of the chips of row 0 to store the eight all ZERO row address signals MADE7010—0010 in the internal row address buffer circuits. The column address signals are then stored in a similar manner. The final result is that the read cycle of operation causes bit location 0 of the 64K bit locations of each chip of row 0 of the first daughter board to be read out and the resulting 22-bit word to be forwarded to the system bus.

Bits 4-6 of the second memory request are assumed to have the value "001". This causes decoder circuit 12-6 to force output signal D64DC1000 to a binary ZERO. This causes NAND

gate 12-24 to force decode row address strobe signal DRAST1010 to a binary ONE state.

In the manner described above, NAND gate 252 of board 20-1 of Figure 5 forces signal DRASE1100 to a binary ZERO. This enables all of the chips of row 1 to store the all ZERO row address signals MADE7000—0000 in the internal row address buffer circuits. Accordingly, the read cycle of operation causes bit location 0 of the 64K bit locations of each chip of row 1 of the first daughter board to be read out and the resulting 22-bit word to be forwarded to the system bus.

Bits 4-6 of the third and fourth memory requests are assumed to have the values "001" and "011", respectively. They cause decoder circuit 12-6 to force in succession output signals D64DC2000 and D64DC3000 to binary ZEROS. This causes NAND gates 12-30 and 12-32 in succession to force row decode signals DRAST4010 and DRAST5010 to binary ONES.

As seen from Figure 5, signals DRAST4010 and DRAST5010 successively condition NAND gates 254 and 256 of the first board 20-1 to force signals DRASE2100 and DRASE3100 to binary ZEROS. Thus, all of the chips in row 2 and then in row 3 are conditioned to store the eight all ZERO row address signals MADE07000—0000 in their internal row address buffer circuits. Accordingly, by these successive read cycles result in words being read out from location 0 of the chips of rows 2 and 3 of the first board 20-1.

Bits 4-6 of the fifth and sixth memory commands are assumed to have the values "100" and "101", respectively. They cause decoder circuit 12-6 to force in succession output signals D64DC4000 and D64DC5000 to binary ZEROS. This causes NAND gates 12-26 and 12-28 in succession to force row decode signals DRAST2010 and DRAST3010 to binary ONES.

As seen from Figure 5, signals DRAST2010 and DRAST3010 successively condition NAND gates 250 and 252 of second board 22-2 to force signals DRASE0100 and DRASE1100 to binary ZEROS. Thus, all of the chips in row 0 and then row 1 are conditioned to store the all ZERO row address signals MADE7000—0000 in their internal row address buffer circuits. The result is that the successive read cycles cause words to be read out from location 0 of the chips of rows 0 and 1 of the second board 20-2.

Bits 4-6 of the seventh and eighth memory commands are assumed to have the values "110" and "111", respectively. They cause decoder circuit 12-6 to force in succession output signals D64DC6000 and D64DC7000 to binary ZEROS. This causes NAND gates 12-34 and 12-36 in succession to force row decode signals DRAST6010 and DRAST7010 to binary ONES.

As seen from Figure 5, signals DRAST6010 and DRAST7010 successively condition NAND gates 254 and 256 of second board 20-2 to force signals DRASE2100 and DRASE3100 to binary ZEROS. Thus, all of the chips in row 2 and then row 3 of the second daughter board 20-2 are conditioned to store the all ZERO row address signals

MADE07000—0000 in their internal buffer circuits. The result is that the successive read cycles cause words to be read out from location 0 of the chips of rows 2 and 3 of board 20-2.

The above sequence of differently coded memory requests shows how a second decoder circuit of Figure 2a operates to address successive rows of chips within double density boards 20-1 and 20-2 as a function of identification signals M256PR000 and MDDBEN000. The rows are selected in response to the possible different values of a second selected combination of memory address bits. As described, addressing proceeds automatically through the different memory segments or rows as indicated by numbers 1 through 8 in Figure 8b.

Figure 8c shows the construction of normal density memory module boards 20-1 and 20-2 with 256K RAM chips. Each chip is organized in a matrix of internal rows and columns (e.g. 512×512, etc.). As shown, each board includes 256K RAM chips positioned in rows 0 and 1. Both memory boards provide a memory addressing capability of one megaword (1024K words). As in the case of Figure 8a, when board 20-1 is installed, the chips of rows 0 and 1, respectively, are connected to receive decode row strobe signals DRAST0010 and DRAST1010. When board 20-2 is installed, the chips of rows 0 and 1 are connected to receive decode row strobe signals DRAST2010 and DRAST3010, respectively.

Since the boards are normal density with 256K RAM chips, both identification sections 26-1 are configured to exclude jumper A00A and to include jumper A00B according to Figure 7. Hence, each of the identification sections 26-1 and 26-2 forces signals MDDBEN000 to a binary ONE and signal M256PR000 to a binary ZERO. Additionally, the remaining jumpers A00C and A00D are wired according to Figure 7. That is, jumper A00C is excluded while jumper A00D is included. This applies as a ninth address bit, signal MADD08010 to the address input terminals of each of the chips of rows 0 and 1 of boards 20-1 and 20-2.

As in the case of Figure 8a, it will be assumed that a series of four memory requests are applied to the memory specifying the read out of words from successive blocks or rows of memory. Each memory request has an all ZERO address with the possible exception of address bits 3 and 4. It is assumed that bits 3 and 4 of the first memory request have the value "00".

As previously explained, the different portions of the memory request address are stored in registers 18-2 through 18-6 of Figures 4 applied to the decoder circuits of Figure 2a and boards 20-1 and 20-2. More specifically, the row and column addresses are sequentially applied to the boards 20-1 and 20-2, as explained above. The ninth bit of each address is provided by multiplexer circuit 18-8. That is, since signal M256PR000 is a binary ZERO, multiplexer circuit 18-8 provides as an output, the input signal selected by the states of signals CASTME010 and RFRNT010. During the

first half of the access cycle (RAS time), since both signals are binary ZEROS, signal MMAD06010 is used as the ninth row address bit of the row address. During the second half of the access cycle (CAS time), the values of the signals are "01". Therefore, signal MMAD05010 is used as the ninth column address bit of the column address.

Referring to Figure 2a, it is seen that since signal M256PR000 is a binary ZERO, decoder circuit 12-6 is enabled for decoding address signals MMAD04010 and MMAD03010. Since both signals are binary ZEROS, decoder circuit 12-8 forces output signals 256DC0000 to a binary ZERO. This causes NAND gate 12-22 to force decode row address signal DRAST0010 to a binary ONE state.

As seen from Figure 5, this causes NAND gate 250 of the first daughter board 20-1 to force signal DRASE0100 to a binary ZERO. This enables all of the chips of row 0 to store the nine all ZERO row address signals MADE08000—0000 in the internal row address buffer circuits. This results in the read cycle of operation causing bit location 0 of the 256K bit locations of each chip of row 0 to be read out and the resulting 22-bit word to be forwarded to the system bus.

Bits 4 and 3 of the second memory request are assumed to have the value "01". This causes decoder circuit 12-8 to force output signal 256DC1000 to a binary ZERO. This causes NAND gate 12-24 to force decode row address strobe signal DRAST1010 to a binary ONE state.

In the above described manner, NAND gate 252 of board 20-1 of Figure 5 forces signal DRASE1100 to a binary ZERO. This enables all of the chips of row 1 to store the nine all ZERO row address signals MADE08000—0000 in the internal row address buffer circuits. Accordingly, the read cycle of operation causes bit location 0 of the 256K bit locations of each chip of row 1 to be read out and transferred.

Bits 4 and 3 of the third and fourth memory requests are assumed to have the values "10" and "11", respectively. They cause decoder circuit 12-8 to force in succession output signals 256DC2000 and 256DC3000 to binary ZEROS. This causes NAND gates 12-26 and 12-28 in succession to force decode row address strobe signals DRAST2010 and DRAST3010 to binary ONES.

As seen from Figure 5, signals DRAST2010 and DRAST3010 successively condition NAND gates 250 and 252 of the second daughter board 20-2 to force signals DRASE0100 and DRASE1100 to binary ZEROS. Thus, all of the chips in row 0 and then in row 1 are conditioned to store the nine all ZERO row address signals MADE08000—0000 in their internal row address buffer circuits. The result is that words are read out from locations 0 of the chips of rows 0 and 1 of the second board 20-2.

The above shows how a third decoder circuit of Figure 2a operates to address successive rows of chips within normal density boards 20-1 and 20-2 constructed with 256K RAM chips as a function of

identification signal M256PR000 in response to possible different values of a third selected combination of memory address bits. Addressing proceeds automatically through the different memory segments or rows as indicated by numbers 1 through 4 in Figure 8c.

The bottom part of Figure 8d shows the construction of double density memory module boards 20-1 with 256K RAM memory chips. As shown, the board 20-1 includes 256K RAM chips positioned in rows 0 through 3. The memory board provides a memory addressing capability of one megaword, the same as Figure 8b. When board 20-1 is installed, the chips of rows 0 through 3 are connected to receive decode row strobe signals DRAST0010 through DRAST5010 as shown in Figure 5.

Since board 20-1 is double density with 256K RAM chips, identification section 26-1 is configured to include jumpers A00A and A00B according to Figure 8. Hence, identification section 26-1 forces signals MDDBEN000 and M256PR000 to binary ZEROS. The remaining jumpers A00C and A00D are wired in the same way as the boards of Figure 8c.

It will be assumed that the same series of four memory requests are applied to memory. Accordingly, decoder circuit 12-8 forces in succession output signals 256DC0000 through 256DC3000 to binary ZEROS. This in turn causes NAND gates 12-22 through 12-28 to force in succession decode row address strobe signals DRAST0010 through DRAST3010 to binary ONES. Since the second board 20-2 is not installed, decode row address strobe signals DRAST2010 and DRAST3010 have no effect on memory operation. Because signals 256DC2000 and 256DC3000 are also applied to NAND gates 12-30 and 12-32, respectively, decode row address strobe signals DRAST4010 and DRAST5010 are also successively forced to binary ONES.

Referring to Figure 5, it is seen that NAND gates 250 through 256 of board 20-1 in succession force signals DRASE0100 through DRASE3100 to binary ZEROS. This enables all of the chips of rows 0-3 to store the nine row address signals MADE08000-0000 in the internal row address buffer circuits. Thus, in successive read cycles of operation, the contents of bit location 0 of the 256K bit locations of each chip of rows 0-3 are read out and the resulting 22-bit-words are forwarded to the system bus.

The above shows how the third decoder circuit of Figure 2a operates to address successive rows of chips within a single density board 20-1 as a function of identification signal M256PR000. The rows are selected in response to the possible different values of the third selected combination of memory address bits. As described, addressing proceeds automatically through the different memory segments or rows as indicated by numbers 1 through 4 in the lower portion of Figure 8d.

Both portions of Figure 8d show the construction of double density memory module boards 20-1 and 20-2 with 256K RAM chips for a memory

system having an expanded addressing capability. As shown, each board includes 256K RAM chips positioned in rows 0-3. Both memory boards provide a memory addressing capability of two megawords (2048 words).

As in the case of Figure 8b, when board 20-1 is installed, the chips of rows 0 through 3 are connected to receive decode row strobe signals DRAST0010 through DRAST5010. When board 20-2 is installed, the chips of rows 0 through 3 are connected to receive decode row signals MRAST2010 through DRAST7010. Both identification sections 26-1 and 26-2 are wired the same as single board 20-1. That is, each of the identification sections 26-1 and 26-2 forces signals MDDBEN000 and M256PR000 to binary ZEROS. The remaining jumpers A00C and A00D are wired in the same way as described above.

Again, it will be assumed that a series of eight memory requests are applied to the memory requesting the read out of words from successive blocks or rows of memory. Each memory request has an all ZERO address with the exception of address bits 2-4. Address bit 2 as discussed above is required for the expanded addressing capability.

The decoding arrangement of either Figure 2b or Figure 2c will be used for providing the expanded addressing capability.

In the case of Figure 2b, identification signals MDDBEN000 and M256PR000, when binary ZEROS, cause NAND gates 12-12 and 12-14 to force signal 256KRAM10 to a binary ONE. This in turn enables decoder circuit 12-10 and at the same time disables decoder circuit 12-8. When enabled, decoder circuit 12-10 decodes address signals MMAD04010 through MMAD02010.

It will be assumed that address signals MMAD04010 through MMAD02010 have the values "000" through "111". Therefore, in response to the series of eight memory requests, decoder circuit 12-10 in succession forces signals D256DC000 through D256DC7000 to binary ZEROS. This causes NAND gates 12-22 through 12-36 to force row decode signals DRAST0010 through DRAST7010 to binary ZEROS.

As seen from Figure 5, NAND gates 250 through 256 of board 20-1 and NAND gates 250 through 256 of board 20-2 are successively conditioned to force signals DRASE0100 through DRASE3100 of board 20-1 and signals DRASE0100 through DRASE3100 of board 20-2 to binary ONES. The result is that all of the chips in rows 0 through 3 of both boards are in turn conditioned to store 9-bit row address signals MADE0800-0000 within their internal row address buffer circuits. Accordingly, at the end of the cycles, the bit location of each of the chips of rows 0 through 3 of both boards are read out and transferred to the system bus. The succession of row addressing proceeds as shown by numbers 1a through 8a in Figure 8d.

The same result is achieved when the same series of eight memory requests are decoded by the decoder circuits of Figure 2c. That is, since signal M256PR000 is a binary ZERO, address bits

2-4 are applied to decoder circuit 12-610 for decoding. The decoder circuit 12-610 is enabled by the binary ZERO state of signal MDDBEN000. Accordingly, decoder circuit 12-610 operates to force in succession signals DDENS0000 through DDENS7000 to binary ZEROS. This in turn causes NAND gates 12-22 through 12-36 to force row decode signals DRAST0010 through DRAST7010 to binary ONES. Accordingly, the succession of row or segment addressing proceeds as shown by numbers 1a through 8a in Figure 8d.

The above shows how the decoder circuits of Figures 2b and 2c operate to address successive rows of chips within double density 256K RAM boards 20-1 and 20-2 as a function of identification signals M256PR000 and MDDBEN000 in response to the different values of a selected combination of memory address bits.

From the explanation it is seen how the apparatus and method of the preferred embodiment of the present invention are able to automatically generate the desired sequences of row decode strobe signals for addressing locations within a function of identification signals provided by the identification sections included in the memory module boards installed in the system. The rows are selected in the sequence defined by the selected address bit combinations of a predetermined address portion of each memory request address.

This enables different density memory module boards constructed with different types of memory parts to be installed within the same memory system without requiring any changes to the system. That is, the addressable or memory address space does not have to be established. Also, no changes are required to be made to the circuits which control memory operations (e.g. timing circuits, address circuits, etc.).

It will be appreciated by those skilled in the art that the present invention may be utilized with other memory parts (e.g. programmable read only memory (PROM) parts, read only memory parts). Also, the invention may be used with different types of memory parts (e.g. 16K RAM chips, 1024K RAM chips, etc.) and with other board densities.

Other changes may be made to the preferred embodiments, such as the type of decoder circuits, the number of address bits, the number of identification signals and memory module boards utilized within the memory system. Also, the identification section may be constructed in alternate ways, as for example, the desired connections may be etched onto each memory module board.

Claims

1. A memory system including a memory section having a plurality of memory modules and an addressing section to which are applied multibit address code portions of memory requests and which is configurable to suit a different memory section address structure, said addressing section

comprising a plurality of address registers responsive to a first portion of each address code so as to generate addresses of locations within the memory modules and a decoder circuit responsive to a part of the address code comprising at least a second portion thereof in dependence upon a module parameter signal so as to generate address signals adapted to the address structure of the memory section, characterised in that said addressing section is contained on a mother board, and said memory modules (24-1, 24-2) are daughter boards each having rows populated with discrete memory chips (240-1, 240-22), each chip being of preselected addressable memory size and each daughter board having an identification circuit (26-1) providing said module parameter signal and that said module parameter signal in respect of each daughter board is constituted by at least two logic signals including a first logic signal (MDDBEN000) representative of the population density, i.e. the number of chip populated rows, of the respective daughter board and a second logic signal (M256PR000) representative of the size of the chips populating the respective daughter board, the said logic signals of the daughter boards being combined at the input of the decoder circuit such that said decoder circuit (Figure 2a, 2b or 2c) is conditioned by the module parameter signals of all the daughter boards so as to interpret the address signals connected thereto and thereby generate row select signals (DRAST0010 to DRAST7010) in the appropriate sequence in dependence upon the population density and chip size in respect of each said daughter board.

2. The device according to Claim 1, characterised in that the multibit address code portion of the memory request corresponds to the number of most significant address bits coded for specifying a maximum number of rows of memory chips which can be included on the daughter boards capable of being built into a memory system, and the daughter boards are identical to one another.

3. The device according to Claim 1, characterised in that the decoder circuit (12) comprises a number of discrete decoder circuits (12-10 to 12-8), each of the said decoder circuits having an enabling input circuit and an input select circuit, where the enabling input circuit of each of the decoder circuits is coupled to receive a different logical combination of said module parameter signals (MDDBEN100—M256PR200), and where the input select circuit of each of the decoder circuits is coupled to receive at least one of a number of different combinations of bits of the said multibit address portion, each decoder circuit, when enabled by a logic signal derived from said parameter signals, being operative to generate decode selection signals for application to the daughter boards (20-1, 20-2) in the predetermined sequence as specified by the coding of the different combinations of address bits applied to the input select circuits of the decoder circuits.

4. The device according to Claim 1, characterised in that the daughter boards (20-1, 20-2) are

2-4 are applied to decoder circuit 12-610 for decoding. The decoder circuit 12-610 is enabled by the binary ZERO state of signal MDDBEN000. Accordingly, decoder circuit 12-610 operates to force in succession signals DDENS0000 through DDENS7000 to binary ZEROS. This in turn causes NAND gates 12-22 through 12-36 to force row decode signals DRAST0010 through DRAST7010 to binary ONES. Accordingly, the succession of row or segment addressing proceeds as shown by numbers 1a through 8a in Figure 8d.

The above shows how the decoder circuits of Figures 2b and 2c operate to address successive rows of chips within double density 256K RAM boards 20-1 and 20-2 as a function of identification signals M256PR000 and MDDBEN000 in response to the different values of a selected combination of memory address bits.

From the explanation it is seen how the apparatus and method of the preferred embodiment of the present invention are able to automatically generate the desired sequences of row decode strobe signals for addressing locations within a function of identification signals provided by the identification sections included in the memory module boards installed in the system. The rows are selected in the sequence defined by the selected address bit combinations of a predetermined address portion of each memory request address.

This enables different density memory module boards constructed with different types of memory parts to be installed within the same memory system without requiring any changes to the system. That is, the addressable or memory address space does not have to be established. Also, no changes are required to be made to the circuits which control memory operations (e.g. timing circuits, address circuits, etc.).

It will be appreciated by those skilled in the art that the present invention may be utilized with other memory parts (e.g. programmable read only memory (PROM) parts, read only memory parts). Also, the invention may be used with different types of memory parts (e.g. 16K RAM chips, 1024K RAM chips, etc.) and with other board densities.

Other changes may be made to the preferred embodiments, such as the type of decoder circuits, the number of address bits, the number of identification signals and memory module boards utilized within the memory system. Also, the identification section may be constructed in alternate ways, as for example, the desired connections may be etched onto each memory module board.

Claims

1. A memory system including a memory section having a plurality of memory modules and an addressing section to which are applied multibit address code portions of memory requests and which is configurable to suit a different memory section address structure, said addressing section

comprising a plurality of address registers responsive to a first portion of each address code so as to generate addresses of locations within the memory modules and a decoder circuit responsive to a part of the address code comprising at least a second portion thereof in dependence upon a module parameter signal so as to generate address signals adapted to the address structure of the memory section, characterised in that said addressing section is contained on a mother board, and said memory modules (24-1, 24-2) are daughter boards each having rows populated with discrete memory chips (240-1, 240-22), each chip being of preselected addressable memory size and each daughter board having an identification circuit (26-1) providing said module parameter signal and that said module parameter signal in respect of each daughter board is constituted by at least two logic signals including a first logic signal (MDDBEN000) representative of the population density, i.e. the number of chip populated rows, of the respective daughter board and a second logic signal (M256PR000) representative of the size of the chips populating the respective daughter board, the said logic signals of the daughter boards being combined at the input of the decoder circuit such that said decoder circuit (Figure 2a, 2b or 2c) is conditioned by the module parameter signals of all the daughter boards so as to interpret the address signals connected thereto and thereby generate row select signals (DRAST0010 to DRAST7010) in the appropriate sequence in dependence upon the population density and chip size in respect of each said daughter board.

2. The device according to Claim 1, characterised in that the multibit address code portion of the memory request corresponds to the number of most significant address bits coded for specifying a maximum number of rows of memory chips which can be included on the daughter boards capable of being built into a memory system, and the daughter boards are identical to one another.

3. The device according to Claim 1, characterised in that the decoder circuit (12) comprises a number of discrete decoder circuits (12-10 to 12-8), each of the said decoder circuits having an enabling input circuit and an input select circuit, where the enabling input circuit of each of the decoder circuits is coupled to receive a different logical combination of said module parameter signals (MDDBEN100—M256PR200), and where the input select circuit of each of the decoder circuits is coupled to receive at least one of a number of different combinations of bits of the said multibit address portion, each decoder circuit, when enabled by a logic signal derived from said parameter signals, being operative to generate decode selection signals for application to the daughter boards (20-1, 20-2) in the predetermined sequence as specified by the coding of the different combinations of address bits applied to the input select circuits of the decoder circuits.

4. The device according to Claim 1, characterised in that the daughter boards (20-1, 20-2) are



constructed to have one of a number of population densities and one of a number of sizes of memory chips (240-1 to 243-22), and the respective identification circuits (26-1, 26-2) include a number of output terminals and a corresponding number of jumper conductors (A00A—A00D) selectively connected to the different output terminals to generate said module parameter signals.

Patentansprüche

1. Speichersystem mit einem Speicherabschnitt, der mehrere Speichermodule und einen Adressierungsabschnitt aufweist, and den mehrere Bit aufweisende Adressierungscodierteile von Speicherabrufbefehlen gegeben werden und der konfiguriert werden kann, um auf eine unterschiedliche Speicherabschnitt-Adressierungsstruktur zu passen, und der darüber hinaus mehrere Adressenregister, die auf einen ersten Teil jedes Adressencodes ansprechen, um Adressen von Stellen innerhalb der Speichermodule zu erzeugen, sowie eine Decodierschaltung aufweist, die auf einen Teil des Adressencodes bestehend aus zumindest hiervon einem zweiten Teil in Abhängigkeit von einem Modulparametersignal anspricht, um der Adressenstruktur des Speicherabschnitts angepaßte Adressensignale zu erzeugen, dadurch gekennzeichnet, daß der Adressierungsabschnitt auf der Mutterplatte enthalten ist und die Speichermodule (24-1, 24-2) Tochterplatten sind, von denen jede mit diskreten Speicherchips (240-1 bis 240-22) belegte Reihen aufweist, von denen ein jeder von vorgewählter adressierbarer Speichergröße ist und jede Tochterplatte eine identifizierungsschaltung (26-1) besitzt, die das Modulparametersignal vorsieht, und daß das Modulparametersignal in Bezug zu jeder Tochterplatte gebildet ist aus zumindest zwei Logiksignalen einschließlich eines ersten Logiksignals (MDDBEN000) des die Belegungs- oder Populationsdichte, d.h. die Anzahl von chipbelegten Reihen der jeweiligen Tochterplatte darstellt, und einschließlich eines zweiten Logiksignals (M256PR000), das die Größe der Chips darstellt, mit der die jeweilige Tochterplatte belegt ist, wobei die Logiksignale der Tochterplatten am Eingang der Decodierschaltung derart verknüpft oder kombiniert werden, daß die Decodierschaltung (Figuren 2a, 2b oder 2c) durch die Modulparametersignale sämtlicher Tochterplatten dahingehend konditioniert wird, die mit ihnen verbundenen Adressensignale zu interpretieren und dadurch in geeigneter Sequenz und in Abhängigkeit von der Belegungsichte und Chipgröße in Bezug zu jeder Tochterplatte Reihenauswahlsignale (DRAST0010 bis DRAST7010) zu erzeugen.

2. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß das Multibit-Adressencodierteil des Speicherabrufbefehls der Anzahl der meistsignifikanten Adressenbits entspricht, die zum Spezifizieren einer maximalen Anzahl von Reihen von Speicherchips codiert sind, die auf die Tochterplatten hineingenommen werden können,

die in einem Speichersystem einsetzbar sowie baugleich zueinander ausgestaltet sind.

3. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß die Decodierschaltung (12) eine Anzahl diskreter Decodierschaltungen (12-10 bis 12-8) aufweist, von denen jede dieser Decodierschaltungen einen befähigenden Eingangsschaltkreis sowie einen Eingangsschaltkreis besitzt, wobei der befähigende Eingangsschaltkreis jeder der Decodierschaltungen gekoppelt ist, eine unterschiedliche logische Kombination der Modulparametersignale

(MDDBEM100—M256PR200) zu empfangen, und der Eingangsauswahlschaltkreis jeder der Decodierschaltungen gekoppelt ist, zumindest eine aus einer Anzahl von unterschiedlichen Bit-Kombinationen des Multibit-Adressenteils zu empfangen, und wobei jede Decodierschaltung, wenn sie durch ein von den Parametersignalen abgeleitetes Logiksignal befähigt ist, wirksam wird, Decodierungsauswahlsignale zu erzeugen, die in vorbestimmter Sequenz, wie diese durch die Codierung der unterschiedlichen Kombinationen der an die Eingangsauswahlschaltkreise der Decodierschaltungen gegebenen Adressenbits vorgeschrieben ist, and die Tochterplatten (20-1, 20-2) gegeben werden.

4. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß die Tochterplatten (20-1, 20-2) so ausgestaltet sind, daß sie eine von mehreren Belegungsichten und eine von mehreren Speicherchipgrößen (240-1 bis 243-22) haben, und daß die jeweiligen Identifizierungsschaltungen (26-1, 26-2) eine Anzahl von Ausgangsanschlüssen sowie eine entsprechende Anzahl von Steckverbindungen (A00A—A00D) besitzen, die selektiv an unterschiedlichen Ausgangsanschlüssen zur Erzeugung der Modulparametersignale angeschlossen sind.

Revendications

1. Système de mémoire comprenant une section de mémoire ayant une multitude de modules de mémoire et une section d'adressage à laquelle sont appliquées des parties de code d'adresse à bits multiples de demandes de mémoire et qui est configurable pour répondre à une structure d'adresses différente de la section de mémoire, la section d'adressage comprenant une multitude de registres d'adresses répondant à une première partie de chaque code d'adresse de manière à produire des adresses d'emplacements à l'intérieur des modules de mémoire et un circuit de décodeur répondant à une partie du code d'adresse comprenant au moins une seconde partie dépendant d'un signal de paramètre de module de manière à produire des signaux d'adresses destinés à la structure d'adresses de la section de mémoire, caractérisé en ce que la section d'adressage est contenue sur une carte-mère, et les modules de mémoire (24-1, 24-2) sont des cartes-filles ayant chacune des rangées peuplées de puces de mémoire discrètes (240-1 à 240-22), chaque puce étant d'une taille de mémoire



adressable présélectionnée et chaque carte-fille comportant un circuit d'identification (26-1) fournissant ledit signal de paramètre de module, et en ce que ledit signal de paramètre de module en ce qui concerne chaque carte-fille est constitué d'au moins deux signaux logiques comportant un premier signal logique (MDDBEN000) représentatif de la densité de la population, c'est-à-dire du nombre des rangées peuplées de puces, de la carte-fille respective et un second signal logique (M256PR000) représentatif de la taille des puces peuplant la carte-fille respective, lesdits signaux logiques des cartes-filles étant combinés à l'entrée du circuit du décodeur de façon que ce circuit du décodeur (figures 2a, 2b ou 2c) soit conditionné par les signaux de paramètre de module de toutes les cartes-filles de façon à interpréter les signaux d'adresses qui leur sont appliqués et produire ainsi des signaux de sélection de rangées (DRAST0010 à DRAST7010) dans la séquence appropriée en fonction de la densité de la population et de la taille des puces en ce qui concerne chaque carte-fille.

2. Dispositif selon la revendication 1, caractérisé en ce que la partie du code d'adresse à bits multiples de la demande de mémoire correspond au nombre des bits des adresses de poids fort codés pour spécifier un nombre maximum de rangées de puces de mémoire qui peuvent être incorporées sur les cartes-filles capables d'être incorporées dans un système de mémoire, et les cartes-filles sont identiques les unes aux autres.

3. Dispositif selon la revendication 1, caractérisé en ce que le circuit (12) du décodeur comprend un certain nombre de circuits de décodeur

discrets (12-10 à 12-8), chacun des circuits de décodeur ayant un circuit d'entrée de validation et un circuit de sélection d'entrée, où le circuit d'entrée de validation de chacun des circuits de décodeur est accouplé de manière à recevoir une combinaison logique différente des signaux de paramètre de module (MDDBEN100—M256PR200), et où le circuit de sélection d'entrée de chacun des circuits de décodeur est accouplé de manière à recevoir au moins une combinaison parmi un certain nombre de combinaisons différentes de bits de la partie d'adresse à bits multiples, chaque circuit de décodeur, lorsqu'il est validé par un signal logique obtenu à partir des signaux de paramètre, pouvant fonctionner pour produire des signaux de sélection de décodage pour application aux cartes-filles (20-1, 20-2) dans la séquence prédéterminée telle qu'elle est spécifiée par le codage des combinaisons différentes des bits d'adresses appliqués aux circuits de sélection d'entrée des circuits de décodeur.

4. Dispositif selon la revendication 1, caractérisé en ce que les cartes-filles (20-1, 20-2) sont construites de façon à avoir une densité parmi un certain nombre de densités de population et une taille parmi un certain nombre de tailles de puces de mémoire (240-1 à 243-22), et les circuits respectifs d'identification (26-1, 26-2) comprennent un certain nombre de bornes de sortie et un nombre correspondant de conducteurs de cavaliers (A00A—A00D) sélectivement connectés aux différentes bornes de sortie pour produire les signaux de paramètre de module.

