ABSTRACT

A METHOD TO FABRICATE A MOSFET USING SELECTRIVE EPITAXIAL GROWTH TO FORM LIGHTLY DOPED SOURCE/DRAIN REGIONS

A new method of fabricating a sub-quarter micron MOSFET device is achieved. A semiconductor substrate is provided. Isolation regions are formed in this substrate. An oxide layer is provided overlying both the substrate and the isolation regions. The oxide layer is patterned and etched exposing two regions of the substrate. A selective epitaxial growth (SEG) is performed with in situ doping covering the two exposed substrate regions formed during the previous step. The doped SEG regions will form the source and drain contact regions of the MOSFET. The oxide layer region between the two doped SEG regions is then patterned and etched away exposing the substrate. This is followed by a gate oxide formation and either a polysilicon or metal gate deposition. Planarization is then performed on the surface to facilitate interconnection later in the process and to form the final gate structure. Thermal energy provided from processing steps or from a rapid thermal anneal (RTA) allows the doping atoms in the SEG regions to diffuse into the substrate thereby forming the active source/drain regions. This method allows precise control of the doping profile in the active source/drain region. An interlevel dielectric is then deposited over the entire surface. Contact holes are then etched in the interlevel dielectric and metalization patterned to allow interconnection to the completed MOSFET device.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)