

WHAT IS CLAIMED IS:

1. A three-dimensional semiconductor device comprising:
main separation structures on a substrate, and extending in a first direction, parallel to a surface of the substrate;
gate electrodes between the main separation structures;
a first secondary separation structure penetrating through the gate electrodes, between the main separation structures, and including a first linear portion and a second linear portion, having end portions opposing each other; and
second secondary separation structures between the first secondary separation structure and the main separation structures, and penetrating through the gate electrodes,
wherein the second secondary separation structures have end portions opposing each other between the second linear portion and the main separation structures, and
wherein each of the second secondary separation structures extends in the first direction.
2. The three-dimensional semiconductor device of Claim 1, wherein each of the second secondary separation structures has a shorter length than a length of the second linear portion, in the first direction.
3. The three-dimensional semiconductor device of Claim 1, wherein each of the main separation structures, the first secondary separation structure, and the second secondary separation structures comprises a conductive pattern and an insulating spacer on a side of the conductive pattern.
4. The three-dimensional semiconductor device of Claim 3, further comprising impurity regions disposed in the substrate below the main separation structures, the first secondary separation structure, and the second secondary separation structures.
5. The three-dimensional semiconductor device of Claim 1:
wherein the substrate comprises a memory cell array region and a connection region,

wherein the gate electrodes are stacked in a direction perpendicular to the surface of the substrate in the memory cell array region, and extend to the connection region, and

wherein the gate electrodes comprise pad regions arranged in a stepwise manner in the connection region.

6. The three-dimensional semiconductor device of Claim 5, further comprising vertical structures on the substrate,

wherein the vertical structures comprise vertical memory cell structures on the memory cell array region and penetrating through the gate electrodes, and vertical dummy structures on the connection region and penetrating through the pad regions; and

wherein a density of disposition of the vertical memory cell structures on the memory cell array region is higher than a density of disposition of the vertical dummy structures disposed on the connection region.

7. The three-dimensional semiconductor device of Claim 6, wherein each of the vertical structures comprises a channel semiconductor layer extending in the direction perpendicular to the surface of the substrate, and a data storage layer between the channel semiconductor layer and the gate electrodes.

8. The three-dimensional semiconductor device of Claim 6, wherein the vertical dummy structures are spaced apart from a boundary between the pad regions when viewed from above.

9. The three-dimensional semiconductor device of Claim 6, wherein a portion of the vertical dummy structures penetrates through a boundary between the pad regions when viewed from above.

10. The three-dimensional semiconductor device of Claim 6, wherein a portion of the vertical dummy structures is between the end portions of the second secondary separation structures opposing each other.

11. A three-dimensional semiconductor device comprising:
main separation structures traversing a memory cell array region and a connection region of a substrate;
gate electrodes including pad regions, sequentially stacked on the memory cell array region and extending to the connection region to be arranged in a stepped manner in the connection region, between the main separation structures;
a first secondary separation structure penetrating through the gate electrodes between the main separation structures, and including a first linear portion extending to the connection region while traversing the memory cell array region, and a second linear portion disposed on the connection region and having an end portion opposing the first linear portion in the connection region; and
second secondary separation structures disposed between the first secondary separation structure and the main separation structures, and penetrating through the gate electrodes, wherein the second secondary separation structures have end portions opposing each other in the connection region, and wherein each of the second secondary separation structures and the main separation structures extends in a first direction, parallel to a surface of the substrate.

12. The three-dimensional semiconductor device of Claim 11, wherein the end portions of the second secondary separation structures, opposing each other, are between the second linear portion of the first secondary separation structure and the main separation structures.

13. The three-dimensional semiconductor device of Claim 11:
wherein the gate electrodes comprise a lower gate electrode, a plurality of intermediate gate electrodes disposed on the lower gate electrode, and a plurality of upper gate electrodes disposed on the plurality of intermediate gate electrodes;
wherein the plurality of upper gate electrodes comprise an upper select gate electrode;
wherein the first linear portion traverses the upper select gate electrode; and

wherein the second linear portion is spaced apart from the upper select gate electrode.

14. The three-dimensional semiconductor device of Claim 13, wherein the second secondary separation structures are spaced apart from the upper select gate electrode.

15. The three-dimensional semiconductor device of Claim 13, further comprising vertical structures disposed on the substrate,

wherein the vertical structures include vertical memory cell structures on the memory cell array region and penetrating through the gate electrodes, and vertical dummy structures disposed on the connection region and penetrating through the pad regions; and

wherein a portion of the vertical dummy structures is between opposing end portions of the first and second linear portions and between opposing end portions of the second secondary separation structures.

16. A three-dimensional semiconductor device comprising:

a substrate including a memory cell array region and a connection region adjacent to the memory cell array region;

gate electrodes stacked in a vertical direction perpendicular to a surface of the substrate in the memory cell array region, and extending to the connection region;

main separation structures penetrating through the gate electrodes, while traversing the memory cell array region and the connection region;

a first secondary separation structure including a first linear portion and a second linear portion, penetrating through the gate electrodes between the main separation structures, and having opposing end portions in the connection region; and

second secondary separation structures located on both sides of the first secondary separation structure, and penetrating through the gate electrodes between the first secondary separation structure and the main separation structures,

wherein the second secondary separation structures have end portions spaced apart from each other while opposing each other, in the connection region; and

wherein each of the second secondary separation structures and the main separation structures extends in a first direction, parallel to a surface of the substrate, wherein each of the

second secondary separation structures has a length shorter than a length of each of the first and second linear portions of the first secondary separation structure.

17. The three-dimensional semiconductor device of Claim 16:

wherein one of the gate electrodes comprises a first gate connection portion between the first and second linear portions, and a second gate connection portion between the second secondary separation structures; and

wherein the second gate connection portions are closer to the main separation structures than the first gate connection portion adjacent to the main separation structures.

18. The three-dimensional semiconductor device of Claim 16:

wherein the gate electrodes comprise a lower gate electrode, a plurality of intermediate gate electrodes on the lower gate electrode, and a plurality of upper gate electrodes on the plurality of intermediate gate electrodes;

wherein the second linear portion of the first secondary separation structure is spaced apart from the plurality of upper gate electrodes; and

wherein the gate electrode including the first and second gate connection portions is one of the plurality of intermediate gate electrodes and the lower gate electrode.

19. The three-dimensional semiconductor device of Claim 17, further comprising vertical structures disposed on the substrate,

wherein the vertical structures include vertical memory cell structures on the memory cell array region and penetrating through the gate electrodes, and vertical dummy structures on the connection region and penetrating through pad regions of the gate electrodes; and

wherein a portion of the vertical dummy structures penetrates through the first and second gate connection portions.

20. The three-dimensional semiconductor device of Claim 16, wherein the gate electrodes comprise pad regions having thicknesses increased to be greater than thicknesses of the gate electrodes, in the connection region.