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A SYSTEM FOR CONTROLLING THE RECORDING OF A COPY PROTECTED VIDEO SIGNAL

The present invention relates to a system for controlling the recording of a copy protected video signal. For example, the invention relates to a copy guard system for protecting a software for a video tape recorder by constructing a circuit for determining the existence and/or non-existence of a copy guard signal within a video tape recorder set, due to an illegal copy of a software for a video tape recorder, in a field of the video signal to be processed by the video tape recorder.

Generally, in a recording system of a video signal of a video tape recorder or video cassette recorder (VTR or VCR), the composite video signal input is applied to a low pass filter, and separated into a luminance signal and a chrominance signal. As the composite video signal is passed by the low pass filter, the amplitude of the input video signal is modulated, for example, the video signal is controlled to have a constant amplitude by way of an automatic gain control (AGC) circuit. Conventionally, in a VHS format VTR or VCR, the AGC circuit comprises a peak AGC and a keyed AGC.

If a signal above a predetermined amplitude is input, the peak type AGC controls the amplitude to a predetermined value. Similarly, if a signal below a predetermined amplitude is applied, the keyed AGC controls the amplitude to a predetermined value. Therefore, the synchronizing signal is a predetermined value regardless of any change of a luminance signal output by the AGC. Commonly, in an AGC including only peak AGC, the luminance signal is lowered, and the screen is dark. Accordingly, there is a disadvantage that a synchronizing signal value is larger than a predetermined value so as to constantly maintain an

entire size of a screen.

The peak-type AGC is the process that a peak of synchronizing signal of television wave is input with a constant value having no relation to the brightness of the screen and thereby the AGC voltage is obtained from the peak. It is based on the peak of the synchronizing signal having no relation to a brightness of screen. And, because the output of the AGC is large, if a large noise pulse is input, the voltage of the noise pulse is utilised to charge a capacitor and the discharge time is lengthened by a resistor. Accordingly, the peak-type AGC has the disadvantage that the large output of the AGC is continued for some time so that the synchronization is unstable and the contrast is lowered.

The keyed AGC was proposed to overcome these disadvantages, and is usually provided as one of the AGC circuits in a TV set. If noise above the level of the synchronization signal is input, the keyed AGC is selected and operates only during the input of the horizontal synchronizing signal so as to easily operate the AGC. Because the keyed AGC is not confused by pulse noise and is stable regardless of the brightness of screen, the keyed AGC is widely employed.

However, in the keyed AGC, the time constant at the AGC detection portion is made large by the VTR having a copy preventive function. Thus, if copy protection, such as a copy guard signal, is existent, the detected signal level and the discharging time are continued for a long time. The AGC detection portion charges the gain characteristics according to the detected level. And, when the detected level is large, that is, in the case when the copy guard signal does exist, the recording loop signal becomes smaller so as not to copy by lessening the size of

the signal output from AGC. Accordingly, the keyed AGC has the disadvantage that the AGC characteristics are bad because of the change of the time constant.

The present invention seeks to solve the above mentioned problems.

According to the present invention there is provided a system for controlling the recording of a copy protected video signal, the system being arranged to receive the video signal and an enable signal for recording means, and having a signal output for coupling the video signal to recording means, wherein the system comprises detector means arranged to detect the presence of copy protection in said video signal and to detect the receipt of a record enable signal, the detector means being arranged to establish the presence of copy protection within a predetermined period following the receipt of a record enable signal, and output means responsive to said detector means and arranged to control the signal applied to said signal output, and wherein said output means is arranged to inhibit the passage of the video signal to said signal output where the presence of copy protection within said predetermined period is established.

In an embodiment, said copy protection comprises one or more copy guard signals imposed during a blanking interval of the video signal, and said detector means is arranged to establish the presence of said copy guard signals in the blanking interval within a predetermined period from the start of said interval.

For example, said detector means may be enabled to detect said copy guard signals for said predetermined period. Thus, said detector means may be arranged to establish the presence of copy guard signals within a

period of 20H from the rising or falling edge of the record enable signal.

Preferably, said system further comprises a gate pulse generator arranged to generate gate pulses in response to an edge of an input head switch pulse and to an edge of horizontal synchronizing pulses of said video signal.

In an embodiment, said detector means comprises a level detector for outputting a signal representative of the presence of copy protection when a clamped input level of said video signal exceeds a predetermined level.

For example, said detector means may further comprise means for generating an output inhibit signal in response to the arrival of said signal representative of the presence of copy protection between the arrival of two spaced gate pulses.

The present invention has the advantage of providing a copy guard system for preventing an illegal copy of a software for a video tape recorder and applying the above system wherever the recording loop of the video tape recorder after an integrating circuit, with both digital and analog signal process technology.

Embodiments of the present invention will hereinafter be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1A illustrates a field of a video signal showing the position of a copy guard signal within the field,

Figure 1B shows part of a video signal illustrating a copy guard signal,

Figure 2 shows a circuit diagram of a copy guard system of the invention,

Figure 3A shows a circuit diagram of a digital signal

process portion of the system of Figure 2, and Figure 3B shows associated waveform diagrams,

Figure 4A shows a circuit diagram of a level detection portion of the system of Figure 2, and Figure 4B is a input waveform diagram of the relationship between a reference voltage and the output waveform of the level detection portion,

Figure 5A shows a circuit diagram of a pulse detection generator of the system of Figure 2, and Figure 5B is a diagram showing the output waveform of the detection pulse generator,

Figure 6A shows a circuit diagram of a signal killer pulse generator of the system of Figure 2 and Figure 6B shows associated waveform diagrams, and

Figure 7 is a circuit diagram showing a signal killer portion of the system of Figure 2.

Figure 1A represents one field of a video signal, G indicating the start of the field and G' indicating the starting point of the next field. The horizontal scanning period is represented as H, whilst the period of vertical blanking is E. During the vertical blanking interval equalizing pulses occur in periods A and C before and after a period B in which one or more vertical synchronising pulses occur. Copy guard signals, for preventing illegal copying of the video signal, are added in period D.

It will be seen from Figure 1A that the horizontal synchronizing pulse signal is added to a period of the vertical synchronizing pulse signal. That is because the horizontal synchronizing pulse signal does not scatter during the period of a vertical synchronizing pulse signal. The equalizing pulse signals of periods A and C preferably comprise a number of equalising pulses each having a width 0.04H (that is, half of a horizontal synchronizing signal) and the period the equalizing pulses is 0.5H, which is

equal to half of a horizontal scanning period. It will be appreciated that if six equalising pulses appear in each period A and C, the period of each equalising pulse signal (6 x 0.5H) will be 3H as shown.

The equalizing pulse signal is effective for interlaced scanning, serving as a horizontal synchronizing signal during a long vertical retrace line interval and stabilizing the horizontal synchronization.

Whilst Figure 1A shows a possible position for a copy guard signal within one field, Figure 1B shows part of the video signal, illustrating a commonly employed copy guard signal. As can be seen, the copy guard signals occupy a period between 3H and 7H and commence 13H from the field start G. The copy guard signal, may comprise between 3 to 7 signals and the system of the invention is arranged to allow no copy when such copy guard signal exists. Figure 1B shows one copy guard signal having a period 1H. In the Figure D1 is a horizontal synchronizing pulse signal and D2 is a peak level signal. D3 indicates a pseudo-synchronizing front porch and D5 indicates a pseudo-synchronizing pulse signal. It will thus be seen that the copy guard signal comprises pairs of pulses added after the synchronizing pulse D1, the pairs of pulses comprising a pseudo-synchronizing pulse as D5 followed by a positive, peak level pulse, as D2. The pairs of pulses are each separated by a respective pseudo-synchronizing front porch D3. It will be seen that the synchronizing pulse D1 and the pseudo-synchronizing pulses D5 have a level of -40 IRE whilst the peak level is given as 100 IRE. It will be appreciated that these levels show the relative levels only. (IRE is an abbreviation for Institute of Radio Engineering.)

Figure 2 shows a system for inhibiting copying of a

video signal including a copy guard signal as described above. The system of Figure 2 may be incorporated, for example, into a video tape recorder (VTR) or video cassette recorder (VCR) or other recording apparatus. In Figure 2, 100 represents an analog signal processing portion, whilst 200 signifies a digital signal processing portion. It will be seen that the video or image signal is input to the portion 100, whilst a head switch pulse signal of the recording apparatus is applied to the digital signal processing portion 200. A horizontal synchronizing signal of the video signal is also applied to the processing portion 200.

The head switch pulse is input to a positive edge detector portion 1 and to a negative edge detector 2 so that both a positive edge and a negative edge of the or each head switch pulse is detected. Input pulses of the horizontal synchronizing signal are input to a counter portion 3 which is arranged to count by 20H from a starting point of each positive edge to a negative edge of the head switch pulse. The positive and negative edge detectors 1 and 2 are arranged to apply pulses to a gate pulse generator 4 controlled by the counter 3 such that a gate pulse is generated.

The input video signal is applied by way of a clamp 5 to a level detector 6 which is controlled by the signal from the gate pulse generator portion 4. The level detector 6 is arranged to detect each level according to the existence and/or non-existence of a copy guard signal. A detection pulse generator 7 receives an output signal from the level detector 6 and produces a rectangular output wave from the detected waveform, the rectangular waveform then being applied to a signal killer pulse generator 8. It will be seen that the signal killer pulse generator 8 also receives the signals output from the positive edge

detector 1 and from the negative edge detector 2. The signal killer pulse generator 8 is arranged to produce an output signal, shown in Figure 6B, to control the signal during the period having a video signal in the field.

A signal killer circuit 9 receives the signal output from the clamp 5 and output from the signal killer pulse generator 8 and is arranged to control the output of the image signal.

Figure 3A shows a circuit diagram of the digital signal processing portion 200 of the system of Figure 2, and Figure 3B is an associated waveform diagram. Figures 3A and 3B illustrate the generation of the reversed gate pulse f described with reference to Figure 2.

Figures 3A and 3B show the application of a head switch pulse signal a to a positive edge and negative edge detector circuit configured by two flip-flops and two NAND gates and arranged to output a pulse c marking the positive edge of the head switch pulse signal a, and a pulse d marking the negative edge thereof. In this respect, it will be appreciated that the existence of the pulse signal a indicates that recording by the recording apparatus is to be enabled. Inverted horizontal synchronizing pulses b are fed by way of an inverter to clock inputs of two further flip-flops configuring the counter 3. It will be appreciated that a signal e is generated by the gate pulse generator 4 by way of the edge-triggered flip-flop configured by further NAND gates which receives both of the signals c and d and pulses derived from the horizontal synchronizing signal. In this respect, it will be seen that e comprises a positive pulse determined by the existence of a positive going pulse c and cut off by a positive going edge of the signal b, whilst e comprises a spaced positive pulse determined by the existence of a

positive going pulse d and cut off by a negative going edge of the signal b. It will also be seen that the output f of the gate pulse generator 4 is the inversion of the signal e. It will also be seen that the period of each pulse of the signal f is 20H. The gate pulse signal f is input to the level detector 6, and the circuit is only operated during the time of 20H (vertical blanking) having the copy guard signal.

Figure 4 shows the circuit and waveform of the level detector 6. If the gate pulse output signal f as shown in Figure 3B is input to the level detector 6, the circuit is operated for 20H started at the rising edge and then the falling edge of the signal a as shown in Figure 3B. In the above operation, in the case where a copy guard signal is present, the copy guard signal is applied to the base of a transistor QA3 from the clamp circuit 5. If the copy guard signal is larger than the voltage on the base of a transistor QA4, the transistor QA3 is turned on, and transistors QA1 and QA2 are also turned on. As a result, current through the transistor QA2 charges a capacitor CA1. The waveform of the charged current in the capacitor CA1 is an integral waveform. In addition, a transistor QA6 and a transistor QA10 are in their off state during the period in which the copy guard signal occurs, that is for the period of 20H from each field starting point. The transistors QA6 and QA10 are saturated at all other times.

Figure 5A shows a circuit of the detection pulse generator 7. As shown in Figure 5A, a voltage source is connected to the emitter of a transistor QB1 and of a transistor QB2 by way of respective resistors RB1 and RB2. The collector of the transistor QB1 is connected to the ground through a constant current source.

The base of the transistor QB2 is coupled to both the

base and the collector of the transistor QB1. The collector of the transistor QB2 is connected to a comparator comprised of transistor QB3 and QB4. A reference voltage (Vref) is applied to the base of the transistor QB3. Also, the collector of the transistor QB3 is connected to the ground by way of a resistor RB3. The collector of the transistor QB4 is also connected to ground.

In operation, as indicated in Figure 5, the comparator comprising the transistors QB3 and QB4 compares the signal waveform output by the level detector 6 with the reference voltage Vref. When the reference voltage is lower than the level of the output signal of the level detector 7, the transistor QB3 is turned on and thus the collector current of the transistor QB2 can flow through resistor RB3. Thus, in the circuit, a voltage is developed across the resistor RB3, which is generally ICB2 x RB3. At all other times, that is, when the output signal of the level detector 7 is equal to or less than the reference voltage, the transistor QB3 is off and there is no current flow in the resistor RB3. Therefore the output waveform has a low state. Further, in the case in which the copy guard signal exists and is input to the base of the transistor QA3 of the level detector 6, the output signal waveform made by the application of the constant reference voltage Vref to the transistor QB3 is a complete rectangular wave as shown in Figure 5B.

Figure 6 shows the circuit and the input and output waveforms of the signal killer pulse generator 8 receiving the output g of the detection pulse generator 7. It will be seen that the signal g is inverted by way of an inverter INb1 and is then input to a clock terminal of a flip-flop. In addition, the positive and negative edge signals c and d are applied to the reset terminal of the RS-flip-flip by

way of a NAND gate. Thus, a killer signal h is output from the Q terminal of the flip-flop at the falling edge of the signal g as shown in Figure 6B.

Figure 7 shows a circuit diagram of the signal killer circuit 9 of the system shown in Figure 2. As can be seen, the circuit 9 comprises transistors QC1 and QC2 whose collectors are each connected to the voltage source line Vcc. The emitter of the transistor QC1 is connected to ground through a DC current source IC1 and also to the base of the transistor QC2. The output signal of the clamp circuit 5 is input to the base of the transistor QC1. The collector of a further transistor QC3 is connected to the emitter of the transistor QC1 and to the base of the transistor QC2 by way of a resistor RC2, and the base of the transistor QC3 receives the killer signal h by way of a resistor RC1. The emitter of the transistor QC3 is connected to ground. As a result, whether or not the image signal is output is determined in accordance with the killer signal h applied to the resistor RC1. Thus, if a copy guard signal exists the positive killer signal h is applied to the base of the transistor QC3. This turns on the transistors QC3 and QC2 to connect their collector current paths, and the output, to ground. It also turns off the transistor QC1 whereby connection of the image signal to the output is prevented. Thus, the image signal is effectively removed by the signal killer circuit portion 9 shown in Figure 2. The image signal is not generated and only a constant DC output appears on the output.

The system described above may be incorporated into a VTR, VCR or other recording apparatus and the improved copy guard system having an AGC function is adapted. If a copy guard signal does exist, recording of the signal is prevented by the copy guard signal, and so the production of an illegal copy is prevented.

Although a currently preferred embodiment of the invention has been shown and described, it will be understood that variations and modifications may be made therein without departing from the scope of the appended claims.

CLAIMS

1. A system for controlling the recording of a copy protected video signal, the system being arranged to receive the video signal and an enable signal for recording means, and having a signal output for coupling the video signal to recording means, wherein the system comprises detector means arranged to detect the presence of copy protection in said video signal and to detect the receipt of a record enable signal, the detector means being arranged to establish the presence of copy protection within a predetermined period following the receipt of a record enable signal, and output means responsive to said detector means and arranged to control the signal applied to said signal output, and wherein said output means is arranged to inhibit the passage of the video signal to said signal output where the presence of copy protection within said predetermined period is established.

2. A system as claimed in Claim 1, wherein said copy protection comprises one or more copy guard signals imposed during a blanking interval of the video signal, and wherein said detector means is arranged to establish the presence of said copy guard signals in the blanking interval within a predetermined period from the start of said interval.

3. A system as claimed in Claim 2, wherein said detector means is enabled to detect said copy guard signals for said predetermined period.

4. A system as claimed in Claim 2 or 3, wherein said detector means is arranged to establish the presence of copy guard signals within a period of 20H from the rising or falling edge of the record enable signal.

5. A system as claimed in any preceding claim, further comprising a gate pulse generator arranged to generate gate pulses in response to an edge of an input head switch pulse and to an edge of horizontal synchronizing pulses of said video signal.

6. A system as claimed in any preceding claim, wherein said detector means comprises a level detector for outputting a signal representative of the presence of copy protection when a clamped input level of said video signal exceeds a predetermined level.

7. A system as claimed in Claim 6, wherein said detector means further comprises means for generating an output inhibit signal in response to the arrival of said signal representative of the presence of copy protection between the arrival of two spaced gate pulses.

8. A system for controlling the recording of a copy protected video signal substantially as hereinbefore described with reference to the accompanying drawings.