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ABSTRACT

An image signal processor which comprises a memory device (9) for storing an image signal representative of a picture during one field period; an operating unit (18) for generating a READ-OUT command necessary to read out contents stored in the memory device from the memory device; a selector (SW 1) for selectively switching the memory device (9) between a WRITE-IN READY condition and a READ-OUT READY condition; and a switching control unit (15) for generating a control signal necessary to control the switching operation of the selector (SW 1). The switching control unit is adapted to receive the READ-OUT command and a vertical synchronizing signal included in a composite video signal. The selector performs the switching operation in synchronism with the initial vertical synchronizing signal applied immediately after the READ-OUT command has been inputted.

(Fig. 1)