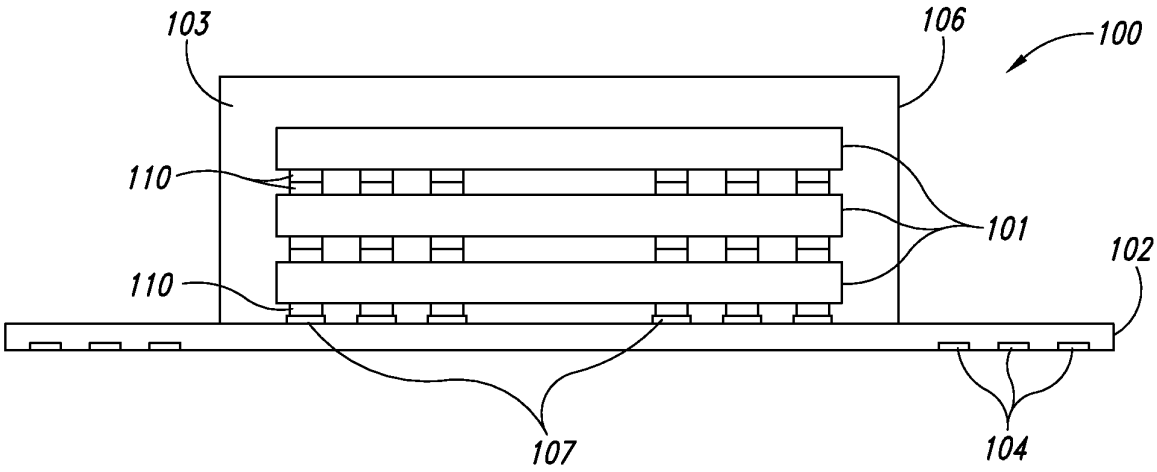

103
106
100
110
101
102
110
107
104

Fig. 1

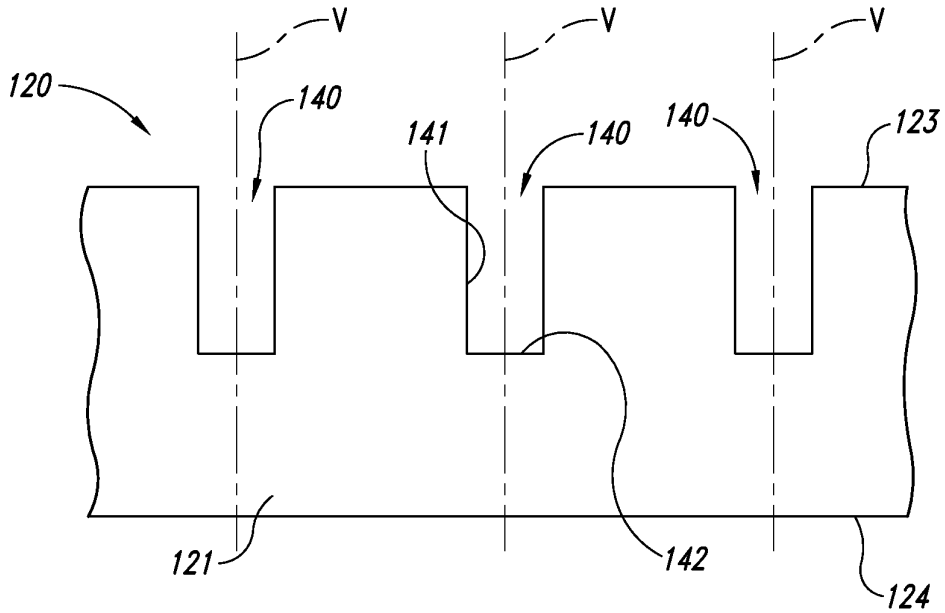

V
V
V
120
140
141
140
140
123
121
142
124

Fig. 2A

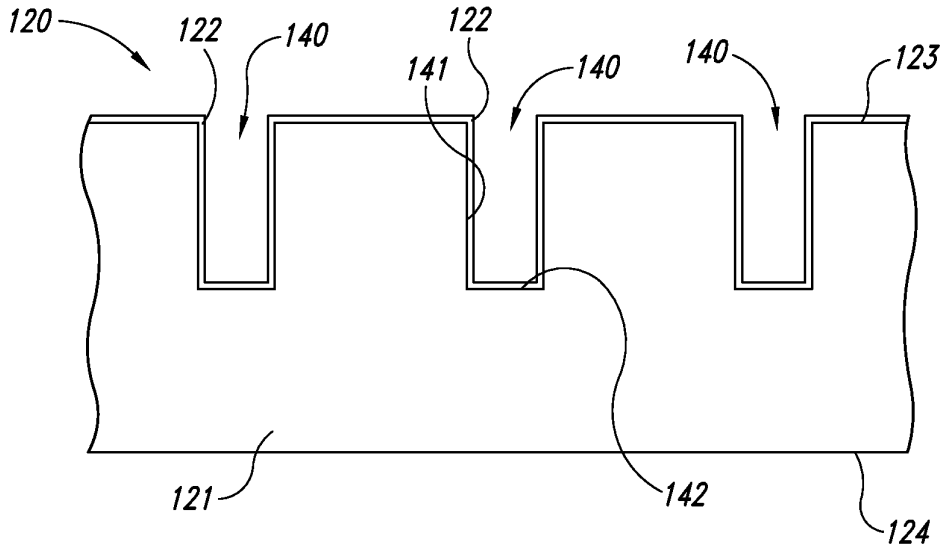

120
122
140
122
141
140
140
123
121
142
124

Fig. 2B

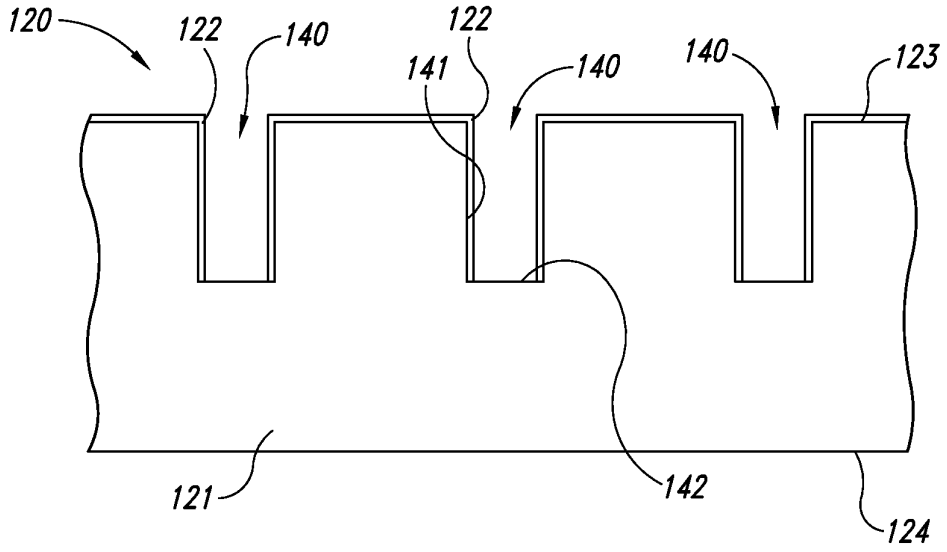

120
122
140
122
141
140
140
123
121
142
124

Fig. 2C

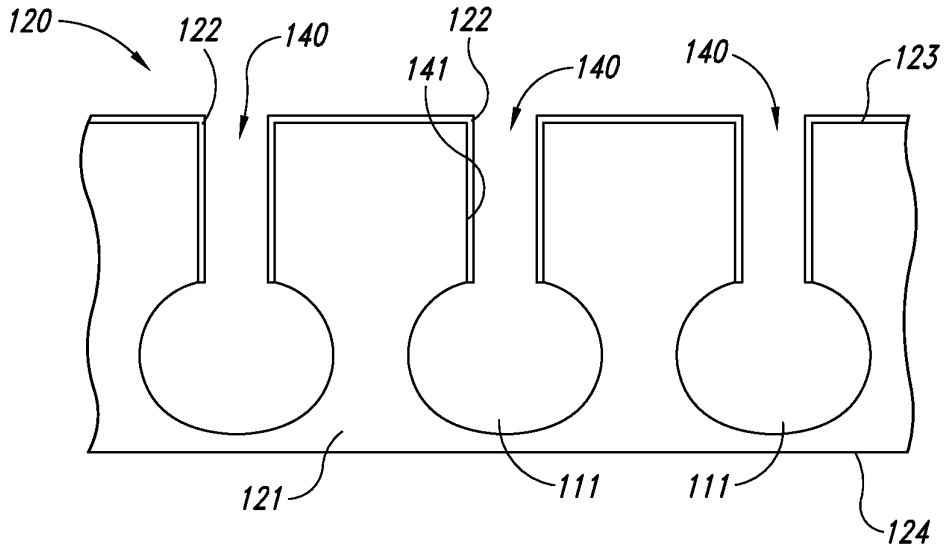

120
122
140
122
141
140
140
123
121
111
111
124

Fig. 2D

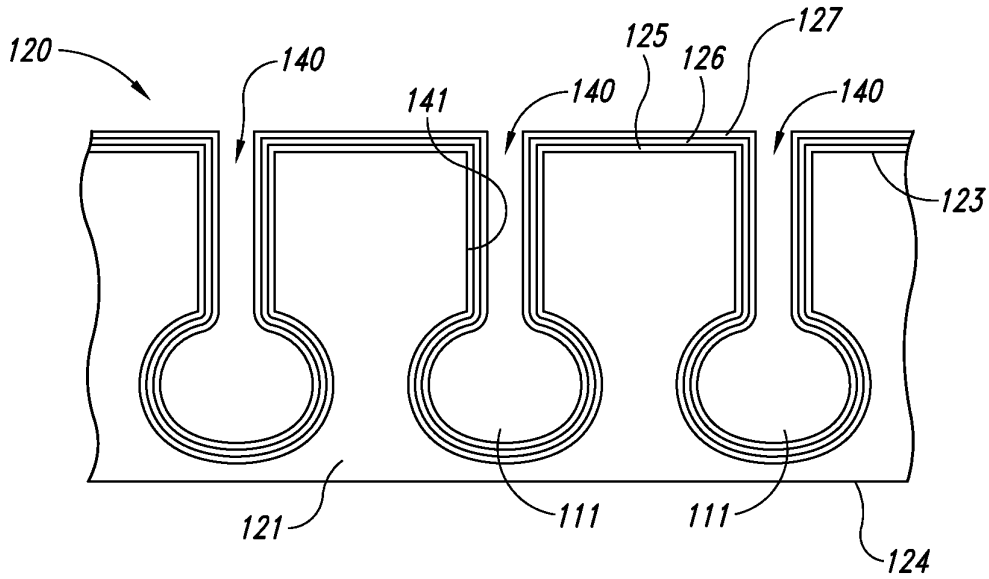

120
140
125
126
127
141
140
140
123
121
111
111
124

Fig. 2E

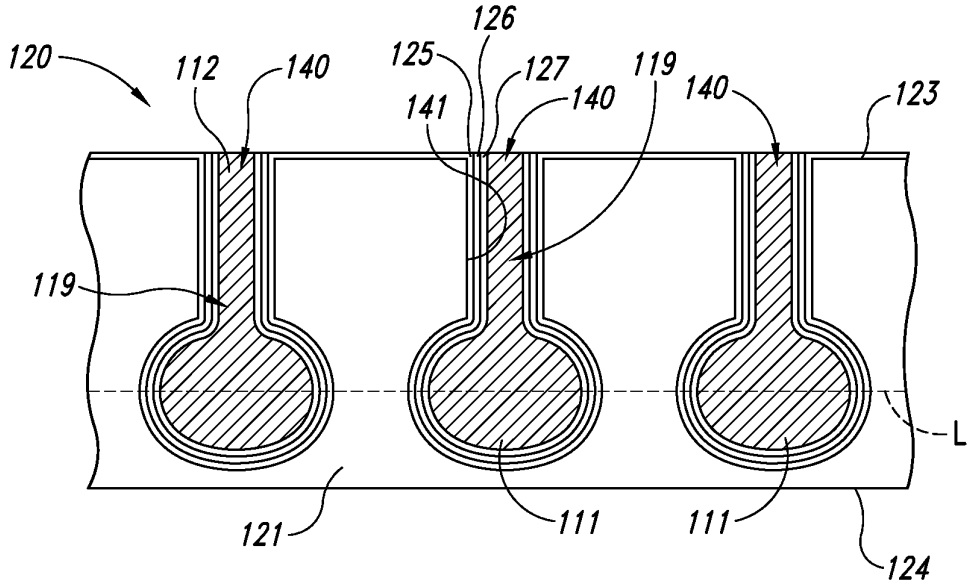

120
112
140
125
126
127
141
140
119
140
123
119
L
121
111
111
124

Fig. 2F

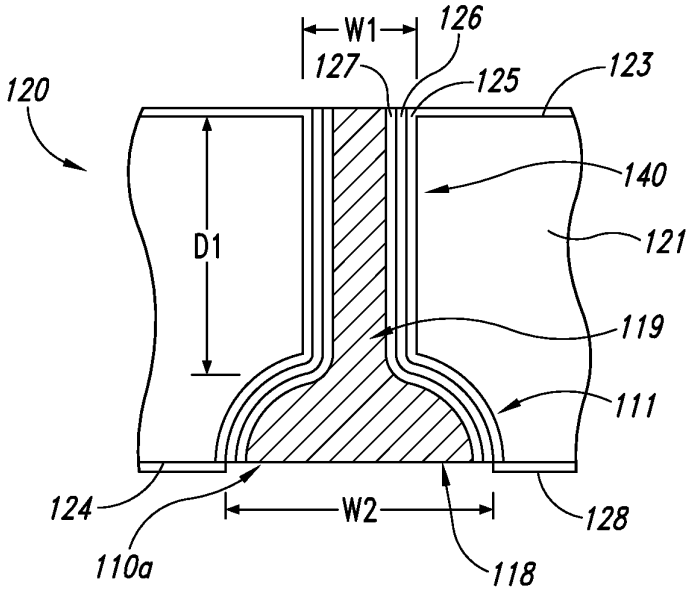

W1
126
127
125
123
120
140
D1
121
119
111
124
W2
128
110a
118

Fig. 2G

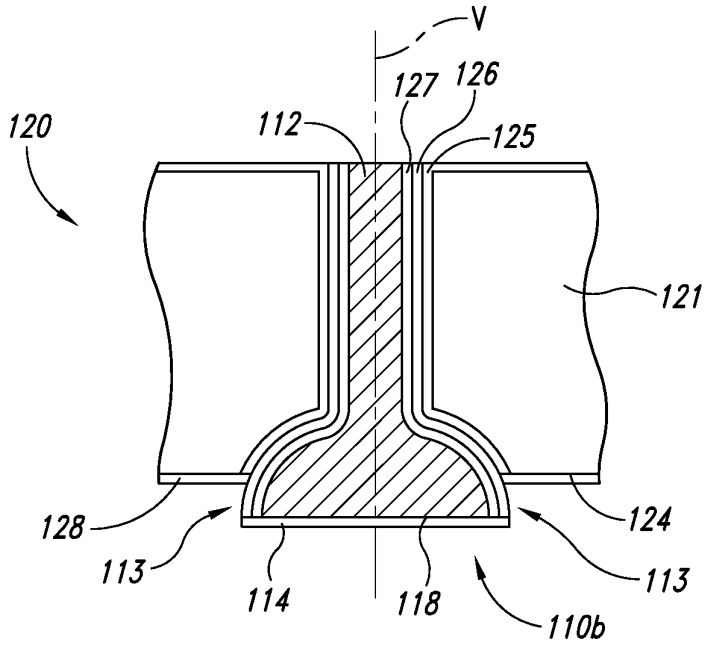

V
127
126
120
112
125
121
128
124
113
113
114
118
110b

Fig. 2H

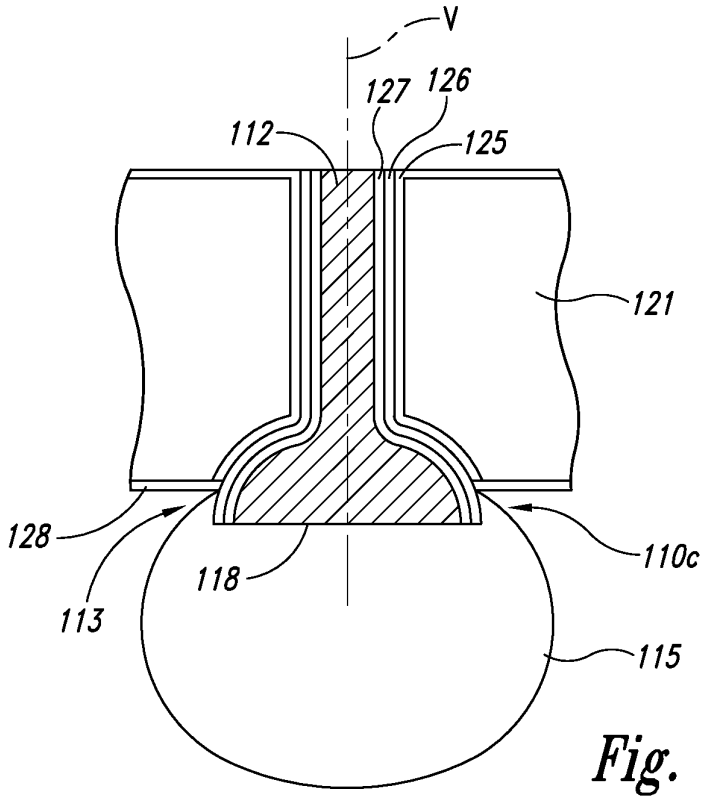

V
127
126
112
125
121
128
110c
118
113
115

Fig. 2I

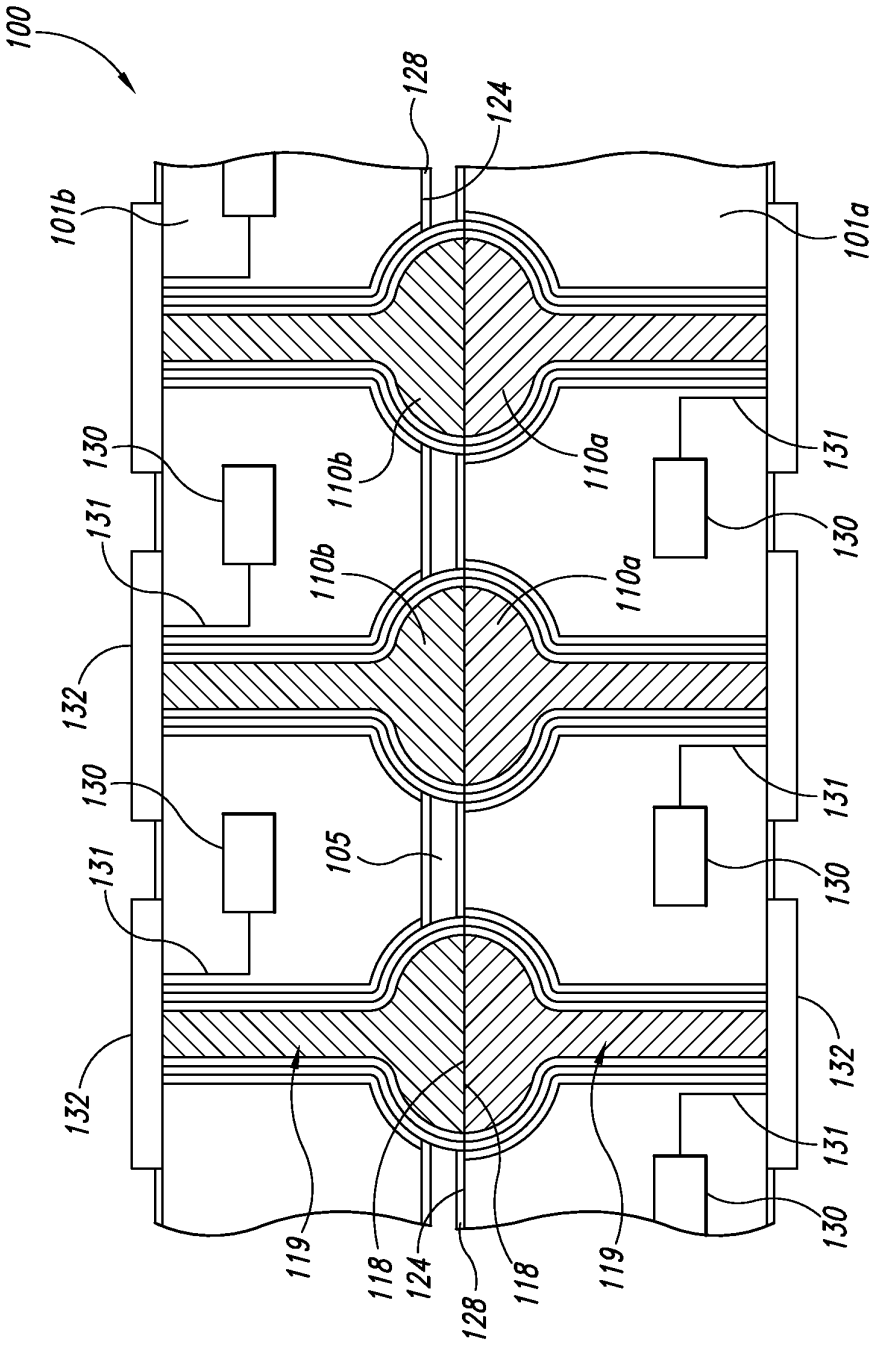

100
128
124
101b
101a
130
131
110b
110a
131
130
110b
110a
132
130
131
105
131
130
132
132
131
130
119
118
124
128
118
119

Fig. 2J

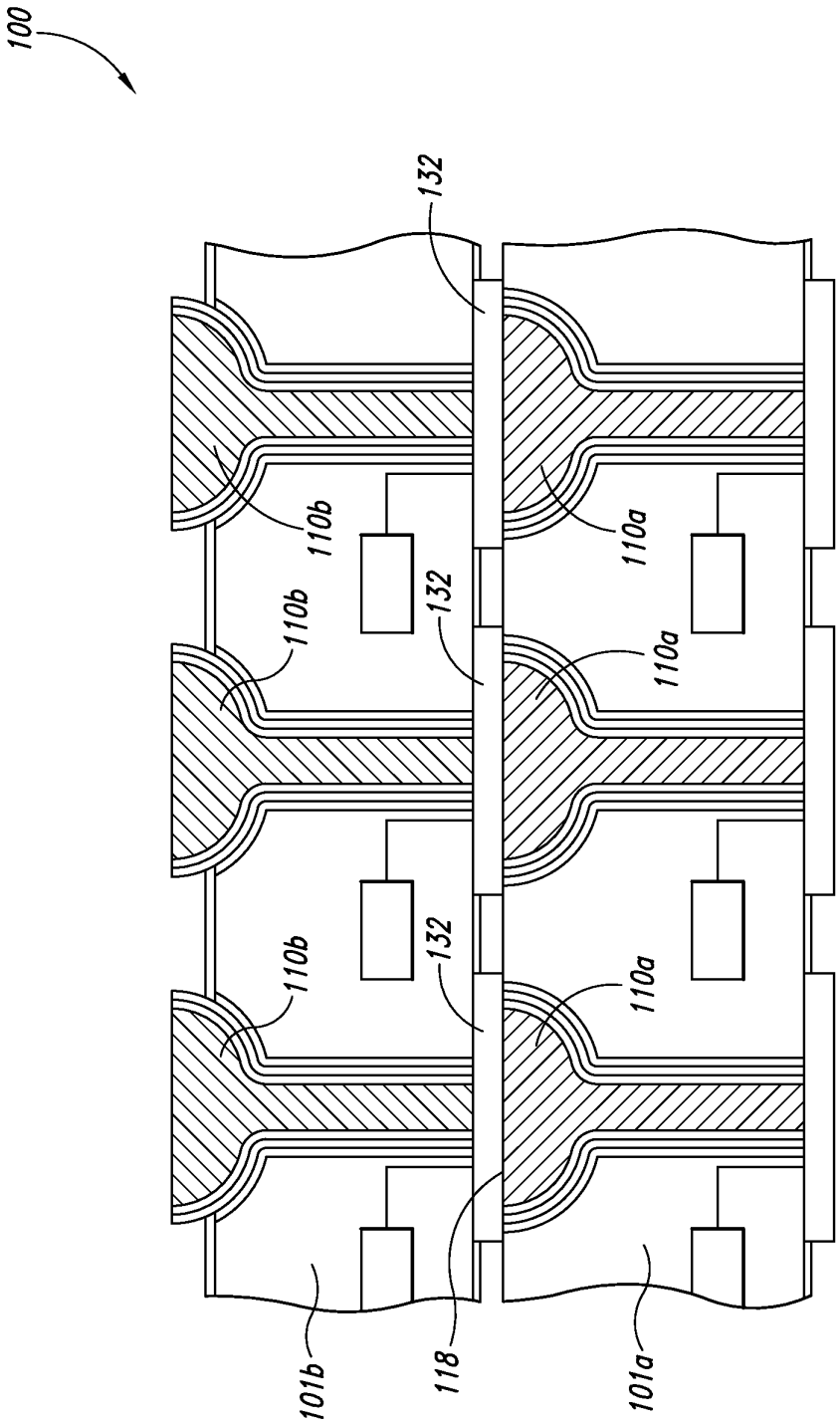


Fig. 2K

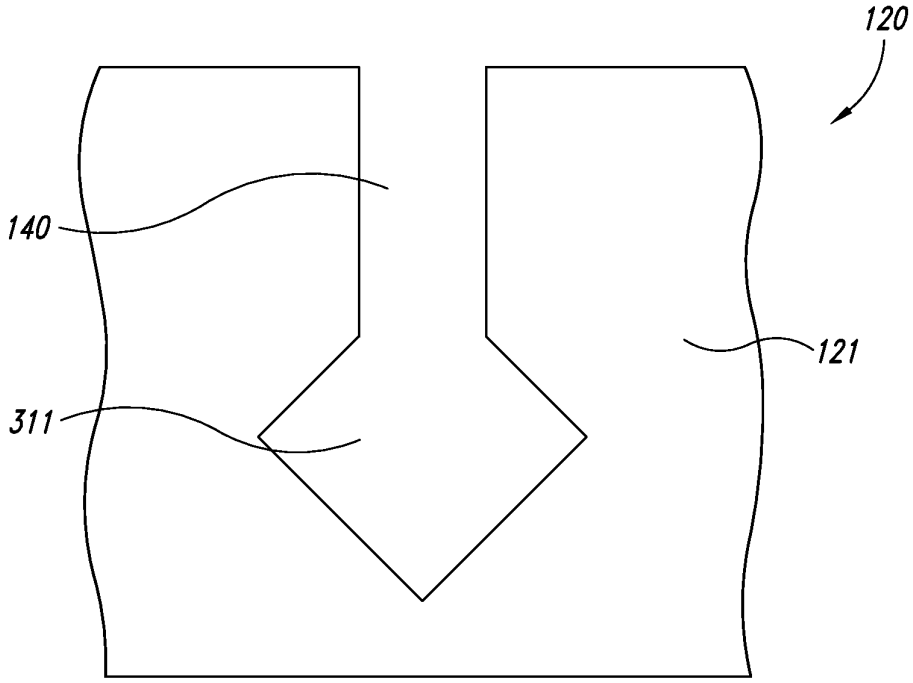


Fig. 3A

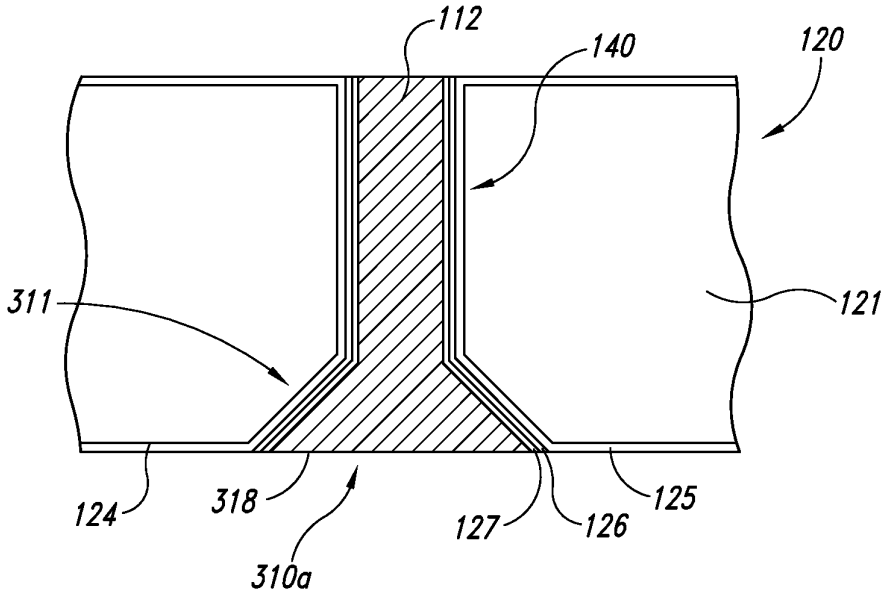


Fig. 3B

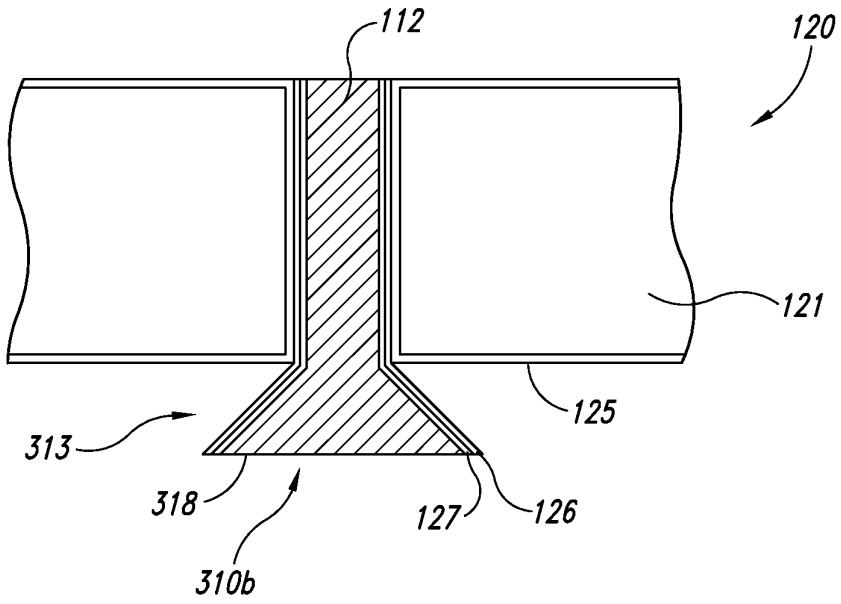

112
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318
127
126
310b

Fig. 3C

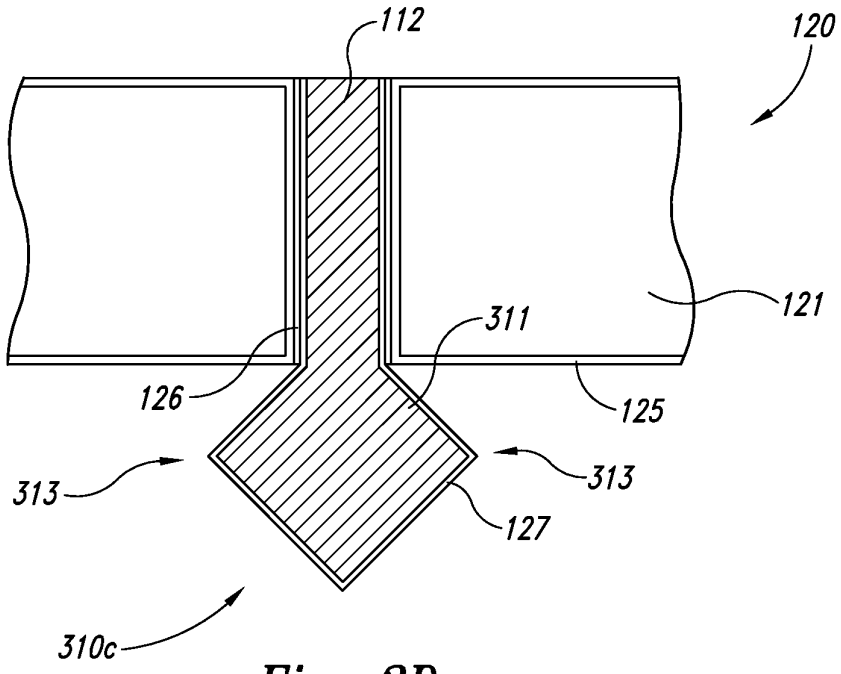

112
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311
126
125
313
313
127
310c

Fig. 3D

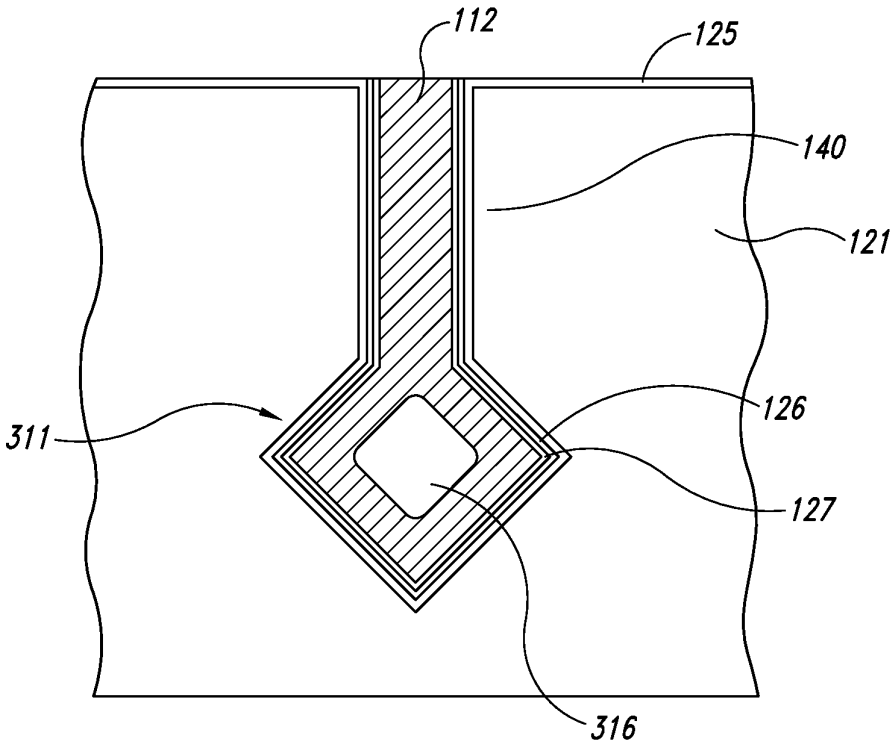

112
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126
127
316

Fig. 3E

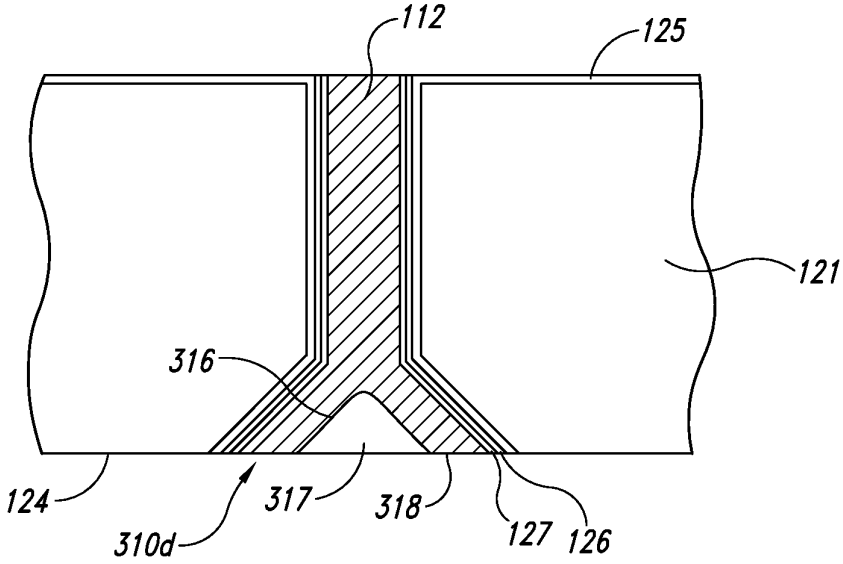

112
125
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316
124
310d
317
318
127
126

Fig. 3F

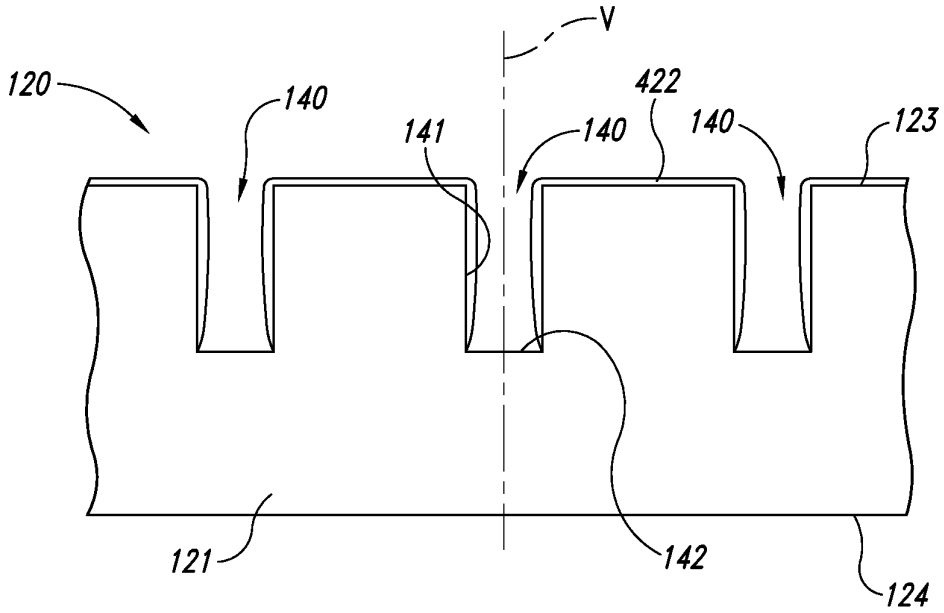

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124

Fig. 4

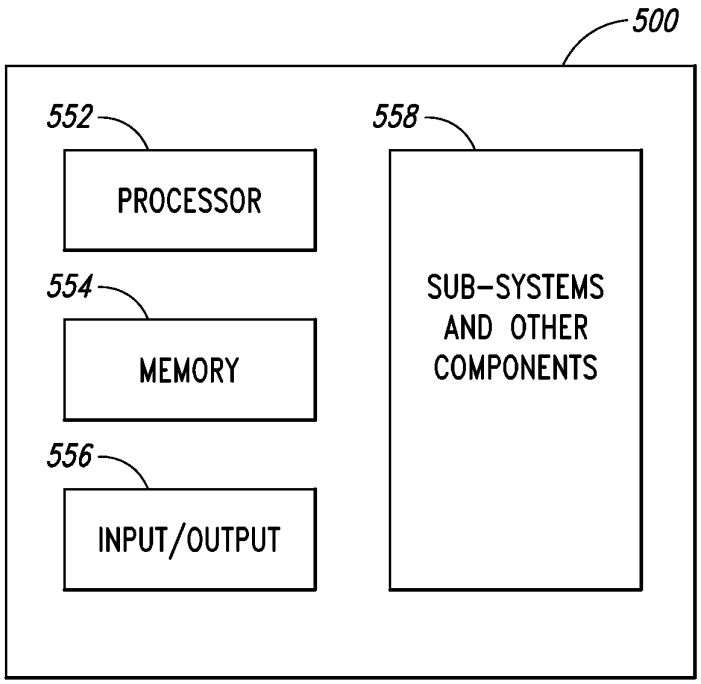

500
552
PROCESSOR
554
MEMORY
556
INPUT/OUTPUT
558
SUB-SYSTEMS AND OTHER COMPONENTS

Fig. 5