CLAIMS

1. An integrated structure for an optoelectronic device, the integrated structure comprising:

a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit for the optoelectronic device;

a plurality of optical elements on the CMOS backplane, wherein the plurality of optical elements are based on a material system different from CMOS and are disposed in different device layers;

a first bonding dielectric provided between the CMOS backplane and a first one of the different device layers for monolithic integration; and

a second bonding dielectric provided between respective ones of the different device layers for monolithic integration, the second bonding dielectric being transparent;

wherein the second bonding dielectric is the same as the first bonding dielectric.

2. The integrated structure of claim 1, wherein each device layer comprises a reflector disposed below a first optical element in said each device layer, wherein the reflector is configured to be reflective at a first operating wavelength range of a first optical element.

3. The integrated structure of claim 2, wherein the reflector is configured to be transmissive at a second operating wavelength range of a second optical element in a lower device layer.

4. The integrated structure of claims 2 or 3, wherein the reflector comprises a distributed Bragg reflector, DBR.

5. The integrated structure of any one of claims 2 to 4, wherein at least a portion of an electrical interconnection metal in each device layer functions as the reflector.

6. The integrated structure of any one of claims 1 to 5, wherein respective top contacts of the optical elements in the same device layer are connected to a common top electrode, and respective bottom contacts of the optical elements in the same device layer are individually connected to the driver circuit.

7. The integrated structure of any one of claims 1 to 5, wherein respective bottom contacts of the optical elements in the same device layer are connected to a common electrode, and respective top contacts of the optical elements in the same device layer are individually connected to the driver circuit.

8. The integrated structure of claim 7, comprising micro-trenches patterned between optical elements in the same device layer through the common bottom electrode to achieve optical isolation between the optical elements in the same device layer without breaking the electrical continuity of the common bottom electrode.

9. The integrated structure of claims 7 or 8, comprising metal pads, lines or net patterned on the common bottom electrode with direct electrical contact to enhance current spreading.

10. The integrated structure of any one of claims 6 to 9, comprising micro-structures patterned on respective bottom layers of the optical elements to enhance a light extraction from the optical elements.

11. The integrated structure of any one of claims 6 to 10, comprising a photonic crystal structure patterned on respective bottom layers of the optical elements to increase an emission directionality of light from the optical elements.

12. The integrated structure of any one of claims 1 to 11, wherein at least some of the optical elements in different device layer are horizontally interlaced.

13. The integrated structure of any one of claims 1 to 12, wherein at least some of the optical elements in different device layer at least partially overlap.

14. The integrated structure of claim 13, wherein the optical devices comprise at least partially overlapping RGB micro-light emitting diodes, micro-LEDs, in a pixel arrangement for enhancing color mixing.

15. The integrated structure of any one of the preceding claims, further comprising electrical interconnections including one or more of a group consisting of chemical mechanical planarization based contact, tungsten plug, and metal pad.

16. The integrated structure of any one of the preceding claims, further comprising at least one micro-lens to assist light collimation.

17. The integrated structure of any one of the preceding claims, comprising one or more redundant tungsten plugs to prevent crosstalk between adjacent optical elements.

18. A method of fabricating an integrated structure for an optoelectronic device, the method comprising the steps of:

providing a complementary metal-oxide-semiconductor, CMOS, backplane comprising a driver circuit for the optoelectronic device; and

providing a plurality of optical elements on the CMOS backplane, wherein the plurality of optical elements are based on a material system different from CMOS and are disposed in different device layers;

wherein a first bonding dielectric is provided between the CMOS backplane and a first one of the different device layers for monolithic integration; and

wherein a second bonding dielectric is provided between respective ones of the different device layers for monolithic integration, the second bonding dielectric being transparent;

wherein the second bonding dielectric is the same as the first bonding dielectric.

19. The method of claim 18, comprising providing, in each device layer, a reflector disposed below a first optical element in said each device layer, wherein the reflector is configured to be reflective at a first operating wavelength range of a first optical element.

20. The method of claim 19, wherein the reflector is configured to be transmissive at a second operating wavelength range of a second optical element in a lower device layer.

21. The method of claims 19 or 20, wherein the reflector comprises a distributed Bragg reflector, DBR.

22. The method of any one of claims 19 to 21, comprising providing, in each device layer, an electrical interconnection metal, wherein at least a portion of an electrical interconnection metal functions as the reflector.

23. The method of any one of claims 18 to 22, comprising connecting respective top contacts of the optical elements in the same device layer to a common top electrode, and connecting respective bottom contacts of the optical elements in the same device layer individually to the driver circuit.

24. The method of any one of claims 18 to 22, comprising connecting respective bottom contacts of the optical elements in the same device layer to a common electrode, and connecting respective top contacts of the optical elements in the same device layer individually to the driver circuit.

25. The method of claim 24, comprising patterning micro-trenches between optical elements in the same device layer through the common bottom electrode to achieve optical isolation between the optical elements in the same device layer without breaking the electrical continuity of the common bottom electrode.

26. The method of claims 24 or 25, comprising patterning metal pads, lines or net on the common bottom electrode with direct electrical contact to enhance current spreading.

27. The method of any one of claims 23 to 26, comprising patterning micro-structures on respective bottom layers of the optical elements to enhance a light extraction from the optical elements.

28. The method of any one of claims 23 to 27, comprising patterning a photonic crystal structure on respective bottom layers of the optical elements to increase an emission directionality of light from the optical elements.

29. The method of any one of claims 18 to 28, comprising horizontally interlacing at least some of the optical elements in different device layer.

30. The method of any one of claims 18 to 29, comprising at least partially overlapping at least some of the optical elements in different device layer.

31. The method of claim 30, comprising at least partially overlapping RGB micro-light emitting diodes, micro-LEDs, in a pixel arrangement for enhancing color mixing.

32. The method of any one of claims 18 to 31, further comprising providing electrical interconnections including one or more of a group consisting of chemical mechanical planarization based contact, tungsten plug, and metal pad.

33. The method of any one of claims 18 to 32, further comprising providing at least one micro-lens to assist light collimation.

34. The method of any one of claims 18 to 33, comprising providing one or more redundant tungsten plugs to prevent crosstalk between adjacent optical elements.