CLAIMS

What is claimed is:

1. A Phase-Change Memory (PCM) storage element, comprising:

an n-type semiconductor layer in direct contact with a p-type chalcogenide material to form a diode embedded with the PCM storage element, wherein the diode is used to select the PCM storage element.

2. The PCM storage element of claim 1 wherein the PCM storage element changes state with or without a heater element.

3. The PCM storage element of claim 1 wherein the n-type semiconductor layer is an oxide-based semiconductor layer and the p-type chalcogenide material is a phase change alloy.

4. The PCM storage element of claim 3 wherein the oxide-based semiconductor layer is a Zinc Oxide (ZnO) layer.

5. The PCM storage element of claim 3 wherein the phase change alloy is a Ge, Sb, Te (GST) alloy.

6. The PCM storage element of claim 5 wherein a bias applied to the diode allows two states of the PCM storage element to be detected by reading a resistance of the GST alloy.

7. The PCM storage element of claim 5 wherein the ZnO layer is directly above the GST alloy.

8. The PCM storage element of claim 5 wherein the GST alloy is directly above the ZnO layer.

9. A storage cell, comprising:

a selector diode formed by a Zinc Oxide (ZnO) layer in direct contact with a Phase-Change Memory layer, where the selector diode is biased to allow a state of the storage cell to be detected by reading a resistance of the PCM layer.

10. The storage cell of claim 9 wherein the storage cell is realized with or without a heater element:

11. The storage cell of claim 9 wherein the PCM layer is naturally p-type and the ZnO layer is n-type to form the selector diode employed for selecting the storage cell.

12. The storage cell of claim 9 wherein the ZnO layer is deposited using Atomic Layer Deposition (ALD).

13. The storage cell of claim 9 wherein the ZnO layer is deposited directly above the PCM layer.

14. The storage cell of claim 9 wherein the PCM layer is deposited directly above the ZnO layer.

15. The storage cell of claim 9 wherein the PCM layer is a chalcogenide material.

16. A Phase-Change Memory (PCM), comprising:

a memory cell having an n-type Zinc Oxide (ZnO) layer deposited in direct contact with a natural p-type crystalline PCM material to form a diode junction embedded in the PCM material; and

a capping layer adjacent to the ZnO layer to form a stack with the ZnO layer and the PCM material.

17. The PCM of claim 16 wherein a storage in the PCM material is done with or without a heater element.

18. The PCM of claim 16 wherein a positive bias of two volts or less forward biases the diode junction to allow detection of a state of the memory cell by reading a resistance of the PCM material

19. The PCM of claim 16 wherein the ZnO layer is deposited using Atomic Layer Deposition (ALD).

20. The PCM of claim 15 wherein the ZnO layer is deposited directly above the PCM material.

21. The PCM of claim 15 wherein the PCM material is deposited directly above the ZnO layer.

CLAIMS

What is claimed is:

1. A Phase-Change Memory (PCM), comprising:
a first metal line;
a second metal line;
a dielectric between the first and second metal lines;
a first barrier between the first metal line and the dielectric and contacting the first metal line and the dielectric;
a second barrier between the second metal line and the dielectric and contacting the second metal line and the dielectric;
a first memory cell having an oxide-based material including an n-type Zinc Oxide (ZnO) material in direct contact with a natural p-type crystalline PCM material to form a diode junction embedded in the PCM material, the ZnO material contacting the first metal line;
first material arranged in a stack with the ZnO material and the PCM material;
a second memory cell having an oxide-based material including an n-type ZnO material in direct contact with a natural p-type crystalline PCM material to form a diode junction embedded in the PCM material, the ZnO material contacting the second metal line; and
a second material arranged in a stack with the ZnO material and the PCM material of the second memory cell.

2. The PCM of claim 1 wherein each of the first and second metal lines includes copper.

3. The PCM of claim 1 wherein a positive bias of two volts or less forward biases the diode junction to allow detection of a state of the memory cell by reading a resistance of the PCM material.

4. The PCM of claim 1 wherein the first material includes TiN.

5. The PCM of claim 1 wherein the second material includes TiN.

6. The PCM of claim 1 wherein the PCM material is deposited directly above the ZnO material.