CONFIGURABLE FILTER FOR PROCESSING TELEVISION AUDIO SIGNALS

RELATED APPLICATION AND TECHNICAL FIELD

[0001] This application is related to the following U.S. application, of common assignee, from which priority is claimed, and the contents of which are incorporated herein in their entirety by reference: "Multiplexed Infinite – Impulse Response (IIR) Filter Section For Broadcast Television Audio Application," U.S. Provisional Patent Application Serial No. 60/555,853, filed March 24, 2004.

[0002] This disclosure relates to processing television audio signals and, more particularly, to a configurable filter for use with encoding and decoding television audio signals.

BACKGROUND

[0003] In 1984, the United States, under the auspices of the Federal Communications Commission, adopted a standard for the transmission and reception of stereo audio for television. This standard is codified in the FCC's Bulletin OET-60, and is often called the BTSC system after the Broadcast Television Systems Committee that proposed it, or the MTS (Multi-channel Television Sound) system.

[0004] Prior to the BTSC system, broadcast television audio was monophonic, consisting of a single "channel" or signal of audio content. Stereo audio typically requires the transmission of two independent audio channels, and receivers capable of detecting and recovering both channels. In order to meet the FCC's requirement that the new transmission standard be 'compatible' with existing monophonic television sets (i.e., that mono receivers be capable of reproducing an appropriate audio signal from the new type of stereo broadcast), the Broadcast Television Systems Committee adopted an approach similar to FM radio systems: stereo Left and Right audio signals are combined to form two new signals, a Sum signal and a Difference signal.

[0005] Monophonic television receivers detect and demodulate only the Sum signal, consisting of the addition of the Left and Right stereo signals. Stereo-capable receivers receive both the Sum and the Difference signals, recombining the signals to extract the original stereo Left and Right signals.

[0006] For transmission, the Sum signal directly modulates the aural FM carrier just as would a monophonic audio signal. The Difference channel, however, is first modulated onto an AM subcarrier located 31.768 kHz above the aural carrier's center frequency. The nature of FM modulation is such that background noise increases by 3 decibel (dB) per octave, and as a result, because the new subcarrier is located further from the aural carrier's center frequency than the Sum or mono signal, additional noise is introduced into the Difference channel, and hence into the recovered stereo signal. In many circumstances, in fact, this rising noise characteristic renders the stereo signal too noisy to meet the requirements imposed by the FCC, and so the BTSC system mandates a noise reduction system in the Difference channel signal path.

[0007] This system, sometimes referred to as dbx noise reduction (after the company that developed the technique) is of the companding type, comprising an encoder and decoder. The encoder adaptively filters the Difference signal prior to transmission such that amplitude and frequency content, upon decoding, hide ("mask") noise picked up during the transmission process. The decoder completes the process by restoring the Difference signal to original form and thereby ensuring that noise is audibly masked by the signal content.

[0008] The dbx noise reduction system is also used to encode and decode Secondary Audio Programming (SAP) signals, which is defined in the BTSC standard as an additional information channel and is often used to e.g., carry programming in an alternative language, reading services for the blind, or other services.

[0009] Cost is, of course, of prime concern to television manufacturers. As a result of

intense competition and consumer expectations, profit margins on consumer electronics products, especially television products, can be vanishingly small. Because the dbx decoder is located in the television receiver, manufacturers are sensitive to the cost of the decoder, and reducing the cost of the decoder is a necessary and worthwhile goal. While the encoder is not located in a television receiver and is not as sensitive from a profit standpoint, any development which will decrease manufacturing costs of the encoder also provides a benefit.

SUMMARY OF THE DISCLOSURE

[0010] In accordance with an aspect of the disclosure, a television audio signal encoder includes a matrix that sums a left channel audio signal and a right channel audio signal to produce a sum signal. The matrix also subtracts one of the left and right audio signals from the other to produce a difference signal. The encoder also includes a configurable infinite impulse response digital filter that selectively uses one or more sets of filter coefficients to filter the difference signal. Each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for transmission.

[0011] In one embodiment, the configurable infinite impulse response digital filter may include a selector that selects one of the one or more sets of filter coefficients. The configurable infinite impulse response digital filter may include a selector that selects an input signal from a group of input signals. One input signal from the group of input signals may include an output signal of the configurable infinite impulse response digital filter. The configurable infinite impulse response digital filter may be a second order infinite impulse response filter. Furthermore, the configurable infinite impulse response digital filter may be configured as a low pass filter, a high pass filter, bandpass filter, an emphasis filter, etc. The selection of the filter coefficients may based on a rate that the television audio signal is sampled. The sets of filter coefficients may be stored in a memory or in a

look – up table that is stored in memory. The television audio signal may comply to the Broadcast Television System Committee (BTSC) standard, the Near Instantaneously Companded Audio Muliplex (NICAM) standard, the A2/Zweiton standard, the EIA – J standard, or other similar audio standard. The configurable infinite impulse response digital filter may be implemented in an integrated circuit.

[0012] In accordance with another aspect of the disclosure, a television audio signal decoder includes a configurable infinite impulse response digital filter that selectively uses one or more sets of filter coefficients to filter a difference signal. The difference signal is produced by subtracting one of a left channel and a right channel audio signal from the other audio signal. Each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for separating the left channel and right channel audio signals. The decoder also includes a matrix that separates the left channel and right channel audio signals from the difference signal and a sum signal. The sum signal includes the sum the left channel audio signal and the right channel audio signal.

[0013] In one embodiment, the configurable infinite impulse response digital filter may include a selector that selects one of the one or more sets of filter coefficients. The configurable infinite impulse response digital filter may include a selector that selects an input signal from a group of input signals. One input signal from the group of input signals may include an output signal of the configurable infinite impulse response digital filter. The configurable infinite impulse response digital filter may be a second order infinite impulse response filter. Furthermore, the configurable infinite impulse response digital filter may be configured as a low pass filter, a high pass filter, bandpass filter, an emphasis filter, etc. The selection of the filter coefficients may based on a rate that the television audio signal is sampled. The sets of filter coefficients may be stored in a memory or in a look – up table that is stored in memory. The television audio signal may comply to the Broadcast Television System Committee (BTSC) standard, the Near Instantaneously

Companded Audio Muliplex (NICAM) standard, the A2/Zweiton standard, the EIA – J standard, or other similar audio standard. The configurable infinite impulse response digital filter may be implemented in an integrated circuit.

[0014] In accordance with another aspect of the disclosure, a digital BTSC signal encoder for encoding digital left and right channel audio signals so that the encoded left and right channel audio signals can be subsequently decoded so as to reproduce the digital left and right channel audio signals with little or no distortion of the signal content of the digital left and right channel audio signals includes, a matrix that sums the left channel audio signal and the right channel audio signal to produce a sum signal. The matrix also subtracts one of the left and right audio signals from the other to produce a difference signal. The BTSC encoder also includes a configurable infinite impulse response digital filter that selectively uses one or more sets of filter coefficients to filter the difference signal. Each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for transmission and to comply with the BTSC standard.

[0015] In one embodiment, the configurable infinite impulse response digital filter may include a selector that selects one of the one or more sets of filter coefficients. The configurable infinite impulse response digital filter may include a selector that selects an input signal from a group of input signals. One input signal from the group of input signals may include an output signal of the configurable infinite impulse response digital filter. The configurable infinite impulse response digital filter may be a second order infinite impulse response filter. Furthermore, the configurable infinite impulse response digital filter may be configured as a low pass filter, a high pass filter, bandpass filter, an emphasis filter, etc. The selection of the filter coefficients may based on a rate that the television audio signal is sampled. The sets of filter coefficients may be stored in a memory or in a look – up table that is stored in memory.

[0016] In accordance with another aspect of the disclosure, a digital BTSC signal

decoder for decoding digital left and right channel audio signals with little or no distortion of the signal content of the digital left and right channel audio signals, includes, a configurable infinite impulse response digital filter that selectively uses one or more sets of filter coefficients to filter a difference signal that complies with the BTSC standard. The difference signal is produced by subtracting one of a left channel and a right channel audio signal from the other audio signal. Each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for separating the left channel and right channel audio signals. BTSC signal decoder also includes a matrix that separates the left channel and right channel audio signals from the difference signal and a sum signal. The sum signal includes the sum the left channel audio signal and the right channel audio signal.

[0017] In one embodiment, the configurable infinite impulse response digital filter may include a selector that selects one of the one or more sets of filter coefficients. The configurable infinite impulse response digital filter may include a selector that selects an input signal from a group of input signals. One input signal from the group of input signals may include an output signal of the configurable infinite impulse response digital filter. The configurable infinite impulse response digital filter may be a second order infinite impulse response filter. Furthermore, the configurable infinite impulse response digital filter may be configured as a low pass filter, a high pass filter, bandpass filter, an emphasis filter, etc. The selection of the filter coefficients may based on a rate that the television audio signal is sampled. The sets of filter coefficients may be stored in a memory or in a look – up table that is stored in memory.

[0018] In accordance with another aspect of the disclosure, a computer program product residing on a computer readable medium has stored instructions that when executed by a processor, cause the processor to sum a left channel audio signal and a right channel audio signal to produce a sum signal. Executed instructions also cause the processor to subtract one of the left and right audio signals from the other signal to produce

a difference signal. Furthermore, executed instructions cause the processor to select one or more sets of filter coefficients to filter the difference signal with a configurable infinite impulse response digital filter. Each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for transmission.

[0019] In one embodiment, the computer program product further includes instructions that, when executed, may select an input signal from a group of input signals.

[0020] In accordance with another aspect of the disclosure, a computer program product residing on a computer readable medium stores instructions which, when executed by a processor, cause that processor to select one or more sets of filter coefficients to filter a difference signal with an infinite impulse response digital filter. The difference signal is produced by subtracting one of a left channel and a right channel audio signal from the other audio signal. The selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for separating the left channel and right channel audio signals. Executed instructions also cause the processor to separate the left channel and right channel audio signals from the difference signal and a sum signal. The sum signal includes the sum the left channel audio signal and the right channel audio signal.

[0021] In one embodiment, the computer program product further includes instructions that, when executed, may select an input signal from a group of input signals.

[0022] In accordance with another aspect of the disclosure, a television audio signal encoder includes an input stage that receives a secondary audio programming signal. The television audio signal encoder also includes a configurable infinite impulse response digital filter that selectively uses one or more sets of filter coefficients to filter the secondary audio programming signal. Each selectable set of filter coefficients is associated with a unique filtering application to prepare the secondary audio programming signal for transmission.

[0023] In one embodiment, the configurable infinite impulse response digital filter may include a selector that selects one of the one or more sets of filter coefficients. The configurable infinite impulse response digital filter may include a selector to select an input signal from a group of input signals. One input signal from the group of input signals may include an output signal of the configurable infinite impulse response digital filter. The configurable infinite impulse response digital filter may be a second order infinite impulse response filter.

[0024] In accordance with another aspect of the disclosure, a television audio signal decoder includes a configurable infinite impulse response digital filter that selectively uses one or more sets of filter coefficients to filter a secondary audio programming signal. Each selectable set of filter coefficients is associated with a unique filtering application to prepare the secondary audio programming signal for a television receiver system.

[0025] In one embodiment, the configurable infinite impulse response digital filter may include a selector that selects one of the one or more sets of filter coefficients. The configurable infinite impulse response digital filter may include a selector to select an input signal from a group of input signals. One input signal from the group of input signals may include an output signal of the configurable infinite impulse response digital filter. The configurable infinite impulse response digital filter may be a second order infinite impulse response filter.

[0026] Additional advantages and aspects of the present disclosure will become readily apparent to those skilled in the art from the following detailed description, wherein embodiments of the present invention are shown and described, simply by way of illustration of the best mode contemplated for practicing the present invention. As will be described, the present disclosure is capable of other and different embodiments, and its several details are susceptible of modification in various obvious respects, all without departing from the spirit of the present disclosure. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as limitative.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram representing a television signal transmission system that is configured to comply with the BTSC television audio signal standard.

FIG. 2 is a block diagram representing a portion of a BTSC encoder included in the television signal transmission system shown in FIG. 1.

FIG. 3 is a block diagram representing a television receiver system that is configured to receive and decode BTSC television audio signals sent by the television signal transmission system shown in FIG. 1.

FIG. 4 is a block diagram representing a portion of a BTSC decoder included in the television receiver system shown in FIG. 3.

FIG. 5 is a diagrammatic view of a configurable second – order infinite impulse response filter with selectable inputs.

FIG. 6 is a graphical representation of a transfer function of the second – order infinite impulse response filter shown in FIG. 5.

FIG. 7 is a block diagram of a portion of a BTSC encoder that highlights operations that may be performed by the configurable second – order infinite impulse response filter shown in FIG. 5.

FIG. 8 is a block diagram of a portion of a BTSC decoder that highlights operations that may be performed by the configurable second – order infinite impulse response filter shown in FIG. 5.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0027] Referring to FIG. 1, a functional block diagram of a BTSC compatible television signal transmitter 10 includes five lines (e.g., conductive wires, cables, etc.) that provide signals for transmission. In particular, left and right audio channels are provided on respective lines 12 and 14. An SAP signal is provided by line 16 in which the signal has content to provide additional channel information (e.g., alternative languages, etc.). A

fourth line 18 provides a professional channel that is typically used by broadcast television and cable television companies. Video signals are provided by a line 20 to a transmitter 22. The left, right, and SAP channels are provided to a BTSC encoder 24 that prepares the audio signals for transmission. Specifically, the left and right audio channels are provided to a matrix 26 that calculates a sum signal (e.g., L + R) and a difference signal (e.g., L – R) from the audio signals. Typically operations of matrix 26 are performed by utilizing a digital signal processor (DSP) or similar hardware or software – based techniques known to one skilled in the art of television audio and video signal processing. Once produced, sum and difference signals (i.e., L + R and L – R) are encoder for transmission. In particular, the sum signal (i.e., L + R) is provided to a pre-emphasis unit 28 that alters the magnitude of select frequency components of the sum signal with respect to other frequency components. The alteration may be in a negative sense in which the magnitude of the select frequency components are suppressed, or the alteration may be in a positive sense in which the magnitude of the select frequency components are enhanced.

[0028] The difference signal (i.e., L – R) is provided to a BTSC compressor 30 that adaptively filters the signal prior to transmission such that when decoded, the signal amplitude and frequency content suppress noise imposed during transmission. Similar to the difference signal, the SAP signal is provided to a BTSC compressor 32. An audio modulator stage 34 receives the processed sum signal, difference signal, and SAP signal. Additionally, signals from the professional channel are provided to audio modulator stage 34. The four signals are modulated by audio modulator stage 34 and provided to transmitter 22. Along with the video signals provided by the video channel, the four audio signals are conditioned for transmission and provided to an antenna 36 (or an antenna system). Various signal transmitting techniques known to one skilled in the art of television systems and telecommunications may be implemented by transmitter 22 and antenna 36. For example, transmitter 22 may be incorporated into a cable television system, a broadcast television system, or other similar television system.

[0029] Referring to FIG. 2, a block diagram representing operations performed by a portion of BTSC compressor 30 is shown. In general, the difference channel (i.e., L – R) processing performed by BTSC compressor 30 is considerably more complex than the sum channel (i.e., L + R) processing by pre-emphasis unit 28. The additional processing provided by the difference channel processing BTSC compressor 30, in combination with complementary processing provided by a decoder (not shown) receiving a BTSC signal, maintains the signal-to-noise ratio of the difference channel at acceptable levels even in the presence of the higher noise floor associated with the transmission and reception of the difference channel. BTSC compressor 30 essentially generates the encoded difference signal by dynamically compressing, or reducing the dynamic range of the difference signal so that the encoded signal may be transmitted through a limited dynamic range transmission path, and so that a decoder receiving the encoded signal may recover substantially all the dynamic range in the original difference signal by expanding the compressed difference signal in a complementary fashion. In some arrangements, BTSC compressor 30 is a particular form of the adaptive signal weighing system described in U.S. Patent No. 4,539,526, incorporated by reference herein, and which is known to be advantageous for transmitting a signal having a relatively large dynamic range through a transmission path having a relatively narrow, frequency dependent, dynamic range.

[0030] The BTSC standard rigorously defines the desired operation of BTSC encoder 24 and BTSC compressors 30 and 32. Specifically, the BTSC standard provides transfer functions and/or guidelines for the operation of each component included e.g., in BTSC compressor 30 and the transfer functions are described in terms of mathematical representations of idealized analog filters. Upon receiving the difference signal (i.e., L – R) from matrix 26, the signal is provided to an interpolation and fixed pre-emphasis stage 38. In some digital BTSC encoders, the interpolation is set for twice the sample rate and the interpolation may be accomplished by linear interpolation, parabolic interpolation, or a filter (e.g., a finite impulse response (FIR) filter, an infinite impulse response (IIR) filter, etc.) of n-th order. The interpolation and fixed pre-emphasis stage 38 also provides

pre-emphasis. After interpolation and pre-emphasis, the difference signal is provided to a divider 40 that divides the difference signal by a quantity determined from the difference signal and described in detail below.

[0031] The output of divider 40 is provided to a spectral compression unit 42 that performs emphasis filtering of the difference signal. In general, spectral compression unit 42 "compresses", or reduces the dynamic range, of the difference signal by amplifying signals having relatively low amplitudes and attenuating signals having relatively large amplitudes. In some arrangements spectral compression unit 42 produces an internal control signal from the difference signal that controls the pre-emphasis/de-emphasis that is applied. Typically, spectral compression unit 42 dynamically compresses high frequency portions of the difference signal by an amount determined by the energy level in the high frequency portions of the encoded difference signal. Spectral compression unit 42 thus provides additional signal compression toward the higher frequency portions of the difference signal. This is done because the difference signal tends to be noisier in the higher frequency portion of the spectrum. When the encoded difference signal is decoded with a spectral expander in a decoder, respectively in a complementary manner to the spectral compression unit of the encoder, the signal – to – noise ratio of the L – R signal is substantially preserved.

[0032] Once processed by spectral compression unit 42, the difference signal is provided to an over-modulation protection unit 44 and band-limiting unit 46. Similar to the other components, the BTSC standard provides suggested guidelines for the operation of over-modulation protection unit 44 and band-limiting unit 46. Generally, band-limiting unit 46 and a portion of over-modulation protection unit 44 may be described as low pass filters. Over-modulation protection unit 44 also performs as a threshold device that limits the amplitude of the encoded difference signal to full modulation, where full modulation is the maximum permissible deviation level for modulating an audio subcarrier in a television signal.

[0033] Two feedback paths 48 and 50 are included in BTSC compressor 30. Feedback path 50 includes a spectral control bandpass filter 52 that typically has a relatively narrow pass band that is weighted towards higher audio frequencies to provide a control signal for spectral compression unit 42. To condition the control signal produced by spectral control bandpass filter 52, feedback path 50 also includes a multiplier 54 (configured to square the signal provided by spectral control bandpass filter 52), an integrator 56, and a square root device that provides the control signal to spectral compression unit 42. Feedback path 48 also includes a bandpass filter (i.e., gain control bandpass filter 60) that filters the output signal from band-limiting unit 46 to set the gain applied to the output signal of interpolation and fixed pre-emphasis stage 38 via divider 40. Similar to feedback path 50, feedback path 48 also includes a multiplier 62, an integrator 64, and a square root device 66 to condition the signal that is provided to divider 40.

[0034] Referring to FIG. 3, a block diagram is shown that represents a television receiver system 68 that includes an antenna 70 (or a system of antennas) to receive BTSC compatible broadcast signals from television transmission system 10 (shown in FIG. 1). The signals received by antenna 70 are provided to a receiver 72 that is capable of detecting and isolating the television transmission signals. However, in some arrangements receiver 72 may receive the BTSC compatible signals from another television signal transmission technique known to one skilled in the art of television signal broadcasting. For example, the television signals may be provided to receiver 72 over a cable television system or a satellite television network.

[0035] Upon receiving the television signals, receiver 72 conditions (e.g., amplifies, filters, frequency scales, etc.) the signals and separates the video signals and the audio signals out of the transmission signals. The video content is provided to a video processing system 74 that prepares the video content contained in the video signals for presentation on a screen (e.g., a cathode ray tube, etc.) associated with the television receiver system 68. Signals containing the separate audio content are provided to a

demodulator stage 76 that e.g., removes the modulation applied to the audio signals at television transmission system 10. The demodulated audio signals (e.g., the SAP channel, the professional channel, the sum signal, the difference signal) are provided to a BTSC decoder 78 that appropriately decodes each signal. The SAP channel is provided a SAP channel decoder 80 and the professional channel is provided to a professional channel decoder 82. After separating the SAP channel and the professional channel, a demodulated sum signal (i.e., L + R signal) is provided to a de-emphasis unit 84 that processes the sum signal in a substantially complementary fashion in comparison to pre-emphasis unit 28 (shown in FIG. 1). Upon de-emphasizing the spectral content of the sum signal, the signal is provided to a matrix 88 for separating the left and right channel audio signals.

[0036] The difference signal (i.e., L – R) is also demodulated by demodulation stage 76 and is provided to a BTSC expander 86 included in BTSC decoder 78. BTSC expander 86 complies with the BTSC standard, and as described in detail below, conditions the difference signal. Matrix 88 receives the difference signal from BTSC expander 86 and with the sum signal, separates the right and left audio channels into independent signals (identified in FIG. 3 as "L" and "R"). By separating the signals, the individual right and left channel audio signals may be conditioned and provided to separate speakers. In this example, both the left and right audio channels are provided to an amplifier stage 90 that applies the same (or different) gains to each channel prior to providing the respective signals to a speaker 92 for broadcasting the left channel audio content and another speaker 94 for broadcasting the right channel audio content.

[0037] Referring to FIG. 4, a block diagram identifies some of the operations performed by BTSC expander 86 to condition the difference signal. In general, BTSC expander 86 performs operations that are complementary to the operations performed by BTSC compressor 32 (shown in FIG. 2). In particular, the compressed difference signal is provided to a signal path 96 for un-compressing the signal, and to two paths 98 and 100

that produce a respective control and gain signal to assist the processing of the difference signal. To initiate the processing, the compressed difference signal is provided to a band-limiting unit 102 that filters the compressed difference signal. The band-limiting unit 102 provides a signal to path 98 to produce a control signal and to path 100 to produce a gain signal. Path 100 includes a gain control bandpass filter 104, a multiplier 106 (that squares the output of the gain control bandpass filter), an integrator 108, and a square root device 110. Signal path 98 also receives the signal from band-limiting unit 102 and processes the signal with a spectral control bandpass filter 112, a squaring device 114, an integrator 116, and a square root device 118. Path 98 then provides a control signal to a spectral expansion unit 120 that performs an operation that is complementary to the operation performed by spectral compression unit 42 shown in FIG. 2. The gain signal produced by path 100 is provided to a multiplier 122 that receives an output signal from spectral expansion unit 120. Multiplier 122 provides the spectrally expanded difference signal to a fixed de-emphasis unit 124 that filters the signal in a complementary manner in comparison to filtering performed by BTSC compressor 30. In general, the term "de-emphasis" means the alteration of the select frequency components of the decoded signal in either a negative or positive sense in a complementary manner in which the original signal is encoded.

[0038] Both BTSC encoder 24 and BTSC decoder 78 include multiple filters that adjust the amplitude of audio signals as a function of frequency. In some prior art television transmission systems and reception systems, each of the filters are implemented with discrete analog components. However, with advancements in digital signal processing, some BTSC encoders and BTSC decoders may be implemented in the digital domain with one or more integrated circuits (ICs). Furthermore, multiple digital BTSC encoders and/or decoders may implemented on a single IC. For example, encoders and decoders may be incorporated into a single IC as a portion of a very large scale integration (VLSI) system.

[0039] A significant portion of the cost of an IC is directly proportional to the physical size of the chip, particularly the size of its 'die', or the active, non-packaging part of the chip. In some arrangements filtering operations performed in digital BTSC encoders and decoders may be executed using general purpose digital signal processors that are designed to execute a range of DSP functions and operations. These DSP engines tend to have relatively large die areas, and are thereby costly to use for implementing BTSC encoders and decoders. Additionally the DSP may be dedicated to executing other functions and operations. By sharing the this resource, the processing performed by the DSP may overload and interfere with the processing of the BTSC encoder and decoder functions and operations.

[0040] In some arrangements, BTSC encoders and decoders may incorporate groups of basic components to reduce cost. For example, groups of multipliers, adders, and multiplexers may be incorporated to produce the BTSC encoder and decoder functions. However, while the groups of nearly identical components may be easily fabricated, the components represent significant die area and add to the total cost of the IC. Thus, a need exists to reduce the number of duplicated circuits components used to implement a digital BTSC encoder and/or decoder.

[0041] Referring to FIG. 5, a block diagram of a configurable infinite impulse response (IIR) filter 126 is shown that is capable of performing multiple filtering operations for a digital BTSC encoder or decoder. By providing selectable filtering coefficients, configurable IIR filter 126 may be configured for various filtering operations. For example, filtering coefficients may be selected so that configurable IIR filter 126 operates as a low pass filter, a high pass filter, a band pass filter, or other type of filter known to one skilled in the art of filter design. Thus, one or a relatively small number of configurable IIR filters may be used to provide most or all of the filtering needs of a BTSC encoder or a BTSC decoder. By reducing the number of decoder and encoder filters, the implementation area of an IC chip is reduced along with the production cost of the BTSC

encoders and decoders.

[0042] To allow configurable IIR filter 126 to perform multiple types of filtering operations, the filter includes an input selector 128 that controls which input (e.g., Input 1, Input 2, ..., Input N) provides an input signal to the filter. Referring briefly to FIG. 2, some of the inputs to selector 128 may be connected to provide input signals for each of the filtering operations performed within BTSC compressor 30. For example, the input to gain control bandpass filter 60 may be connected to input 2 of selector 128. Similarly, the input to spectral control bandpass filter 52 may be connected to another input (e.g., input N) of selector 128. Then, selector 128 may control which particular filtering operation is performed by configurable IIR filter 126. For example, during one time period, one input (e.g., input 2) may be selected and configurable IIR filter 126 is configured to provide the filtering function of gain control bandpass filter 60. Then, at another time period, selector 128 is used to select another input (e.g., input N) to perform a different filtering operation. Along with selecting the other input (e.g., input N), configurable IIR filter 126 is also configured to provide the different type of filtering function, such as the filtering provided by spectral control bandpass filter 52.

[0043] In order to perform multiple filtering operations e.g., for a BTSC compressor or a BTSC expander, configurable IIR filter 126 operates at a clock speed substantially faster than the other portions of the digital compressor or expander. By operating at a faster clock speed, configurable IIR filter 10 may perform one type of filtering without causing other operations of the digital compressor or expander to be delayed. For example, by operating configurable IIR filter 126 at a substantially fast clock speed, the filter may first be configured to perform filtering for gain control bandpass filter 60 without substantially delaying the execution of the next filter configuration (e.g., filter operations for spectral control bandpass filter 52).

[0044] In this particular arrangement, configurable IIR filter 126 is implemented as a second – order IIR filter. Referring to FIG. 6, a z – domain signal flow diagram 130 is

presented for a typical second – order IIR filter. An input node 132 receives an input signal identified as X(z). The input signal is provided to a gain stage 134 that applies a filter coefficient a_0 to the input signal. In some applications the filter coefficient a_0 has a unity value. Similarly, a filter coefficient b_0 is applied to the input signal at gain stage 136. At a delay stage 138, a time delay (i.e., represented in the z – domain as z^{-1}) is applied as the input signal enters the first – order portion of the filter and filter coefficients a_1 and b_1 are applied at respective gain stages 140 and 142. A second delay (i.e., z^{-1}) is applied at delay stage 144 for producing the second – order portion of filter 130 and filter coefficients a_2 and b_2 are applied at respective gain stages 146 and 148. The filtered signal is provided to an output node 150 such that output signal Y(z) may be determined from the transfer function H(z) of the second – order filter 130, as described in the following Equation (1) :

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}$$

[0045] Each of the coefficients (i.e., b_0, a_0, b_1, a_1, b_2, and a_2) included in the transfer function may be assigned particular values to produce a desired type of filter. For example, particular values may be assigned to the coefficients to produce a low – pass filter, a high – pass filter, or a band – pass filter, etc. Thus, by providing the appropriate values for each coefficient, the type and characteristics (e.g., pass band, roll – off, etc) of the second – order filter may be configured and re-configured into another type of filter (dependent upon the application) with a different set of coefficients. While this example describes a second – order filter, in other arrangements an n^{th} – order filter may be implemented. For example, higher order (e.g. third – order, fourth – order, etc.) filters or lower order (e.g., first – order filters) may be implemented. Furthermore, for some applications, filters of the same or different orders may be cascaded to produce an n^{th} – order filter.

[0046] Referring back to FIG. 5, along with using selector 128 to select a particular input for configurable IIR filter 126, the coefficients used by the filter are selected to implement different types of filters and to provide particular filter characteristics. For

example, coefficients may be selected to implement a low – pass filter, a high – pass filter, a band – pass filter, or other similar type of filter used to encode or decode BTSC audio signals. In this example, respective selectors 152, 154, 156, 160 and 162 are used to select each coefficient for the second – order configurable filter 126. For example, selector 152 provides the a_0 coefficient of the second – order filter from a group of "n" coefficients (i.e., $a_{0(0)}$, $a_{0(1)}$, $a_{0(2)}$, …, $a_{0(n)}$) dependent upon the filter type and filter characteristics. Similarly, selectors 154 – 162 also select from respective groups of coefficient values to implement the filters. By providing these selectable coefficients values, configurable IIR filter 126 may be configured to provide filters for both encoding and decoding operations. Returning to the previous example, if selector 128 is placed in a position to select input 2 (i.e., the input for gain control bandpass filter 60), selectors 152 – 162 select the respective coefficients (e.g., $a_{0(0)}$, $b_{0(0)}$, $a_{1(0)}$, $b_{1(0)}$, $b_{2(0)}$, $a_{2(0)}$) so that IIR filter 126 is configured into the appropriate filter type with characteristics to perform as the gain control bandpass filter. Upon completing the filtering, selector 128 may then be placed in a position to provide signals present on input N to configurable IIR filter 126. Still using the previous example, input N of selector 128 may provide the input signal destined for spectral control bandpass filter 52. By selecting this input, new filter coefficients may be selected to provide the particular filter type and filter characteristics needed to perform the filtering of spectral control bandpass filter 52. To provide this filter and filter characteristics, selectors 152 – 162 may be respectively select filter coefficients (e.g., $a_{0(1)}$, $b_{0(1)}$, $a_{1(1)}$, $b_{1(1)}$, $a_{2(1)}$ and $b_{2(1)}$) associated with the filter type and characteristics of spectral control bandpass filter 52.

[0047] In this example, configurable IIR filter 126 is a second – order filter, however, some encoding and/or decoding filtering applications may call for a higher order filter. To provide higher order filters, in this example, one input of selector 128 is connected to an output 164 of IIR filter 126 to form a feed-back path. By providing the output of the IIR filter back to the input, filtered output signals may pass through the IIR filter multiple times using the same (or different) filter coefficients. Thus, signals may be passed through the second – order IIR filter 126 more than one time to produce a higher – order. In this

particular example, a conductor 166 provides a feedback path from output 164 of configurable IIR filter 126 to input 1 of selector 128.

[0048] Various techniques and components known to one skilled in the art of electronics and filter design may be used to implement selector 128 and selectors 152 - 162. For example, selector 128 may be implemented by one or more multiplexers to select among the input lines (i.e., Input 1, Input 2, ..., Input N). Multiplexers or other types digital selection devices may be implemented as one or more of selectors 152 – 162 to select appropriate filter coefficients. Various coefficient values may be used to configure IIR filter 126. For example, coefficients described in U.S. Patent 5,796,842 to Hanna, which is herein incorporated by reference, may be used by configurable IIR filter 126. In some arrangements, the filter coefficients are stored in a memory (not shown) associated with the BTSC encoder or decoder and are retrieved by selectors 152 – 162 at appropriate times. For example, the coefficients may be stored in a memory chip (e.g., random access memory (RAM), read – only memory (ROM), etc.) or another type of storage device (e.g., a hard-drive, CD-ROM, etc.) associated with the BTSC encoder or decoder. The coefficients may also be stored in various software structures such as a look – up table, or other similar structure.

[0049] Configurable second – order IIR filter 126 also includes respective adding devices 168, 170, 172, 174 and 176 are included in configurable IIR filter 126 along with multipliers 178, 180, 182, 184, 186 and 188 that apply the filter coefficients to signal values. Various techniques and/or components known to one skilled in the art of electronic circuit design and filter design may be used to implement adding devices 168 - 176 and multipliers 178 – 188 included in configurable IIR filter 126. For example, logic gates such as one or more "AND" gates may be implemented as each of the multipliers. To introduce time delays that correspond to delay stages 138 and 144 (shown in FIG. 6), registers 190 and 192 provide delays by storing and holding the digitized input signal values for an appropriate number of clock cycles during the filtering process. Additionally,

another register 194 is included configurable IIR filter 126 to initially store input signal values.

[0050] In this example, configurable IIR filter 126 is implemented with hardware components, however, in some arrangements one or more operational portions of the filter may be implemented in software. One exemplary listing of code that performs the operations of configurable IIR filter 126 is presented in appendix A. The exemplary code is provided in Verilog, which, in general, is a hardware description language that is used by electronic designers to describe and design chips and systems prior to fabrication. This code may be stored on and retrieved from a storage device (e.g., RAM, ROM, hard-drive, CD-ROM, etc.) and executed on one or more general purpose processors and/or specialized processors such as a dedicated DSP.

[0051] Referring to FIG. 7, a block diagram of BTSC compressor 30 is provided in which portions of the diagram are highlighted to illustrate functions that may be performed by a single (or multiple) configurable IIR filters such as configurable IIR filter 126. In particular, filtering performed by interpolation and fixed pre-emphasis stage 38 may be performed by configurable IIR filter 126. For example, input 1 of selector 128 may be connected to the appropriate filter input within interpolation and fixed pre-emphasis stage 38. Correspondingly, when input 1 of selector 128 is selected, filter coefficients may be retrieved from memory and used to produce to an appropriate filter type and filter characteristics. Similarly, gain control bandpass filter 60 may be assigned to input 2 of selector 128 in configurable IIR filter 126 and spectral control bandpass filter 52 may be assigned to a third input of selector 128. Band-limiting unit 46 may be assigned to a fourth input of selector 128. For each of these selectable inputs, corresponding filter coefficients are stored (e.g., in memory) and may be retrieved by selectors 152 - 162 of configurable IIR filter 126. In this example, filtering associated with four portions of BTSC compressor 30 is selectively performed by configurable IIR filter 126, however, in other arrangements, more or less filtering operations of the compressor may be performed by the configurable

IIR filter.

[0052] Referring to FIG. 8, portions of BTSC expander 86 are highlighted to identify filtering operations that may be performed by one or more configurable IIR filters such as configurable IIR filter 126. For example, filtering associated with band-limiting unit 102 may be performed by configurable IIR filter 126. In particular, input 1 of selector 128 may be assigned to band-limiting unit 102 such that when input 1 is selected, appropriate filtering coefficients are retrieved and used by IIR filter 126. Similarly, filtering associated with gain control bandpass filter 104 (assigned to a second input of selector 128), spectral control bandpass filter 112 (assigned to a third input of selector 128), and fixed de-emphasis unit 124 (assigned to a fourth input of selector 128) is consolidated onto configurable IIR filter 126.

[0053] While the previous example described using configurable IIR filter 126 with BTSC encoders and BTSC decoders, encoders and decoders that comply with television audio standards may implement the configurable IIR filter. For example, encoders and/or decoders associated with the Near Instantaneously Companded Audio Multiplex (NICAM), which is used in Europe, may incorporate one or more configurable IIR filters such as IIR filter 126. Similarly, encoders and decoders implementing the A2/Zweiton television audio standard (currently used in parts of Europe and Asia) or the Electronics Industry Association of Japan (EIA – J) standard may incorporate one or more configurable IIR filters.

[0054] While the previous example described using configurable IIR filter 126 to encode and decoder a difference signal produced from right and left audio channel, the configurable IIR filter may be used to encode and decode other audio signals. For example, configurable IIR filter 126 may be used to encode and/or decode an SAP channel, a professional channel, a sum channel, or one or more other individual or combined types of television audio channels.

[0055] A number of implementations have been described. Nevertheless, it will be understood that various modifications may be made. Accordingly, other implementations are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A television audio signal encoder, comprising:

a matrix configured to sum a left channel audio signal and a right channel audio signal to produce a sum signal, and to subtract one of the left and right audio signals from the other of the left and right signals to produce a difference signal; and

a configurable infinite impulse response digital filter configured to selectively use one or more sets of filter coefficients to filter the difference signal, wherein each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for transmission.

2. The television audio signal encoder of claim 1, wherein the configurable infinite impulse response digital filter includes a selector configured to select one of the one or more sets of filter coefficients.

3. The television audio signal encoder of claim 1, wherein the configurable infinite impulse response digital filter includes a selector configured to select an input signal from a group of input signals.

4. The television audio signal encoder of claim 3, wherein one input signal from the group of input signals includes an output signal of the configurable infinite impulse response digital filter.

5. The television audio signal encoder of claim 1, wherein the configurable infinite impulse response digital filter includes a second order infinite impulse response filter.

6. The television audio signal encoder of claim 1, wherein the configurable infinite impulse response digital filter is configured as a low pass filter.

7. The television audio signal encoder of claim 1, wherein the configurable infinite impulse response digital filter is configured as a high pass filter.

8. The television audio signal encoder of claim 1, wherein the configurable infinite impulse response digital filter is configured as a band pass filter.

9. The television audio signal encoder of claim 1, wherein the configurable infinite impulse response digital filter is configured as an emphasis filter.

10. The television audio signal encoder of claim 1, wherein selection of the one or more sets of filter coefficients is based on a rate that the television audio signal is sampled.

11. The television audio signal encoder of claim 1, wherein the sets of filter coefficients are stored in a memory.

12. The television audio signal encoder of claim 1, wherein the sets of filter coefficients are stored in a look – up table.

13. The television audio signal encoder of claim 1, wherein the television audio signal complies to the Broadcast Television System Committee (BTSC) standard.

14. The television audio signal encoder of claim 1, wherein the television audio signal complies to the Near Instantaneously Companded Audio Muliplex (NICAM) standard.

15. The television audio signal encoder of claim 1, wherein the television audio signal complies to the A2/Zweiton standard.

16. The television audio signal encoder of claim 1, wherein the television audio signal

complies to the EIA – J standard.

17. The television audio signal encoder of claim 1, wherein the configurable infinite impulse response digital filter is implemented in an integrated circuit.

18. A television audio signal decoder, comprising:

a configurable infinite impulse response digital filter configured to selectively use one or more sets of filter coefficients to filter a difference signal, wherein the difference signal is produced by subtracting one of a left channel and a right channel audio signal from the other of the left channel and right channel audio signal, each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for separating the left channel and right channel audio signals; and

a matrix configured to separate the left channel and right channel audio signals from the difference signal and a sum signal, wherein the sum signal includes the sum the left channel audio signal and the right channel audio signal.

19. The television audio signal decoder of claim 18, wherein the configurable infinite impulse response digital filter includes a selector configured to select one of the one or more sets of filter coefficients.

20. The television audio signal decoder of claim 18, wherein the configurable infinite impulse response digital filter includes a selector configured to select an input signal from a group of input signals.

21. The television audio signal decoder of claim 20, wherein one input signal from the group of input signals includes an output signal of the configurable infinite impulse response digital filter.

22. The television audio signal decoder of claim 18, wherein the configurable infinite impulse response digital filter includes a second order infinite impulse response filter.

23. The television audio signal decoder of claim 18, wherein the configurable infinite impulse response digital filter is configured as a low pass filter.

24. The television audio signal decoder of claim 18, wherein the configurable infinite impulse response digital filter is configured as a high pass filter.

25. The television audio signal decoder of claim 18, wherein the configurable infinite impulse response digital filter is configured as a band pass filter.

26. The television audio signal decoder of claim 18, wherein the configurable infinite impulse response digital filter is configured as an emphasis filter.

27. The television audio signal decoder of claim 18, wherein selection of the one or more sets of filter coefficients is based on a rate that the television audio signal is sampled.

28. The television audio signal decoder of claim 18, wherein the sets of filter coefficients are stored in a memory.

29. The television audio signal decoder of claim 18, wherein the sets of filter coefficients are stored in a look – up table.

30. The television audio signal encoder of claim 18, wherein the television audio signal complies to the Broadcast Television System Committee (BTSC) standard.

31. The television audio signal encoder of claim 18, wherein the television audio signal

complies to the Near Instantaneously Companded Audio Muliplex (NICAM) standard.

32. The television audio signal encoder of claim 18, wherein the television audio signal complies to the A2/Zweiton standard.

33. The television audio signal encoder of claim 18, wherein the television audio signal complies to the EIA – J standard.

34. The television audio signal encoder of claim 18, wherein the configurable infinite impulse response digital filter is implemented in an integrated circuit.

35. A digital BTSC signal encoder for encoding digital left and right channel audio signals so that the encoded left and right channel audio signals can be subsequently decoded so as to reproduce the digital left and right channel audio signals with little or no distortion of the signal content of the digital left and right channel audio signals, the encoder comprising:

a matrix configured to sum the left channel audio signal and the right channel audio signal to produce a sum signal, and to subtract one of the left and right audio signals from the other of the left and right signals to produce a difference signal; and

a configurable infinite impulse response digital filter configured to selectively use one or more sets of filter coefficients to filter the difference signal, wherein each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for transmission and comply with the BTSC standard.

36. The digital BTSC signal encoder of claim 35, wherein the configurable infinite

impulse response digital filter includes a selector configured to select one of the one or more sets of filter coefficients.

37. The digital BTSC signal encoder of claim 35, wherein the configurable infinite impulse response digital filter includes a selector configured to select an input signal from a group of input signals.

38. The digital BTSC signal encoder of claim 37, wherein one input signal from the group of input signals includes an output signal of the configurable infinite impulse response digital filter.

39. The digital BTSC signal encoder of claim 35, wherein the configurable infinite impulse response digital filter includes a second order infinite impulse response filter.

40. The digital BTSC signal encoder of claim 35, wherein the configurable infinite impulse response digital filter is configured as a low pass filter.

41. The digital BTSC signal encoder of claim 35, wherein the configurable infinite impulse response digital filter is configured as a high pass filter.

42. The digital BTSC signal encoder of claim 35, wherein the configurable infinite impulse response digital filter is configured as a band pass filter.

43. The digital BTSC signal encoder of claim 35, wherein the configurable infinite impulse response digital filter is configured as an emphasis filter.

44. The digital BTSC signal encoder of claim 35, wherein selection of the one or more sets of filter coefficients is based on a rate that the television audio signal is sampled.

45. The digital BTSC signal encoder of claim 35, wherein the sets of filter coefficients are stored in a memory.

46. The digital BTSC signal encoder of claim 35, wherein the sets of filter coefficients are stored in a look – up table.

47. A digital BTSC signal decoder for decoding digital left and right channel audio signals with little or no distortion of the signal content of the digital left and right channel audio signals, the decoder comprising:

a configurable infinite impulse response digital filter configured to selectively use one or more sets of filter coefficients to filter a difference signal that complies with the BTSC standard, wherein the difference signal is produced by subtracting one of a left channel and a right channel audio signal from the other of the left channel and right channel audio signal, each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for separating the left channel and right channel audio signals; and

a matrix configured to separate the left channel and right channel audio signals from the difference signal and a sum signal, wherein the sum signal includes the sum the left channel audio signal and the right channel audio signal.

48. The digital BTSC signal decoder of claim 47, wherein the configurable infinite impulse response digital filter includes a selector configured to select one of the one or more sets of filter coefficients.

49. The digital BTSC signal decoder of claim 47, wherein the configurable infinite impulse response digital filter includes a selector configured to select an input signal from

a group of input signals.

50. The digital BTSC signal decoder of claim 49, wherein one input signal from the group of input signals includes an output signal of the configurable infinite impulse response digital filter.

51. The digital BTSC signal decoder of claim 47, wherein the configurable infinite impulse response digital filter includes a second order infinite impulse response filter.

52. The digital BTSC signal decoder of claim 47, wherein the configurable infinite impulse response digital filter is configured as a low pass filter.

53. The digital BTSC signal decoder of claim 47, wherein the configurable infinite impulse response digital filter is configured as a high pass filter.

54. The digital BTSC signal decoder of claim 47, wherein the configurable infinite impulse response digital filter is configured as a band pass filter.

55. The digital BTSC signal decoder of claim 47, wherein the configurable infinite impulse response digital filter is configured as an emphasis filter.

56. The digital BTSC signal decoder of claim 47, wherein selection of the one or more sets of filter coefficients is based on a rate that the television audio signal is sampled.

57. The digital BTSC signal decoder of claim 47, wherein the sets of filter coefficients are stored in a memory.

58. The digital BTSC signal decoder of claim 47, wherein the sets of filter coefficients are

stored in a look – up table.

59. A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

sum a left channel audio signal and a right channel audio signal to produce a sum signal, and to subtract one of the left and right audio signals from the other of the left and right signals to produce a difference signal; and

select one or more sets of filter coefficients to filter the difference signal with a configurable infinite impulse response digital filter, wherein each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for transmission.

60. The computer program product of claim 59 further comprising instructions to:

to select an input signal from a group of input signals.

61. A computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

select one or more sets of filter coefficients to filter a difference signal with an infinite impulse response digital filter, wherein the difference signal is produced by subtracting one of a left channel and a right channel audio signal from the other of the left channel and right channel audio signal, each selectable set of filter coefficients is associated with a unique filtering application to prepare the difference signal for separating the left channel and right channel audio signals; and

separate the left channel and right channel audio signals from the difference signal and a sum signal, wherein the sum signal includes the sum the left channel

audio signal and the right channel audio signal.

62. The computer program product of claim 61 further comprising instructions to:

to select an input signal from a group of input signals.

63. A television audio signal encoder, comprising:

an input stage configured to receive a secondary audio programming signal; and

a configurable infinite impulse response digital filter configured to selectively use one or more sets of filter coefficients to filter the secondary audio programming signal, wherein each selectable set of filter coefficients is associated with a unique filtering application to prepare the secondary audio programming signal for transmission.

64. The television audio signal encoder of claim 63, wherein the configurable infinite impulse response digital filter includes a selector configured to select one of the one or more sets of filter coefficients.

65. The television audio signal encoder of claim 63, wherein the configurable infinite impulse response digital filter includes a selector configured to select an input signal from a group of input signals.

66. The television audio signal encoder of claim 65, wherein one input signal from the group of input signals includes an output signal of the configurable infinite impulse response digital filter.

67. The television audio signal encoder of claim 63, wherein the configurable infinite impulse response digital filter includes a second order infinite impulse response filter.

68. A television audio signal decoder, comprising:

a configurable infinite impulse response digital filter configured to selectively use one or more sets of filter coefficients to filter a secondary audio programming signal, each selectable set of filter coefficients is associated with a unique filtering application to prepare the secondary audio programming signal for a television receiver system.

69. The television audio signal decoder of claim 68, wherein the configurable infinite impulse response digital filter includes a selector configured to select one of the one or more sets of filter coefficients.

70. The television audio signal decoder of claim 68, wherein the configurable infinite impulse response digital filter includes a selector configured to select an input signal from a group of input signals.

71. The television audio signal decoder of claim 70, wherein one input signal from the group of input signals includes an output signal of the configurable infinite impulse response digital filter.

72. The television audio signal decoder of claim 68, wherein the configurable infinite impulse response digital filter includes a second order infinite impulse response filter.

APPENDIX A

Exhibit 1

```
/*****************************************************
(These comments are generalized for any of the filt modules.)

This module is the cascaded direct-form II implementation of
one or more discrete-time filters.  It is actually a single
second-order section that can be 'recycled' up to eight times.
It can implement a single 16th-order filter, eight 2nd-order
filters or any combination as long as the total number of 2nd-order
sections does not exceed 8.  The verilog code is automatically
generated by a program which allows the filters and their coefficients
to be input.  Refer to BTSC Block Diagrams.ppt for the block diagram
of the general form of this module.

This module is initiated by the enable signal 'khz192'.  That resets

the 'section' bus to sec1 which begins the cycle at the first section.
The 'section' bus is used throughout the module to control muxes which
allow the data from the specified section to be used in the calculations.

'Section' first selects the appropriate input to be used for 'indata',
which is the input to that section.  'Indata' can come either from an
outside input (when a new filter begins) or from the output of the
previous section(acc2), when a 4th or higher order filter is computing

a section other than its first section.

'Section' will also select the appropriate a1, a2, b0, b1,and b2 coefficients
to be used for the multiplications of the d0, d1 and d2 registers. The
d registers are long shift registers containing the data for each
of the sections in sequential order.  For example, at the time a new cycle
is initiated, the data in d# will have the section 1 data in its least
significant bits, followed by section 2 in its next most significant
bits, etc.  For each section the bits are arranged in order such that
the lsb of the data is located in a less significant bit than the msb.

So, as the shift registers shift down, more significant bits are multiplied
by the a and b coefficients.  Each of those products is summed and
accumulated in the acc1 and acc2 registers.  Each time a sum of products
is added to each accumulator, the previous value of the accumulator is
divided by 2 to give the proper weighting to each multiplication.

The primary purpose of the 'lastcnt' signal is to handle multiplication
by a negative number.  'Lastcnt' is high when the sign bit is being
multiplied.  'Lastcnt' will invert the bits of 'asum1' and 'bsum2' to
give a 1's complement result in the accumulator.  For the accumulator
associated with acc2 a 1 is added simultaneously with this bit-inversion
to give a 2's complement result.  An approximation is used on the side
associated with acc1 where 1s are added in every addition except for the
one when 'lastcnt' is high.  The result is that 0.11111...(binary) is added
instead of 1.  The approximation is very close and this approach saves some
resources by using the same input to the adder for adding the value
'indata' and the 1s.

There is a dout# register for each of the distinct filters that this
module implements.  The data in acc2 is written to the corresponding
dout register when that filter's cycle is complete.  'Section' also
handles that function.

*****************************************************/

// Generated by SOSFilterGenerator.m on 18-Feb-2004 09:21:24
//
// Delay Register Width = 32

// ***************************  Filter 1 Diff Gain Ctrl Bandpass  ***************************
// This filter is in Q17 format. (Q17 is required.)
//
// - - - - - - - - - - - - - - - (192 kHz Stereo)  - - - - - - - - - - - - - -
// Max Delay Register Value = 13066.680  ------------>  20.247% headroom
//
//
//       b0              b1              b2              a0              a1              a2
//-------------------------------------------------------------------------------------------
//   3.3052890e-002  0.0000000e+000 -3.3052890e-002  1.0000000e+000 -1.9327087e+000  9.3278529e-001
//
// Magnitudes are relative to the system input, not necessarily the filter input.
// Section          Del. max                    Outmax
// -------          --------                    ------
// 1           13066.6798990645000            1.8655542250264
//
//
// - - - - - - - - - - - - - - - (176.4 kHz Stereo)  - - - - - - - - - - - - - -
// Max Delay Register Value = 11062.425  ------------>  32.480% headroom
//
//
//       b0              b1              b2              a0              a1              a2
//-------------------------------------------------------------------------------------------
//   3.5869202e-002  0.0000000e+000 -3.5869202e-002  1.0000000e+000 -1.9269677e+000  9.2705818e-001
//
```

```
// Magnitudes are relative to the system input, not necessarily the filter input.
// Section          Del. max                  Outmax
// -------          --------                  ------
// 1          11062.4247708884870           1.8655578679158
//
//
// - - - - - - - - - - - - - - (192 kHz SAP)  - - - - - - - - - - - - - -
// Max Delay Register Value = 13066.680  ------------>  20.247% headroom
//
//
//      b0             b1             b2             a0             a1             a2
//-------------------------------------------------------------------------------------------
//   3.3052890e-002  0.0000000e+000 -3.3052890e-002  1.0000000e+000 -1.9327087e+000  9.3278529e-001
//
// Magnitudes are relative to the system input, not necessarily the filter input.
// Section          Del. max                  Outmax
// -------          --------                  ------
// 1          13066.6798990645000           1.8655542250264
//
//
// - - - - - - - - - - - - - - (176.4 kHz SAP)  - - - - - - - - - - - - - -
// Max Delay Register Value = 11062.425  ------------>  32.480% headroom
//
//
//      b0             b1             b2             a0             a1             a2
//-------------------------------------------------------------------------------------------
//   3.5869202e-002  0.0000000e+000 -3.5869202e-002  1.0000000e+000 -1.9269677e+000  9.2705818e-001
//
// Magnitudes are relative to the system input, not necessarily the filter input.
// Section          Del. max                  Outmax
// -------          --------                  ------
// 1          11062.4247708884870           1.8655578679158
//
// ***************************  Filter 2 Diff Lowpass  ***************************
// This filter is in Q25 format. (Q18 is required.)
//
// - - - - - - - - - - - - - - (192 kHz Stereo)  - - - - - - - - - - - - - -
// Max Delay Register Value = 31.984  ------------>  50.025% headroom
//
//
//      b0             b1             b2             a0             a1             a2
//-------------------------------------------------------------------------------------------
//   5.2715876e-002  2.0691034e-002  5.2715876e-002  1.0000000e+000 -1.5131160e+000  5.8400921e-001
//   1.7907148e-001 -2.3574553e-001  1.7907148e-001  1.0000000e+000 -1.5854796e+000  7.0937033e-001
//   3.0401514e-001 -4.9151080e-001  3.0401514e-001  1.0000000e+000 -1.6621327e+000  8.4198754e-001
//   3.5735700e-001 -6.0794041e-001  3.5735700e-001  1.0000000e+000 -1.7107429e+000  9.2558392e-001
//   2.6136244e-001 -4.5235123e-001  2.6136243e-001  1.0000000e+000 -1.7366273e+000  9.6885152e-001
//   5.3830645e+000 -9.3702736e+000  5.3830645e+000  1.0000000e+000 -1.7519173e+000  9.9157326e-001
//
// Magnitudes are relative to the system input, not necessarily the filter input.
// Section          Del. max                  Outmax
// -------          --------                  ------
// 1          28.3715156629407          3.5776901313243
// 2          31.9840159840160          3.8305392851226
// 3          31.9840159840161          3.1210477888606
// 4          31.9840159840161          2.0639824177149
// 5          31.9840159840161          0.8396791296564
// 6          31.9840159840157          7.7860720843173
//
//
// - - - - - - - - - - - - - - (176.4 kHz Stereo)  - - - - - - - - - - - - - -
// Max Delay Register Value = 31.984  ------------>  50.025% headroom
//
//
//      b0             b1             b2             a0             a1             a2
//-------------------------------------------------------------------------------------------
//   6.7152569e-002  3.7570123e-002  6.7152569e-002  1.0000000e+000 -1.4728189e+000  5.5557235e-001
//   1.8164684e-001 -2.1982620e-001  1.8164684e-001  1.0000000e+000 -1.5434407e+000  6.8851717e-001
//   3.0315457e-001 -4.7013161e-001  3.0315457e-001  1.0000000e+000 -1.6187569e+000  8.3007841e-001
//   3.5875746e-001 -5.9137598e-001  3.5875746e-001  1.0000000e+000 -1.6668321e+000  9.1980280e-001
//   2.6119117e-001 -4.3950708e-001  2.6119117e-001  1.0000000e+000 -1.6926423e+000  9.6639480e-001
//   4.6230336e+000 -7.8327350e+000  4.6230336e+000  1.0000000e+000 -1.7081951e+000  9.9090135e-001
//
// Magnitudes are relative to the system input, not necessarily the filter input.
// Section          Del. max                  Outmax
// -------          --------                  ------
// 1          24.3079463328329          4.1771147459416
// 2          31.9840159840160          4.4855401597618
// 3          31.9840159840160          3.6514564876954
// 4          31.9840159840160          2.4096818625693
// 5          31.9840159840160          0.9803587530679
// 6          31.9840159840163          7.8035183748296
//
//
// - - - - - - - - - - - - - - (192 kHz SAP)  - - - - - - - - - - - - - -
// Max Delay Register Value = 63.968  ------------>  0.050% headroom
//
//
//      b0             b1             b2             a0             a1             a2
//-------------------------------------------------------------------------------------------
//   3.5592430e-002 -1.5278522e-002  3.5592430e-002  1.0000000e+000 -1.6681586e+000  7.0166935e-001
//   1.7291208e-001 -2.8898617e-001  1.7291208e-001  1.0000000e+000 -1.7369812e+000  7.9467313e-001
//   3.0167936e-001 -5.5024915e-001  3.0167936e-001  1.0000000e+000 -1.8076638e+000  8.9011358e-001
//   3.5737308e-001 -6.6631149e-001  3.5737309e-001  1.0000000e+000 -1.8511403e+000  9.4867213e-001
//   2.6223393e-001 -4.9257885e-001  2.6223391e-001  1.0000000e+000 -1.8738553e+000  9.7876206e-001
```

```
//   5.7674700e+000 -1.0860498e+001  5.7674702e+000  1.0000000e+000 -1.8862768e+000  9.9419075e-001
//
// Magnitudes are relative to the system input, not necessarily the filter input.
// Section          Del. max                  Outmax
// -------          --------                  ------
// 1           60.0034268505309           3.3542136731491
// 2           63.9680319680321           3.5670279294006
// 3           63.9680319680321           2.8857408434409
// 4           63.9680319680321           1.9005959012310
// 5           63.9680319680320           0.7766753946363
// 6           63.9680319680336           7.7499820925803
//
//
// - - - - - - - - - - - - - - (176.4 kHz SAP)  - - - - - - - - - - - - - -
// Max Delay Register Value = 63.968  ------------>  0.050% headroom
//
//
//       b0             b1             b2             a0             a1             a2
//-----------------------------------------------------------------------------------------------
//   4.4204320e-002 -1.1568688e-002  4.4204320e-002  1.0000000e+000 -1.6403229e+000  6.7956503e-001
//   1.7358197e-001 -2.8037672e-001  1.7358197e-001  1.0000000e+000 -1.7110303e+000  7.7879254e-001
//   3.0196683e-001 -5.4126478e-001  3.0196683e-001  1.0000000e+000 -1.7840699e+000  8.8122022e-001
//   3.5775058e-001 -6.5823409e-001  3.5775056e-001  1.0000000e+000 -1.8293921e+000  9.4453343e-001
//   2.6147895e-001 -4.8537764e-001  2.6147899e-001  1.0000000e+000 -1.8528840e+000  9.7681746e-001
//   4.9110551e+000 -9.1432135e+000  4.9110546e+000  1.0000000e+000 -1.8661663e+000  9.9377949e-001
//
// Magnitudes are relative to the system input, not necessarily the filter input.
// Section          Del. max                  Outmax
// -------          --------                  ------
// 1           51.2422098900253           3.9369918486068
// 2           63.9680319680320           4.1915804156462
// 3           63.9680319680319           3.3954719109638
// 4           63.9680319680317           2.2445117940875
// 5           63.9680319680315           0.9126165355909
// 6           63.9680319680318           7.7522411990662
//
module decfilt1 (i1Clk,
                 i1nReset,
                 i1DRegClear,
                 i1Start,
                 i2CoefSelect,
                 i18DataIn1,
                 or19DataOut1,
                 i27DataIn2,
                 or29DataOut2);

input           i1Clk;
input           i1nReset;
input           i1DRegClear;
input           i1Start;
input   [1:0]  i2CoefSelect;

input   [17:0]  i18DataIn1;
output  [18:0]  or19DataOut1;

input   [26:0]  i27DataIn2;
output  [28:0]  or29DataOut2;

reg     [31:0]  r32D0MSBs;
reg     [191:0] r192D0;
reg     [223:0] r224D1;
reg     [223:0] r224D2;

reg     [28:0]  r29DataInReg;
wire    [33:0]  w34IMux1;
reg     [33:0]  r34GA1;
reg     [33:0]  r34GA2;
wire    [33:0]  w34ASum1;
wire    [33:0]  w34ASum1n;
reg     [33:0]  r34Acc1;

reg     [36:0]  r37GB0;
reg     [36:0]  r37GB1;
reg     [36:0]  r37GB2;
wire    [36:0]  w37BSum1;
wire    [36:0]  w37BSum2;
wire    [36:0]  w37BSum2n;
reg     [36:0]  r37Acc2;
reg     [18:0]  or19DataOut1;
reg     [28:0]  or29DataOut2;

reg     [5:0]  r6SOSCnt;
reg            r1LastCnt;
reg            r1FirstCnt;
reg            r1FiltEn;
reg            r1FiltEnDly;
reg     [2:0]  r3Section;

parameter
    SEC1 = 3'b000,
    SEC2 = 3'b001,
    SEC3 = 3'b010,
    SEC4 = 3'b011,
    SEC5 = 3'b100,
    SEC6 = 3'b101,
```

```
    SEC7 = 3'b110,
    SEC8 = 3'b111;

always @(posedge i1Clk or negedge i1nReset)
if (~i1nReset) begin
    r6SOSCnt    <= 32;
    r3Section   <= SEC1;
    r1LastCnt   <= 0;
    r1FirstCnt  <= 1;
    r1FiltEn    <= 0;
end else begin
    if (i1Start) begin
        r6SOSCnt    <= 32;
        r3Section   <= SEC1;
        r1LastCnt   <= 0;
        r1FirstCnt  <= 1;
        r1FiltEn    <= 1;
    end else begin
        r1LastCnt   <= (r6SOSCnt == 1);
        r1FirstCnt  <= r1LastCnt;
        r3Section   <= r1LastCnt ? r3Section + 1 : r3Section;
        r1FiltEn    <= (r1LastCnt && (r3Section == SEC7)) ? 0 : r1FiltEn;
        r1FiltEnDly <= r1FiltEn;
        r6SOSCnt    <= (r6SOSCnt == 0) ? 32 : r6SOSCnt - 1;
    end
end

always @(r192D0[0] or r3Section)
begin
    if (r192D0[0] == 1'b0) begin
        r34GA1  = 0;
        r37GB0  = 0;
    end else begin
        case (i2CoefSelect)

            0: //192 kHz Stereo
            case (r3Section)
                SEC1 : begin r34GA1 = 34'h0F762FFD7;     // 1.932709e+000 in Q31
                             r37GB0 = 37'h00043B13BC; end // 3.305289e-002 in Q31
                SEC2 : begin r34GA1 = 34'h0C1ADC8D3;     // 1.513116e+000 in Q31
                             r37GB0 = 37'h0006BF54D2; end // 5.271588e-002 in Q31
                SEC3 : begin r34GA1 = 34'h0CAF0FF18;     // 1.585480e+000 in Q31
                             r37GB0 = 37'h0016EBD073; end // 1.790715e-001 in Q31
                SEC4 : begin r34GA1 = 34'h0D4C0C369;     // 1.662133e+000 in Q31
                             r37GB0 = 37'h0026E9F7DF; end // 3.040151e-001 in Q31
                SEC5 : begin r34GA1 = 34'h0DAF99F49;     // 1.710743e+000 in Q31
                             r37GB0 = 37'h002DBDDFC9; end // 3.573570e-001 in Q31
                SEC6 : begin r34GA1 = 34'h0DE49CDAD;     // 1.736627e+000 in Q31
                             r37GB0 = 37'h0021745304; end // 2.613624e-001 in Q31
                SEC7 : begin r34GA1 = 34'h0E03ED378;     // 1.751917e+000 in Q31

                             r37GB0 = 37'h02B10841F6; end // 5.383065e+000 in Q31
                default: begin r34GA1 = 0; r37GB0 = 0; end
            endcase

            1: //176.4 kHz Stereo
            case (r3Section)
                SEC1 : begin r34GA1 = 34'h0F6A6E0FA;     // 1.926968e+000 in Q31
                             r37GB0 = 37'h0004975CAC; end // 3.586920e-002 in Q31
                SEC2 : begin r34GA1 = 34'h0BC855431;     // 1.472819e+000 in Q31
                             r37GB0 = 37'h0008987494; end // 6.715257e-002 in Q31
                SEC3 : begin r34GA1 = 34'h0C58F76D4;     // 1.543441e+000 in Q31
                             r37GB0 = 37'h0017403424; end // 1.816468e-001 in Q31
                SEC4 : begin r34GA1 = 34'h0CF336CF8;     // 1.618757e+000 in Q31
                             r37GB0 = 37'h0026CDC4E1; end // 3.031546e-001 in Q31
                SEC5 : begin r34GA1 = 34'h0D55AC15F;     // 1.666832e+000 in Q31
                             r37GB0 = 37'h002DEBC3AC; end // 3.587575e-001 in Q31
                SEC6 : begin r34GA1 = 34'h0D8A88105;     // 1.692642e+000 in Q31
                             r37GB0 = 37'h00216EB65B; end // 2.611912e-001 in Q31
                SEC7 : begin r34GA1 = 34'h0DAA6232E;     // 1.708195e+000 in Q31
                             r37GB0 = 37'h024FBF903E; end // 4.623034e+000 in Q31
                default: begin r34GA1 = 0; r37GB0 = 0; end
            endcase

            2: //192 kHz SAP
            case (r3Section)
                SEC1 : begin r34GA1 = 34'h0F762FFD7;     // 1.932709e+000 in Q31
                             r37GB0 = 37'h00043B13BC; end // 3.305289e-002 in Q31
                SEC2 : begin r34GA1 = 34'h0D58638B3;     // 1.668159e+000 in Q31
                             r37GB0 = 37'h00048E4AF2; end // 3.559243e-002 in Q31
                SEC3 : begin r34GA1 = 34'h0DE556600;     // 1.736981e+000 in Q31
                             r37GB0 = 37'h001621FBAF; end // 1.729121e-001 in Q31
                SEC4 : begin r34GA1 = 34'h0E7618705;     // 1.807664e+000 in Q31
                             r37GB0 = 37'h00269D6DDD; end // 3.016794e-001 in Q31
                SEC5 : begin r34GA1 = 34'h0ECF22A52;     // 1.851140e+000 in Q31
                             r37GB0 = 37'h002DBE66AD; end // 3.573731e-001 in Q31
                SEC6 : begin r34GA1 = 34'h0EFDA7DAD;     // 1.873855e+000 in Q31
                             r37GB0 = 37'h002190E1A2; end // 2.622339e-001 in Q31
                SEC7 : begin r34GA1 = 34'h0F1718472;     // 1.886277e+000 in Q31
                             r37GB0 = 37'h02E23C74EB; end // 5.767470e+000 in Q31
                default: begin r34GA1 = 0; r37GB0 = 0; end
            endcase

            3: //176.4 kHz SAP
            case (r3Section)
```

```
                SEC1 : begin r34GA1 = 34'h0F6A6E0FA;     // 1.926968e+000 in Q31
                       r37GB0 = 37'h0004975CAC; end // 3.586920e-002 in Q31
                SEC2 : begin r34GA1 = 34'h0D1F619CE;     // 1.640323e+000 in Q31
                       r37GB0 = 37'h0005A87CB7; end // 4.420432e-002 in Q31
                SEC3 : begin r34GA1 = 34'h0DB030A3B;     // 1.711030e+000 in Q31
                       r37GB0 = 37'h001637EF23; end // 1.735820e-001 in Q31
                SEC4 : begin r34GA1 = 34'h0E45C66F0;     // 1.784070e+000 in Q31
                       r37GB0 = 37'h0026A6D961; end // 3.019668e-001 in Q31
                SEC5 : begin r34GA1 = 34'h0EA298531;     // 1.829392e+000 in Q31
                       r37GB0 = 37'h002DCAC55F; end // 3.577506e-001 in Q31
                SEC6 : begin r34GA1 = 34'h0ED2B4D38;     // 1.852884e+000 in Q31
                       r37GB0 = 37'h0021782461; end // 2.614789e-001 in Q31
                SEC7 : begin r34GA1 = 34'h0EEDE89D7;     // 1.866166e+000 in Q31
                       r37GB0 = 37'h02749D73CC; end // 4.911055e+000 in Q31
                default: begin r34GA1 = 0; r37GB0 = 0; end
            endcase
        endcase
    end
end


always @(r224D1[0] or r3Section)
begin
    if (r224D1[0] == 1'b0) begin
        r34GA2  = 0;
        r37GB1  = 0;
    end else begin
        case (i2CoefSelect)

            0: //192 kHz Stereo
            case (r3Section)
                SEC1 : begin r34GA2 = 34'h3889A7DDB;     // -9.327853e-001 in Q31
                       r37GB1 = 37'h0000000000; end // 0 in Q31
                SEC2 : begin r34GA2 = 34'h3B53F2FA4;     // -5.840092e-001 in Q31
                       r37GB1 = 37'h0002A600F8; end // 2.069103e-002 in Q31
                SEC3 : begin r34GA2 = 34'h3A5335A60;     // -7.093703e-001 in Q31
                       r37GB1 = 37'h1FE1D31721; end // -2.357455e-001 in Q31
                SEC4 : begin r34GA2 = 34'h39439C091;     // -8.419875e-001 in Q31
                       r37GB1 = 37'h1FC1162C88; end // -4.915108e-001 in Q31
                SEC5 : begin r34GA2 = 34'h389867756;     // -9.255839e-001 in Q31
                       r37GB1 = 37'h1FB22F0237; end // -6.079404e-001 in Q31
                SEC6 : begin r34GA2 = 34'h383FCAC66;     // -9.688515e-001 in Q31
                       r37GB1 = 37'h1FC6195ADF; end // -4.523512e-001 in Q31
                SEC7 : begin r34GA2 = 34'h3811420A7;     // -9.915733e-001 in Q31
                       r37GB1 = 37'h1B509AE053; end // -9.370274e+000 in Q31
                default: begin r34GA2 = 0; r37GB1 = 0; end
            endcase

            1: //176.4 kHz Stereo
            case (r3Section)
                SEC1 : begin r34GA2 = 34'h389562859;     // -9.270582e-001 in Q31
                       r37GB1 = 37'h0000000000; end // 0 in Q31
                SEC2 : begin r34GA2 = 34'h3B8E3014E;     // -5.555724e-001 in Q31
                       r37GB1 = 37'h0004CF190A; end // 3.757012e-002 in Q31
                SEC3 : begin r34GA2 = 34'h3A7DEABS7;     // -6.885172e-001 in Q31
                       r37GB1 = 37'h1FE3DCBC30; end // -2.198262e-001 in Q31
                SEC4 : begin r34GA2 = 34'h395BFFDA5;     // -8.300784e-001 in Q31
                       r37GB1 = 37'h1FC3D2BA38; end // -4.701316e-001 in Q31
                SEC5 : begin r34GA2 = 34'h38A43E6DC;     // -9.198028e-001 in Q31
                       r37GB1 = 37'h1FB44DCABF; end // -5.913760e-001 in Q31
                SEC6 : begin r34GA2 = 34'h3844D2CDF;     // -9.663948e-001 in Q31
                       r37GB1 = 37'h1FC7BE3B63; end // -4.395071e-001 in Q31
                SEC7 : begin r34GA2 = 34'h3812A24F8;     // -9.909014e-001 in Q31
                       r37GB1 = 37'h1C1568F0B5; end // -7.832735e+000 in Q31
                default: begin r34GA2 = 0; r37GB1 = 0; end
            endcase

            2: //192 kHz SAP
            case (r3Section)
                SEC1 : begin r34GA2 = 34'h3889A7DDB;     // -9.327853e-001 in Q31
                       r37GB1 = 37'h0000000000; end // 0 in Q31
                SEC2 : begin r34GA2 = 34'h3A62FB2DC;     // -7.016694e-001 in Q31
                       r37GB1 = 37'h1FFE0B5A78; end // -1.527852e-002 in Q31
                SEC3 : begin r34GA2 = 34'h39A482696;     // -7.946731e-001 in Q31
                       r37GB1 = 37'h1FDB028052; end // -2.889862e-001 in Q31
                SEC4 : begin r34GA2 = 34'h38E10C220;     // -8.901136e-001 in Q31
                       r37GB1 = 37'h1FB9916F98; end // -5.502491e-001 in Q31
                SEC5 : begin r34GA2 = 34'h38691E96A;     // -9.486721e-001 in Q31
                       r37GB1 = 37'h1FAAB64E14; end // -6.663115e-001 in Q31
                SEC6 : begin r34GA2 = 34'h3B2B7ECB7;     // -9.787621e-001 in Q31
                       r37GB1 = 37'h1FC0F32D16; end // -4.925789e-001 in Q31
                SEC7 : begin r34GA2 = 34'h380BE5B90;     // -9.941907e-001 in Q31
                       r37GB1 = 37'h1A91DB35BC; end // -1.086050e+001 in Q31
                default: begin r34GA2 = 0; r37GB1 = 0; end
            endcase

            3: //176.4 kHz SAP
            case (r3Section)
                SEC1 : begin r34GA2 = 34'h389562859;     // -9.270582e-001 in Q31
                       r37GB1 = 37'h0000000000; end // 0 in Q31
                SEC2 : begin r34GA2 = 34'h3A904035A;     // -6.795650e-001 in Q31
                       r37GB1 = 37'h1FFE84EAD0; end // -1.156869e-002 in Q31
                SEC3 : begin r34GA2 = 34'h39C5086AF;     // -7.787925e-001 in Q31
                       r37GB1 = 37'h1FDC1C9D93; end // -2.803767e-001 in Q31
                SEC4 : begin r34GA2 = 34'h38F342D0D;     // -8.812202e-001 in Q31
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                        r37GB1 = 37'h1FBAB7D5F1; end // -5.412648e-001 in Q31
                SEC5 : begin r34GA2 = 34'h387198752;     // -9.445334e-001 in Q31
                        r37GB1 = 37'h1FABBEFC44; end // -6.582341e-001 in Q31
                SEC6 : begin r34GA2 = 34'h382F7A534;     // -9.768175e-001 in Q31
                        r37GB1 = 37'h1FC1DF2549; end // -4.853776e-001 in Q31
                SEC7 : begin r34GA2 = 34'h380CBD572;     // -9.937795e-001 in Q31
                        r37GB1 = 37'h1B6DAB2E50; end // -9.143213e+000 in Q31
                default: begin r34GA2 = 0; r37GB1 = 0; end
            endcase
        endcase
    end
end

always @(r224D2[0] or r3Section)
begin
    if (r224D2[0] == 1'b0)
        r37GB2  = 0;
    else begin
        case (i2CoefSelect)

            0: //192 kHz Stereo
            case (r3Section)
                SEC1 : r37GB2 = 37'h1FFBC4EC44; // -3.305289e-002 in Q31
                SEC2 : r37GB2 = 37'h0006BF64D2; // 5.271588e-002 in Q31
                SEC3 : r37GB2 = 37'h0016EBD073; // 1.790715e-001 in Q31
                SEC4 : r37GB2 = 37'h0026E9F7DF; // 3.040151e-001 in Q31
                SEC5 : r37GB2 = 37'h002DBDDFCB; // 3.573570e-001 in Q31
                SEC6 : r37GB2 = 37'h0021745300; // 2.613624e-001 in Q31
                SEC7 : r37GB2 = 37'h02B1084239; // 5.383065e+000 in Q31
                default: r37GB2 = 0;
            endcase

            1: //176.4 kHz Stereo
            case (r3Section)
                SEC1 : r37GB2 = 37'h1FFB68A354; // -3.586920e-002 in Q31
                SEC2 : r37GB2 = 37'h0008987494; // 6.715257e-002 in Q31
                SEC3 : r37GB2 = 37'h0017403424; // 1.816468e-001 in Q31
                SEC4 : r37GB2 = 37'h0026CDC4E1; // 3.031546e-001 in Q31
                SEC5 : r37GB2 = 37'h002DEBC3AC; // 3.587575e-001 in Q31
                SEC6 : r37GB2 = 37'h00216EB65B; // 2.611912e-001 in Q31
                SEC7 : r37GB2 = 37'h024FBF903B; // 4.623034e+000 in Q31
                default: r37GB2 = 0;
            endcase

            2: //192 kHz SAP
            case (r3Section)
                SEC1 : r37GB2 = 37'h1FFBC4EC44; // -3.305289e-002 in Q31
                SEC2 : r37GB2 = 37'h00048E4AF2; // 3.559243e-002 in Q31
                SEC3 : r37GB2 = 37'h001621FBAF; // 1.729121e-001 in Q31
                SEC4 : r37GB2 = 37'h00269D6DDB; // 3.016794e-001 in Q31
                SEC5 : r37GB2 = 37'h002DBE66BD; // 3.573731e-001 in Q31
                SEC6 : r37GB2 = 37'h002190E183; // 2.622339e-001 in Q31
                SEC7 : r37GB2 = 37'h02E23C76A5; // 5.767470e+000 in Q31
                default: r37GB2 = 0;
            endcase

            3: //176.4 kHz SAP
            case (r3Section)
                SEC1 : r37GB2 = 37'h1FFB68A354; // -3.586920e-002 in Q31
                SEC2 : r37GB2 = 37'h0005A87CB7; // 4.420432e-002 in Q31
                SEC3 : r37GB2 = 37'h001637EF23; // 1.735820e-001 in Q31
                SEC4 : r37GB2 = 37'h0026A6D964; // 3.019668e-001 in Q31
                SEC5 : r37GB2 = 37'h002DCAC536; // 3.577506e-001 in Q31
                SEC6 : r37GB2 = 37'h00217824B6; // 2.614790e-001 in Q31
                SEC7 : r37GB2 = 37'h02749D6F8F; // 4.911055e+000 in Q31
                default: r37GB2 = 0;
            endcase
        endcase
    end
end

assign w34ASum1 = r34GA1 + r34GA2;
assign w34ASum1n = r1LastCnt ? ~w34ASum1 : w34ASum1;
assign w34IMux1 = r1LastCnt ? { {5{r29DataInReg[28]}}, r29DataInReg } : 1;
assign w37BSum1 = r37GB2 + r37GB1;
assign w37BSum2 = w37BSum1 + r37GB0;
assign w37BSum2n = r1LastCnt ? ~w37BSum2 : w37BSum2;

always @(posedge i1Clk or negedge i1nReset)
if (~i1nReset) begin
    r34Acc1 <= 0;
    r37Acc2 <= 0;
    r32D0MSBs <= 0;
    r29DataInReg <= 0;
    or19DataOut1 <= 0;
    or29DataOut2 <= 0;
end else begin

    if (r1FiltEn) begin
        if (r1FirstCnt) begin
            r32D0MSBs   <= r34Acc1;
            r34Acc1     <= 0;
            r37Acc2     <= 0;
            case (r3Section)
                SEC1 : r29DataInReg <= { {11{i18DataIn1[17]}}, i18DataIn1 };
```

```
                SEC2 : r29DataInReg <= { {2{i27DataIn2[26]}}, i27DataIn2 };
                default : r29DataInReg <= r37Acc2[28:0];
            endcase
        end else begin
            r32D0MSBs <= {1'b0, r32D0MSBs[31:1]};
            r34Acc1 <= w34ASum1n + { r34Acc1[33], r34Acc1[33:1] } + w34IMux1;
            r37Acc2 <= w37BSum2n + { r37Acc2[36], r37Acc2[36:1] } + r1LastCnt;
        end
    end

    if (r1FiltEnDly && r1FirstCnt)
        case (r3Section)
            SEC2 : or19DataOut1 <= r37Acc2[18:0];
            SEC8 : or29DataOut2 <= r37Acc2[28:0];
        endcase
end

//The following logic was separated from the above procedure because
//the Synplicity tool could not recognize these as SRL16s.  It is true
//that SRL16s cannot have a reset in Virtex and VirtexE parts.  Synplify
//v6.1.3 was mistakenly not allowing these registers to use SRL16s because
//unrelated registers in the same procedure had resets.  Creating a separate
//procedure works around the problem.
always @(posedge i1Clk)

begin
    if (i1DRegClear) begin
        r192D0 <= {1'b0, r192D0[191:1]};
        r224D1 <= {r192D0[0], r224D1[223:1]};
        r224D2 <= {r224D1[0], r224D2[223:1]};
    end else if (r1FiltEn && ~r1FirstCnt) begin
        r192D0 <= {r32D0MSBs[0], r192D0[191:1]};
        r224D1 <= {r192D0[0], r224D1[223:1]};
        r224D2 <= {r224D1[0], r224D2[223:1]};
    end
end

endmodule
```