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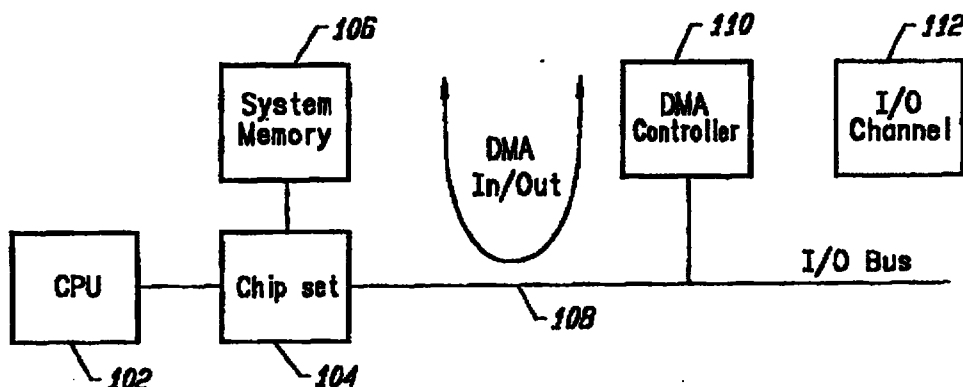
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(21) International Application Number: PCT/US97/13142 (22) International Filing Date: 24 July 1997 (24.07.97) (30) Priority Data: 08/716,555 18 September 1996 (18.09.96) US (71) Applicant: ELECTRONICS FOR IMAGING, INC. [US/US]; 2855 Campus Drive, San Mateo, CA 94403 (US). (72) Inventors: BLUMER, Marc; 3860 West Naughton Avenue, Belmont, CA 94002 (US). ANDO, Wayne; 937 Lake Tahoe Court, San Jose, CA 95123 (US). (74) Agents: GLENN, Michael, A. et al.; Law Offices of Michael A. Glenn, P.O. Box 7831, Menlo Park, CA 94026 (US).		(81) Designated States: AL, AU, BA, BB, BG, BR, CA, CN, CU, CZ, EE, GE, HU, IL, JP, KP, KR, LC, LK, LR, LT, LU, LV, MG, MK, MN, MX, NO, NZ, PL, RO, SG, SI, SK, TR, TT, UA, UZ, VN, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published With international search report.

(54) Title: SYSTEM FOR ALLOWING I/O PROCESSOR TO OPERATE UNDER DIFFERENT TRANSFER ALGORITHMS



(57) Abstract

A programmable DMA controller (110) that uses an instruction set dedicated to moving data efficiently over a bus (108), comprising a program memory (228), a program counter (226), a FIFO memory (222), a bus buffer (224), registers, an accumulator, and an ALU (220). The DMA controller instruction set comprises the following instructions: load, move, add, subtract, branch on zero, branch on not zero, lock, and interrupt. Another DMA controller embodiment uses a SIMD processor. In operation, a CPU downloads DMA programs to the DMA controller. The DMA controller stores these programs in its program memory. The CPU signals the DMA to begin a DMA transfer operation. The ALU and associated devices execute the program instructions to perform the desired DMA transfer. The DMA controller then sends an interrupt to the CPU to indicate the DMA transfer is complete.