CLAIMS

What is claimed is:

1. A method for correcting an analog equalizer, comprising:

monitoring a positive eye height of an output signal of an analog front end (AFE) circuit, the AFE circuit comprising at least one stage of analog equalizer;

generating a correction instruction in response to that the monitored positive eye height is lower than an eye height threshold; and

correcting the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold;

wherein the correcting the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold comprises:

in response to that the amplitude of the output signal is not lower than the amplitude threshold and the low-frequency gain of the analog equalizer is not lower than the lower limit, decreasing the low-frequency gain of the analog equalizer in the AFE circuit according to the second step size until the monitored positive eye height reaches the eye height threshold.

2. The method according to claim 1, wherein the correction instruction comprises a compensation function enabling instruction, and the compensation function enabling instruction is configured to instruct to enable a compensation function of the analog equalizer in the AFE circuit.

3. The method according to claim 1, wherein the correction instruction comprises a gain adjustment instruction;

the gain adjustment instruction is configured to instruct at least one of the following:

to increase a high-frequency gain of the analog equalizer in the AFE circuit according to a first step size;

to reduce a low-frequency gain of the analog equalizer in the AFE circuit according to a second step size.

4. The method according to any one of claims 1 to 3, wherein the monitoring the positive eye height of the output signal of the AFE circuit comprises:

sampling the output signal through a first decision circuit and a clock data recovery circuit to obtain a first data signal, an edge signal and a two-phase clock corresponding to the first data signal and the edge signal;

sampling the output signal according to a sampling clock through a second decision circuit to obtain a second data signal; and

comparing the second data signal with the first data signal to determine a relationship between the monitored positive eye height and the eye height threshold.

5. The method according to claim 4, wherein the comparing the second data signal with the first data signal to determine the relationship between the monitored positive eye height and the eye height threshold comprises:

in response to detecting a clock lock signal, reading the second data signal and the first data signal of the same length;

XORing a bit with a value of 1 in the first data signal and a value of a corresponding bit in the second data signal, and accumulating XOR results of each bit;

in response to that the accumulation result is 0, determining that the monitored positive eye height reaches the eye height threshold; or

in response to that the accumulation result is not 0, determining that the monitored positive eye height is lower than the eye height threshold or a positive eye diagram of the output signal is closed.

6. The method according to claim 4 or 5, wherein a sampling clock corresponding to the second data signal is synchronized and edge-aligned with a clock corresponding to the first data signal.

7. The method according to any one of claims 4 to 6, wherein the generating the correction instruction in response to that the monitored positive eye height is lower than the eye height threshold comprises:

in response to that the monitored positive eye height is lower than the eye height threshold, determining an on-off state of the compensation function of each analog equalizer in the AFE circuit, and a gain adjustment strategy for the analog equalizer based on the first data signal, the second data signal and the clock lock signal; and

generating the correction instruction based on the on-off state and the gain adjustment strategy.

8. The method according to any one of claims 4 to 7, further comprising:

determining a relationship between an amplitude of the output signal and an amplitude threshold based on the second data signal; and

determining whether the low-frequency gain of the analog equalizer in the AFE circuit is reduced to a lower limit based on the relationship between the amplitude of the output signal and the amplitude threshold.

9. The method according to claim 8, wherein the determining the relationship between the amplitude of the output signal and the amplitude threshold based on the second data signal comprises:

in response to detecting the clock lock signal, reading the second data signal of a set length;

counting number of bits with a value of 1 in the second data signal, or accumulating the values of each bit in the second data signal;

in response to that the number of bits with a value of 1 is greater than or equal to a set value, or the accumulation result is greater than or equal to the set value, determining that the amplitude of the output signal reaches the amplitude threshold;

in response to that the number of bits with a value of 1 is less than the set value, or the accumulation result is less than the set value, determining that the amplitude of the output signal is lower than the amplitude threshold.

10. The method according to any one of claims 1 to 9, wherein the correcting the analog equalizer in the AFE circuit according to the correction instruction until the monitored positive eye height reaches the eye height threshold comprises:

enabling the compensation function of the analog equalizer in the AFE circuit according to

the correction instruction;

based on an initial state, increasing the high-frequency gain of the analog equalizer in the AFE circuit according to the first step size until the monitored positive eye height reaches the eye height threshold; and

in response to that the high-frequency gain of the analog equalizer is increased to an upper limit and the monitored positive eye height has not yet reached the eye height threshold, enabling the compensation function of at least one stage of the analog equalizer that is not enabled and repeating the operation of increasing the high-frequency gain, or reducing the low-frequency gain of the analog equalizer in the AFE circuit according to the second step size until the monitored positive eye height reaches the eye height threshold.

11. The method according to claim 10, wherein the initial state comprises: the low-frequency gain of the analog equalizer is set to a maximum value, and the high-frequency gain of the analog equalizer is set to a minimum value.

12. A control chip, comprising: a memory, a processor, and a computer program stored on the memory and operable on the processor, when the computer program is executed by the processor, the method for correcting an analog equalizer according to any one of claims 1 to 11 is implemented.

13. A receiver, comprising:

an analog front end (AFE) circuit;

a monitoring circuit; and

the control chip according to claim 12,

wherein an output end of the AFE circuit is connected to an input end of the monitoring circuit, an output end of the monitoring circuit is connected to an input end of the control chip, and the control chip is configured to correct an analog equalizer in the AFE circuit according to a monitoring result of the monitoring circuit.

14. The receiver according to claim 13, wherein:

the monitoring circuit comprises a first decision circuit, a clock data recovery circuit and a second decision circuit;

the first decision circuit is configured to sample an output signal of the AFE circuit according to a two-phase clock provided by the clock data recovery circuit to obtain a first data signal and an edge signal; and

the second decision circuit is configured to sample the output signal according to a sampling clock to obtain a second data signal.

15. A computer-readable storage medium, wherein a computer program is stored on the computer-readable storage medium, and when the computer program is executed by a processor, the method for correcting an analog equalizer according to any one of claims 1 to 11 is implemented.