FIG. 1

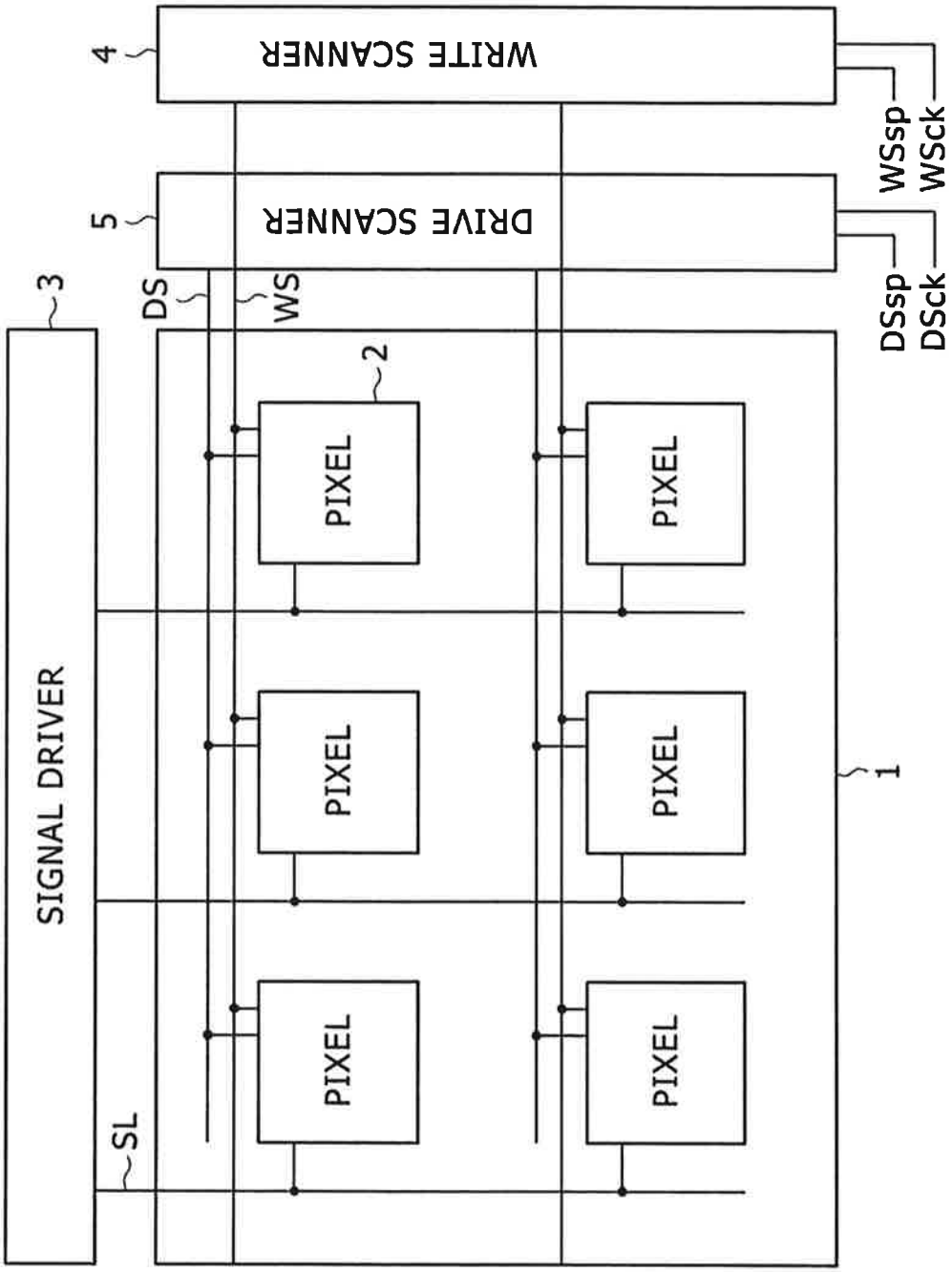

WRITE SCANNER
4
DRIVE SCANNER
5
WSsp
WSck
DSsp
DSck
3
DS
WS
2
PIXEL
SIGNAL DRIVER
SL
1

FIG. 2

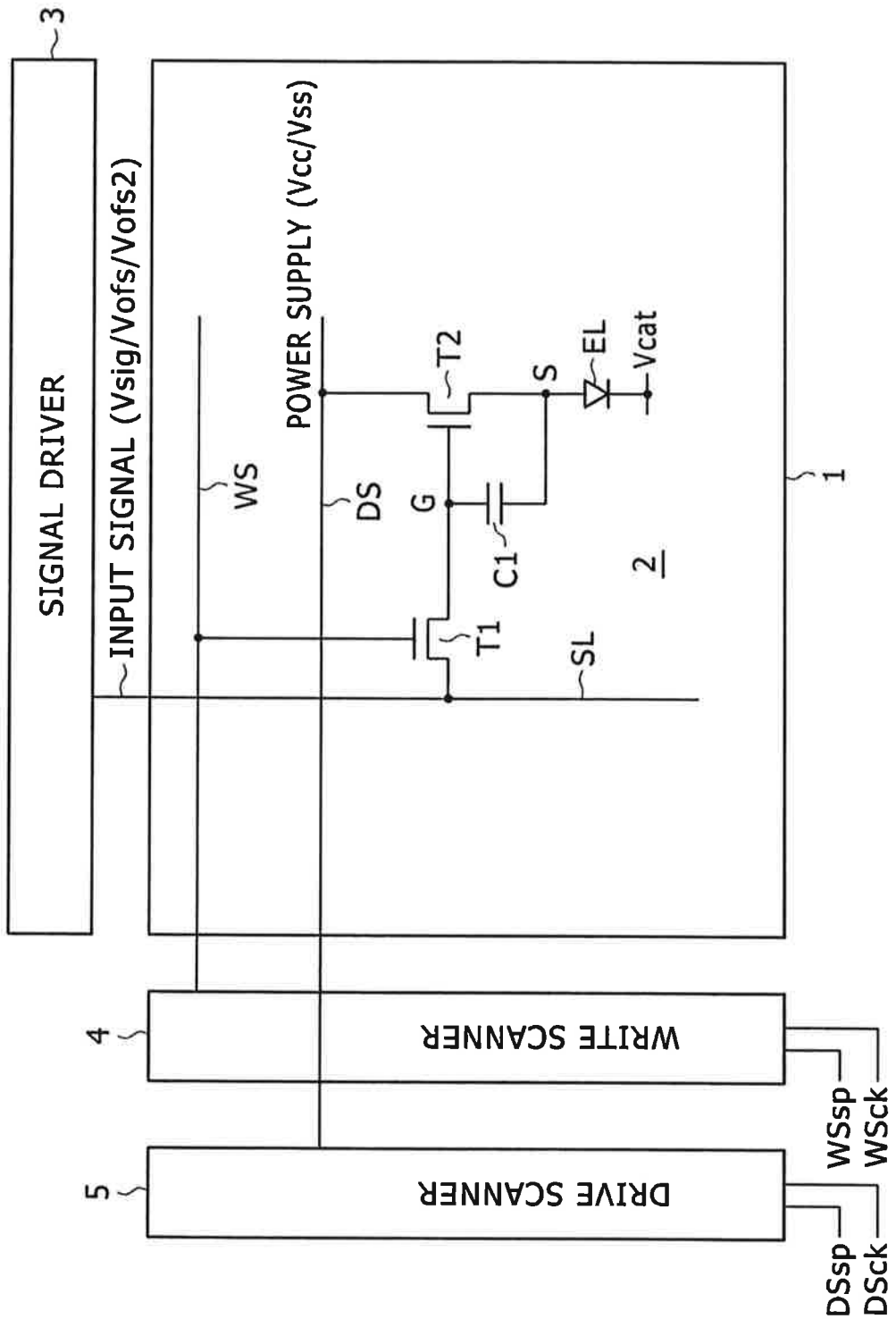

3
SIGNAL DRIVER
INPUT SIGNAL (Vsig/Vofs/Vofs2)
POWER SUPPLY (Vcc/Vss)
WS
DS
G
T2
S
EL
Vcat
C1
T1
SL
2
1
4
WRITE SCANNER
5
DRIVE SCANNER
WSsp
WSck
DSsp
DSck

FIG. 3

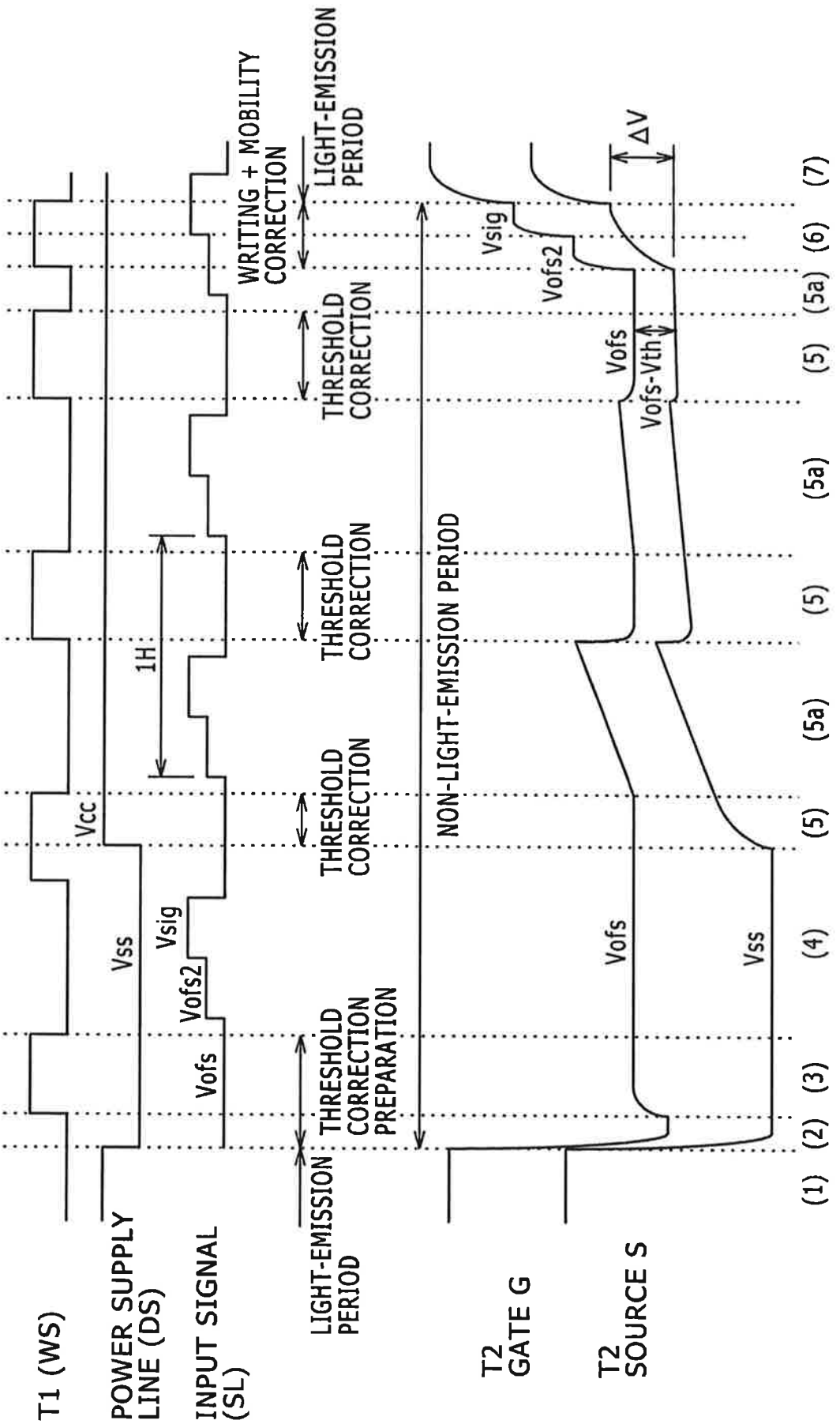

T1 (WS)
POWER SUPPLY LINE (DS)
INPUT SIGNAL (SL)
T2 GATE G
T2 SOURCE S
Vcc
Vss
Vsig
Vofs2
Vofs
1H
ΔV
Vofs-Vth
LIGHT-EMISSION PERIOD
THRESHOLD CORRECTION PREPARATION
THRESHOLD CORRECTION
THRESHOLD CORRECTION
THRESHOLD CORRECTION
WRITING + MOBILITY CORRECTION
LIGHT-EMISSION PERIOD
NON-LIGHT-EMISSION PERIOD
(1) (2) (3) (4) (5) (5a) (5) (5a) (5) (5a) (6) (7)

FIG. 4
(1)

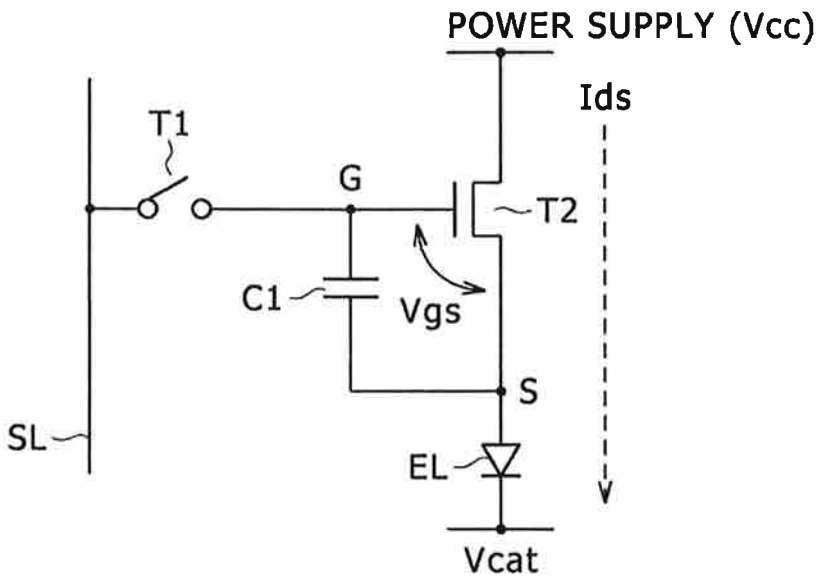

POWER SUPPLY (Vcc)
Ids
T1
G
T2
C1
Vgs
S
SL
EL
Vcat

FIG. 5
(2)

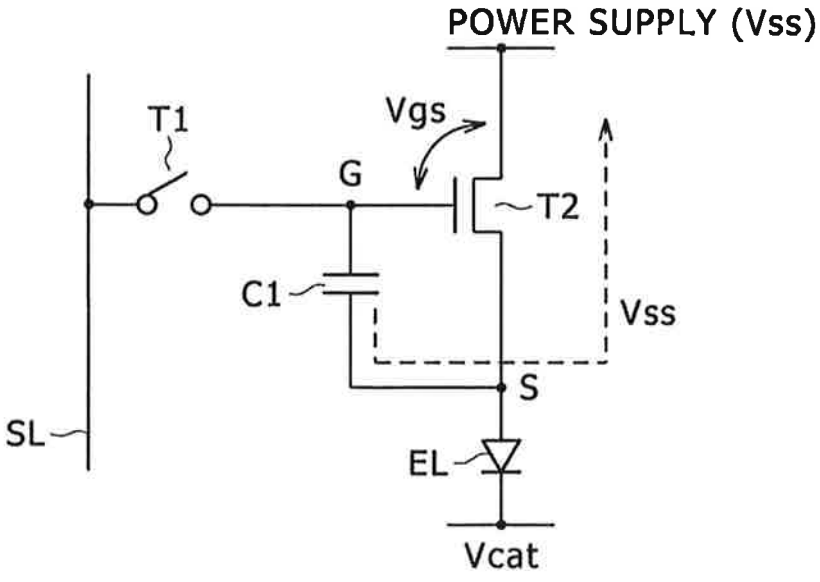

POWER SUPPLY (Vss)
T1
Vgs
G
T2
C1
Vss
S
SL
EL
Vcat

FIG. 6
(3)

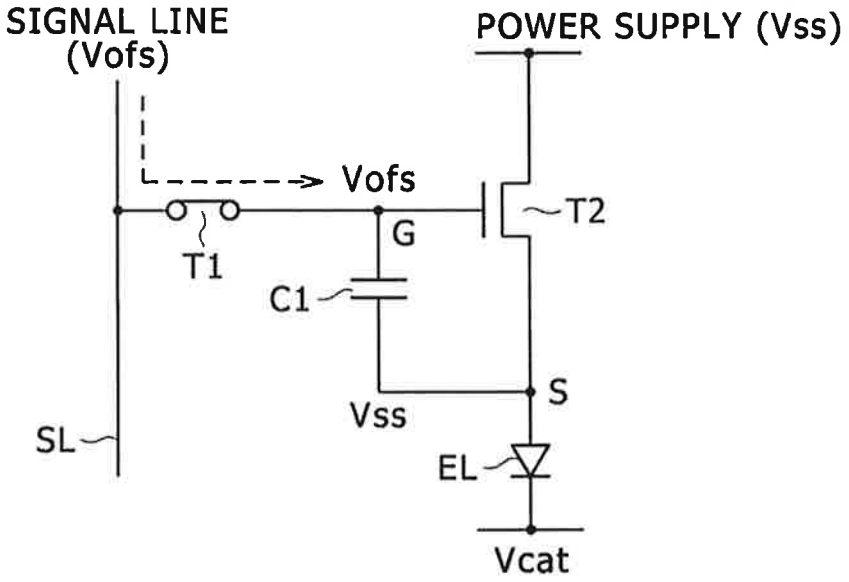

SIGNAL LINE
(Vofs)
POWER SUPPLY (Vss)
Vofs
T2
G
T1
C1
S
Vss
SL
EL
Vcat

FIG. 7
(5)

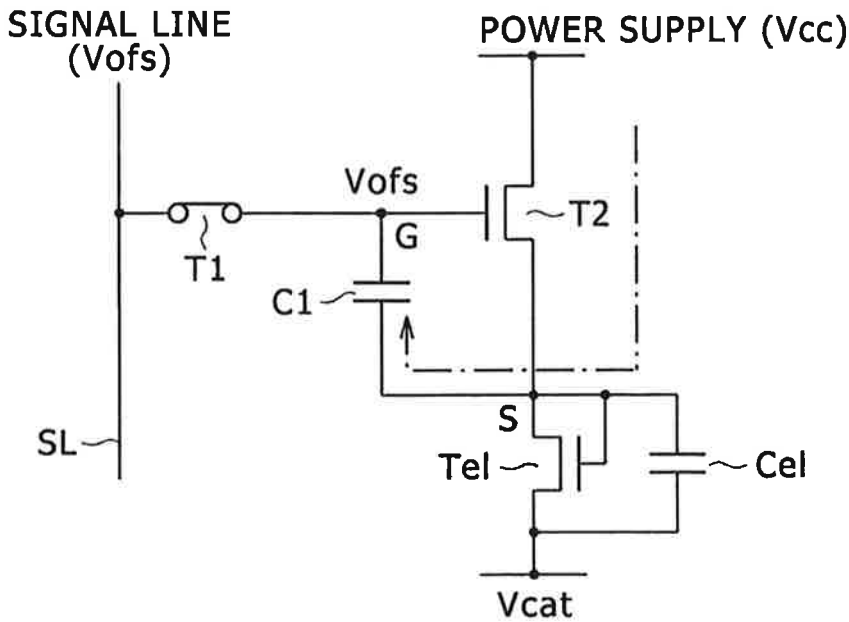

SIGNAL LINE
(Vofs)
POWER SUPPLY (Vcc)
Vofs
T2
G
T1
C1
S
SL
Tel
Cel
Vcat

FIG. 8

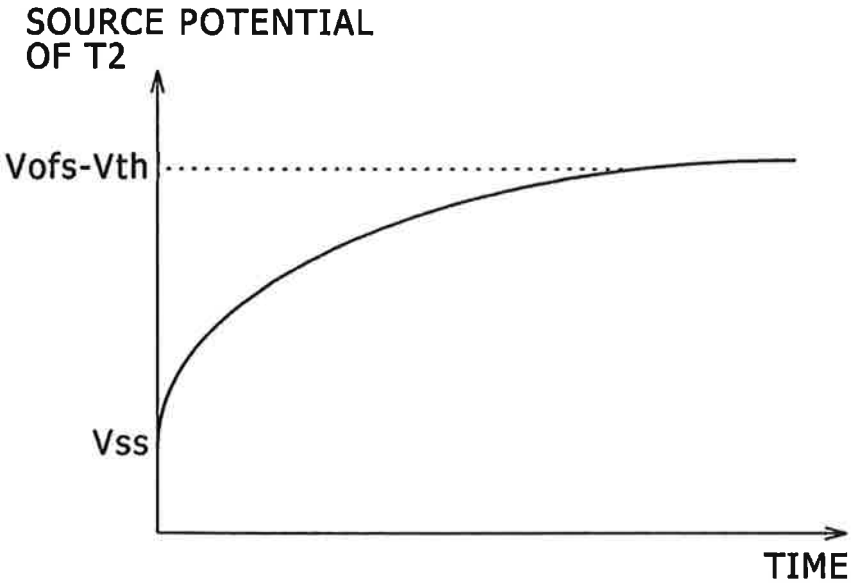

SOURCE POTENTIAL
OF T2
Vofs-Vth
Vss
TIME

FIG. 9

(5a)

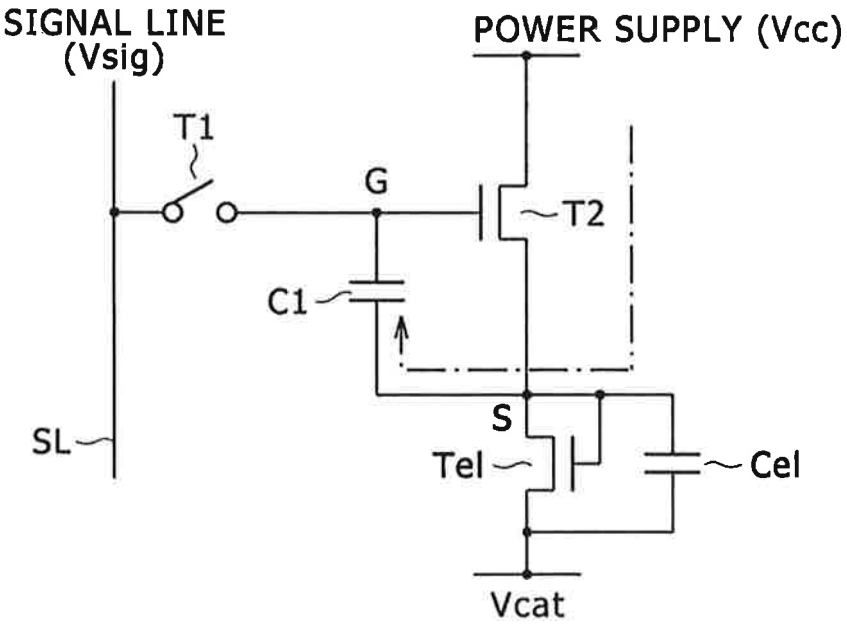

SIGNAL LINE
(Vsig)
POWER SUPPLY (Vcc)
T1
G
T2
C1
S
SL
Tel
Cel
Vcat

FIG. 10
(6)

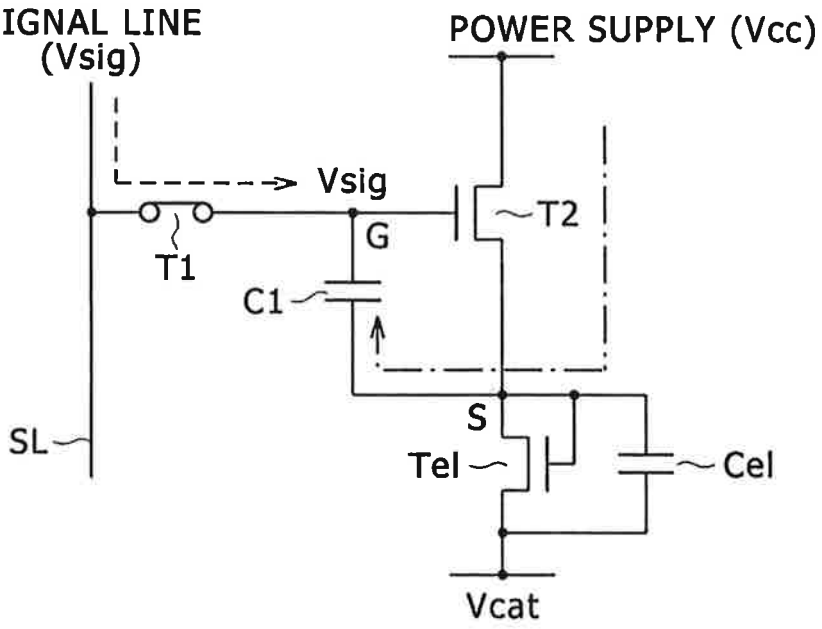


FIG. 11

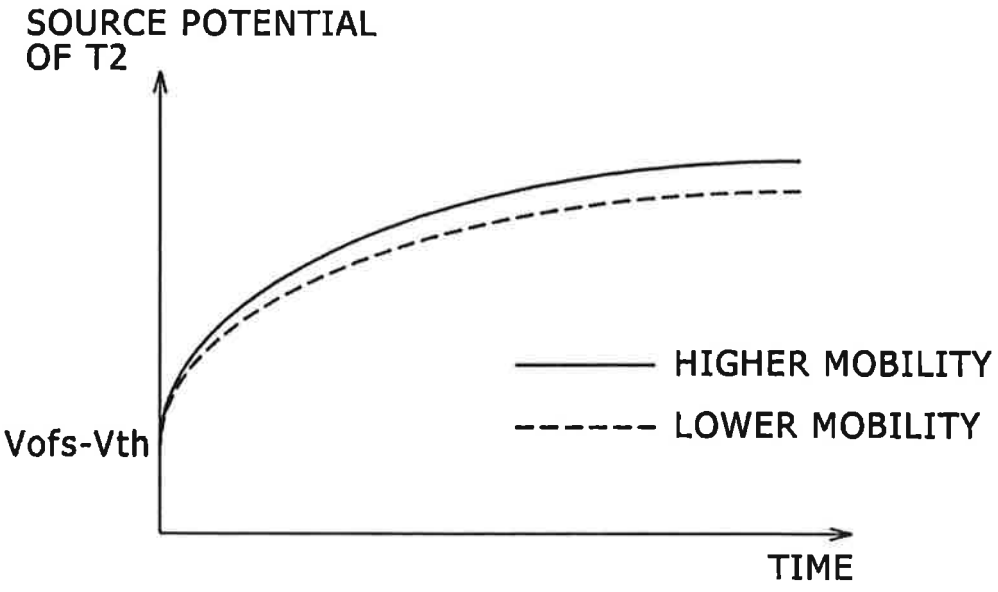


FIG. 12

(7)

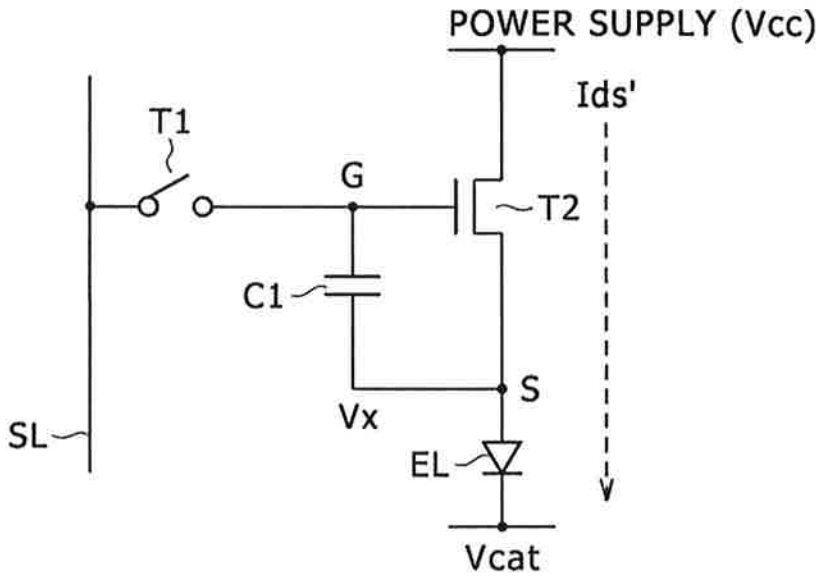


FIG.13A

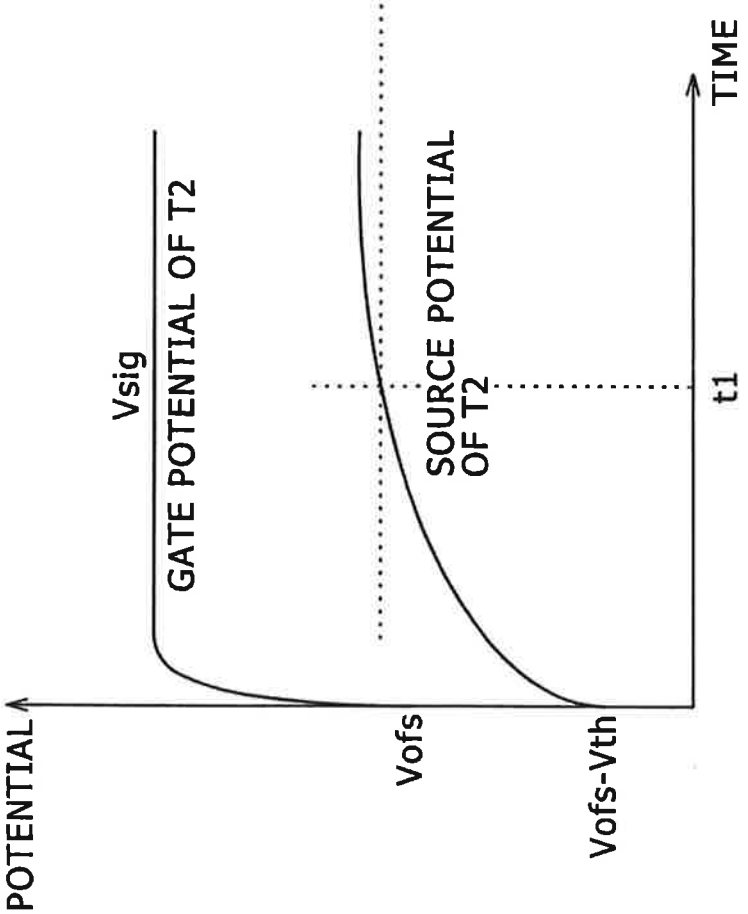


FIG.13B

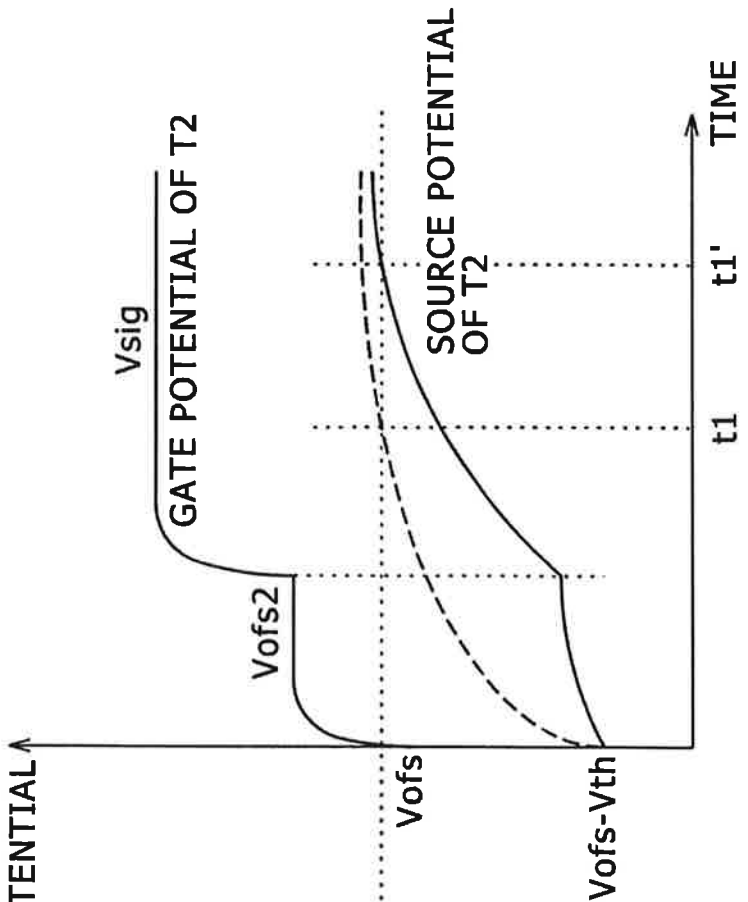


FIG.14A

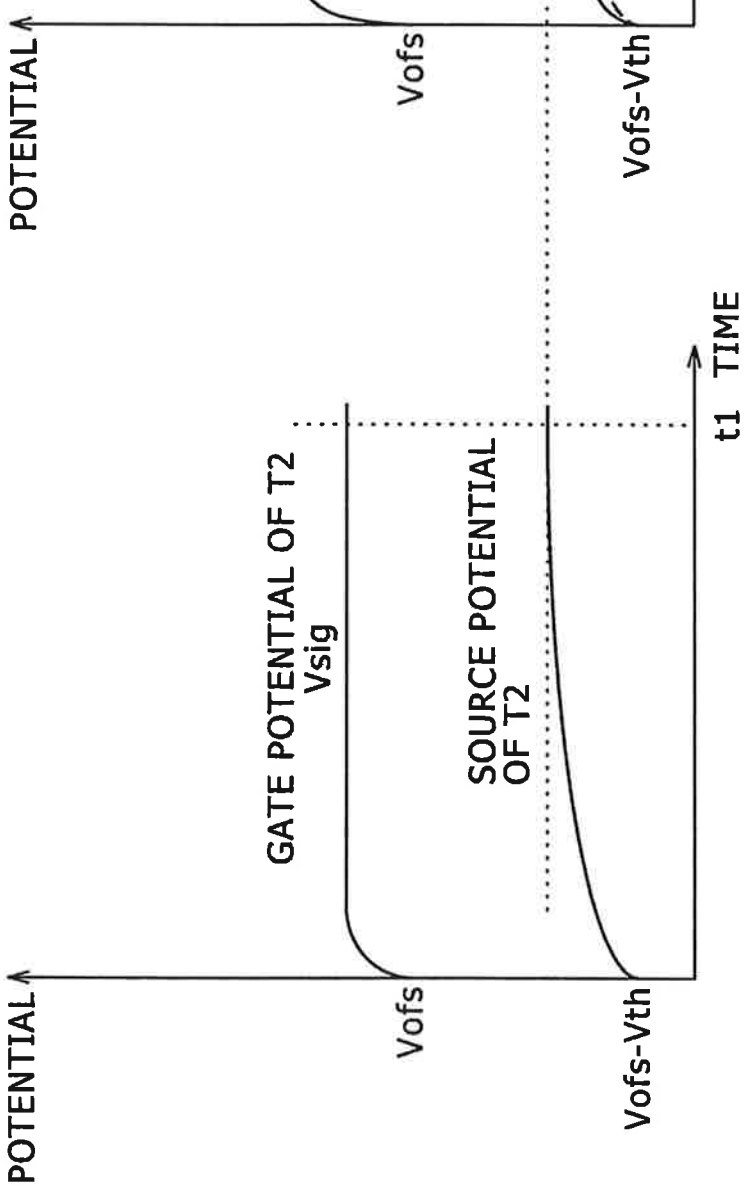


FIG.14B

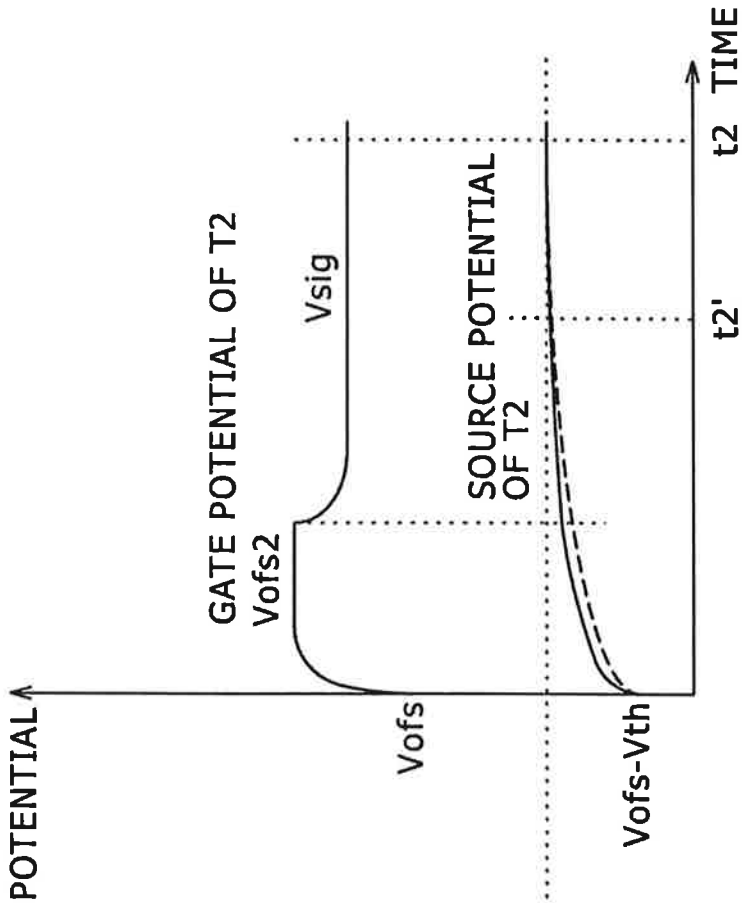


FIG. 15

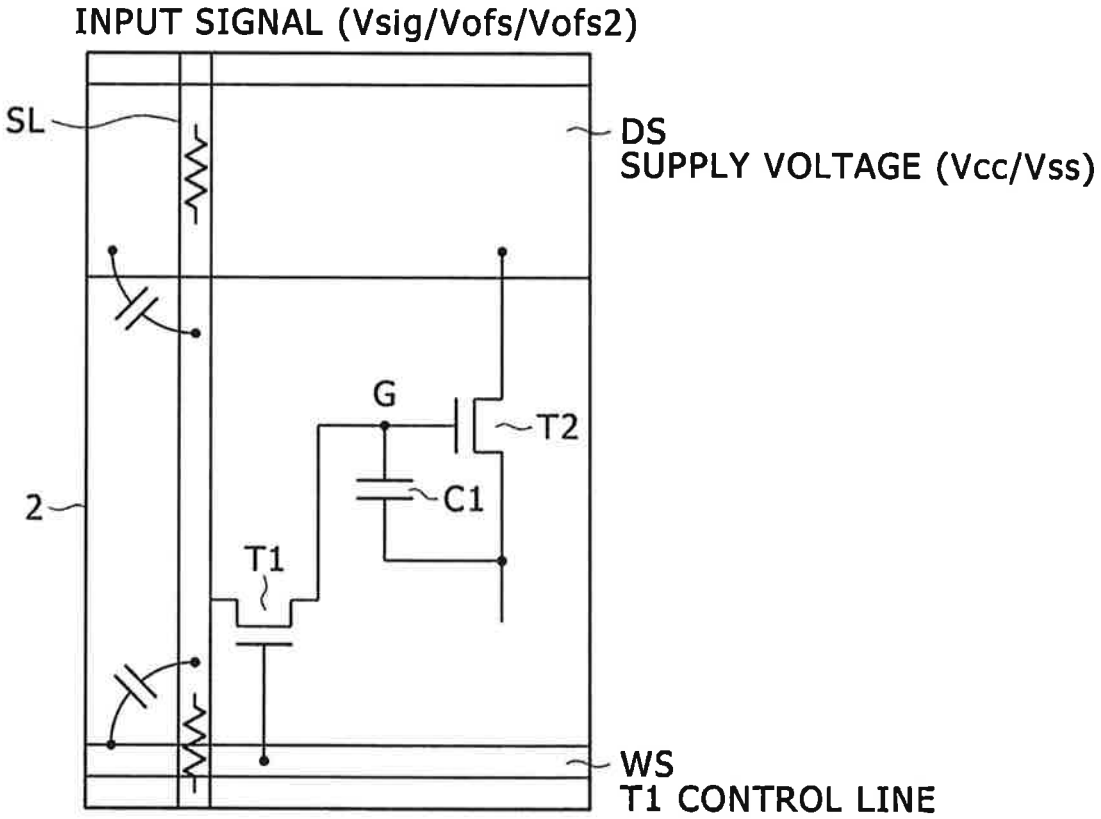

INPUT SIGNAL (Vsig/Vofs/Vofs2)
SL
DS
SUPPLY VOLTAGE (Vcc/Vss)
G
T2
C1
2
T1
WS
T1 CONTROL LINE

FIG.16

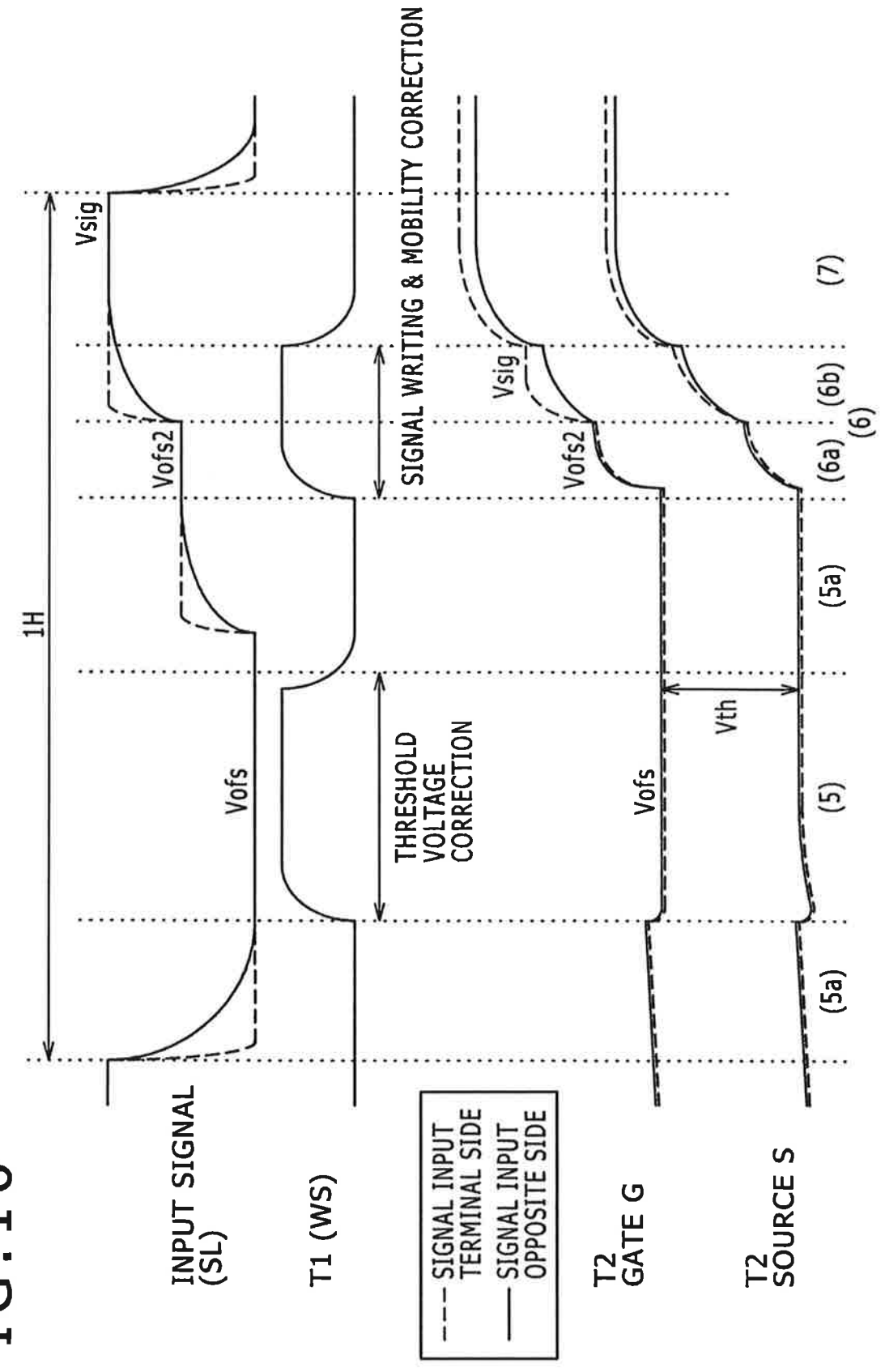

INPUT SIGNAL (SL)
T1 (WS)
T2 GATE G
T2 SOURCE S
1H
Vsig
Vofs2
Vofs
THRESHOLD VOLTAGE CORRECTION
SIGNAL WRITING & MOBILITY CORRECTION
Vth
SIGNAL INPUT TERMINAL SIDE
SIGNAL INPUT OPPOSITE SIDE
(5a)
(5)
(5a)
(6a)
(6b)
(6)
(7)

FIG.17

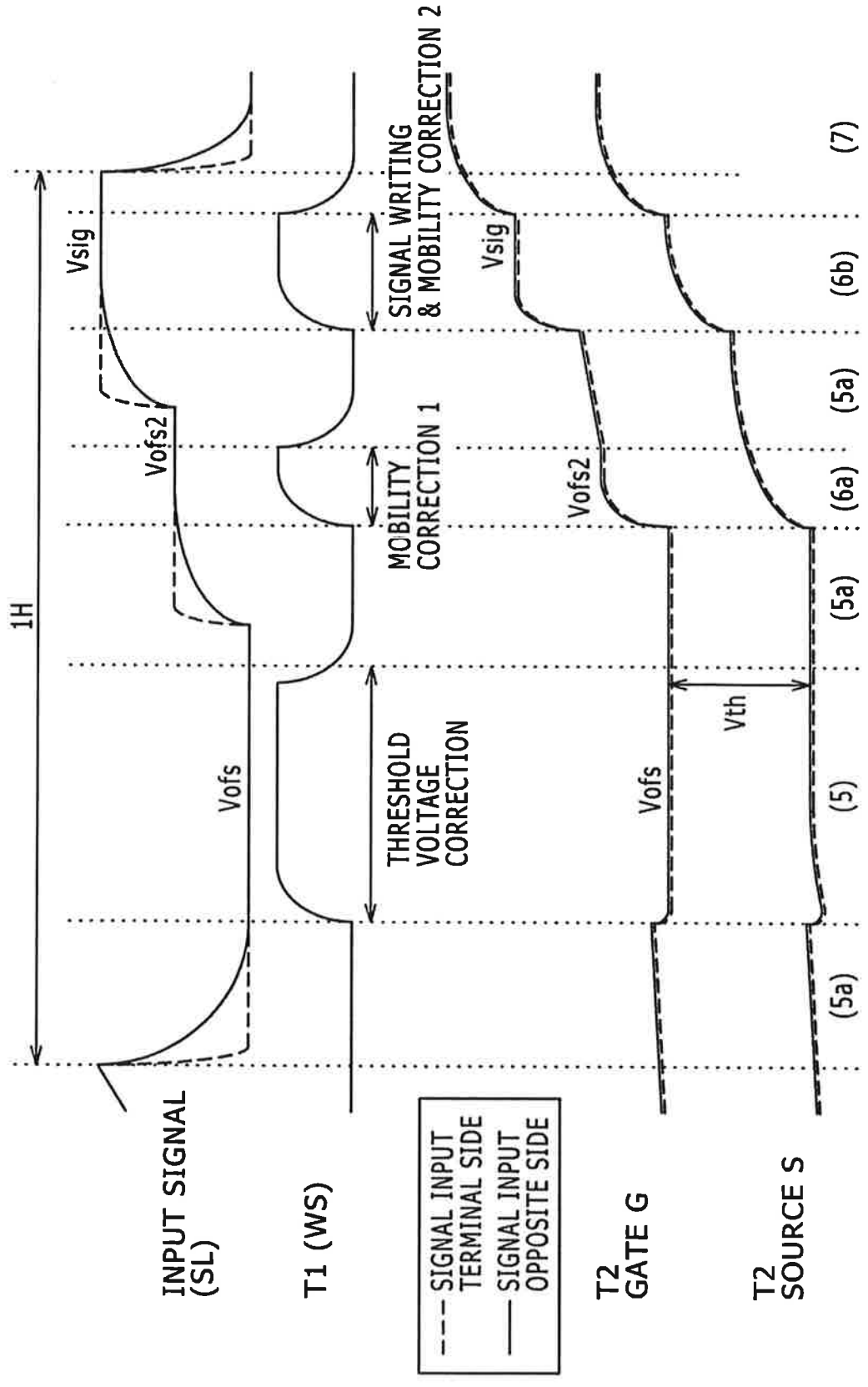

INPUT SIGNAL (SL)
T1 (WS)
T2 GATE G
T2 SOURCE S
1H
Vsig
Vofs2
Vofs
THRESHOLD VOLTAGE CORRECTION
MOBILITY CORRECTION 1
SIGNAL WRITING & MOBILITY CORRECTION 2
Vth
(5a)
(5)
(5a)
(6a)
(5a)
(6b)
(7)
SIGNAL INPUT TERMINAL SIDE
SIGNAL INPUT OPPOSITE SIDE

FIG.18

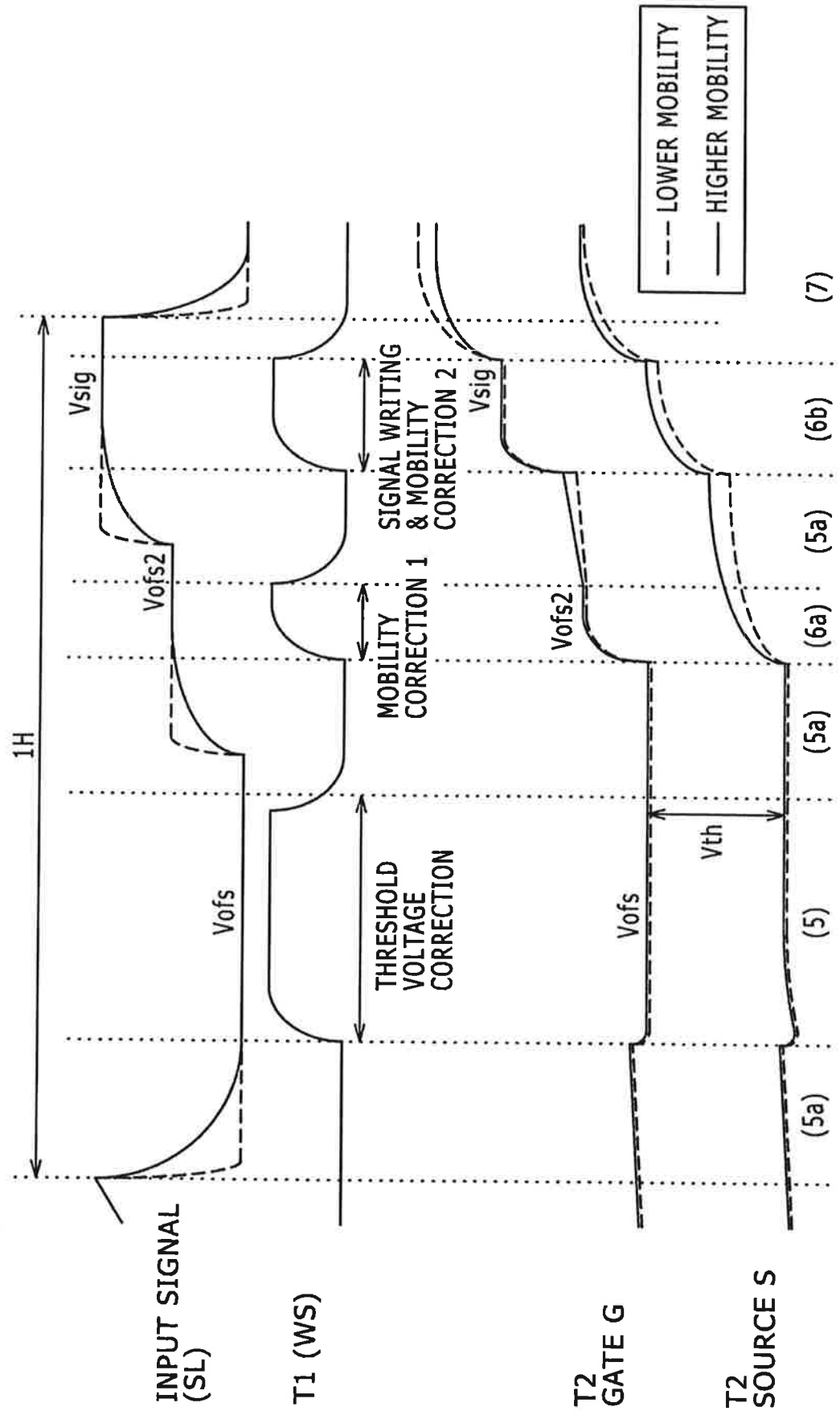

INPUT SIGNAL (SL)
T1 (WS)
T2 GATE G
T2 SOURCE S
1H
Vsig
Vofs2
Vofs
THRESHOLD VOLTAGE CORRECTION
MOBILITY CORRECTION 1
SIGNAL WRITING & MOBILITY CORRECTION 2
Vth
LOWER MOBILITY
HIGHER MOBILITY
(5a)
(5)
(5a)
(6a)
(5a)
(6b)
(7)

FIG.19

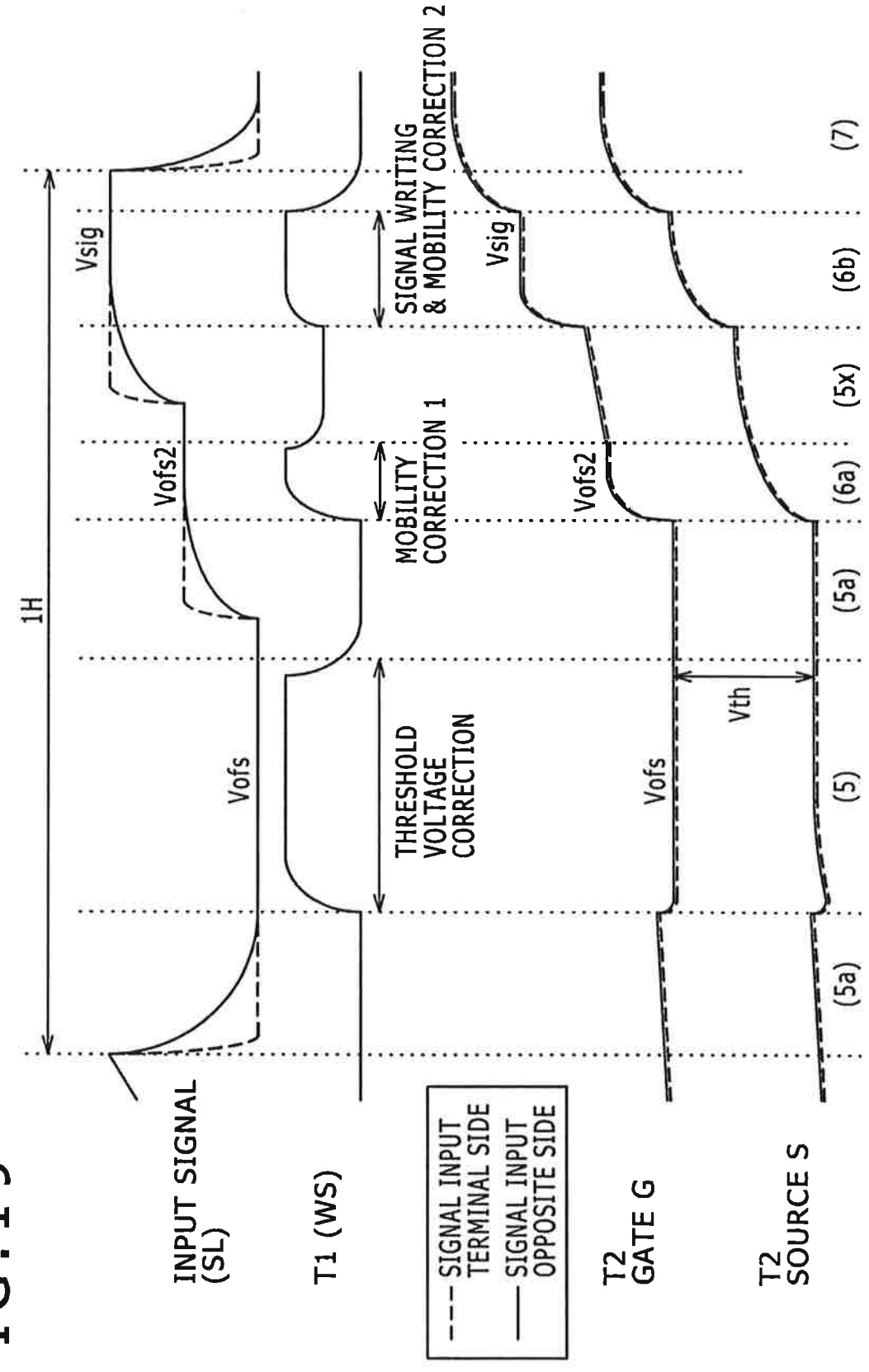

INPUT SIGNAL (SL)
T1 (WS)
T2 GATE G
T2 SOURCE S
1H
Vsig
Vofs2
Vofs
THRESHOLD VOLTAGE CORRECTION
MOBILITY CORRECTION 1
SIGNAL WRITING & MOBILITY CORRECTION 2
Vth
(5a)
(5)
(5a)
(6a)
(5x)
(6b)
(7)
SIGNAL INPUT TERMINAL SIDE
SIGNAL INPUT OPPOSITE SIDE

FIG.20

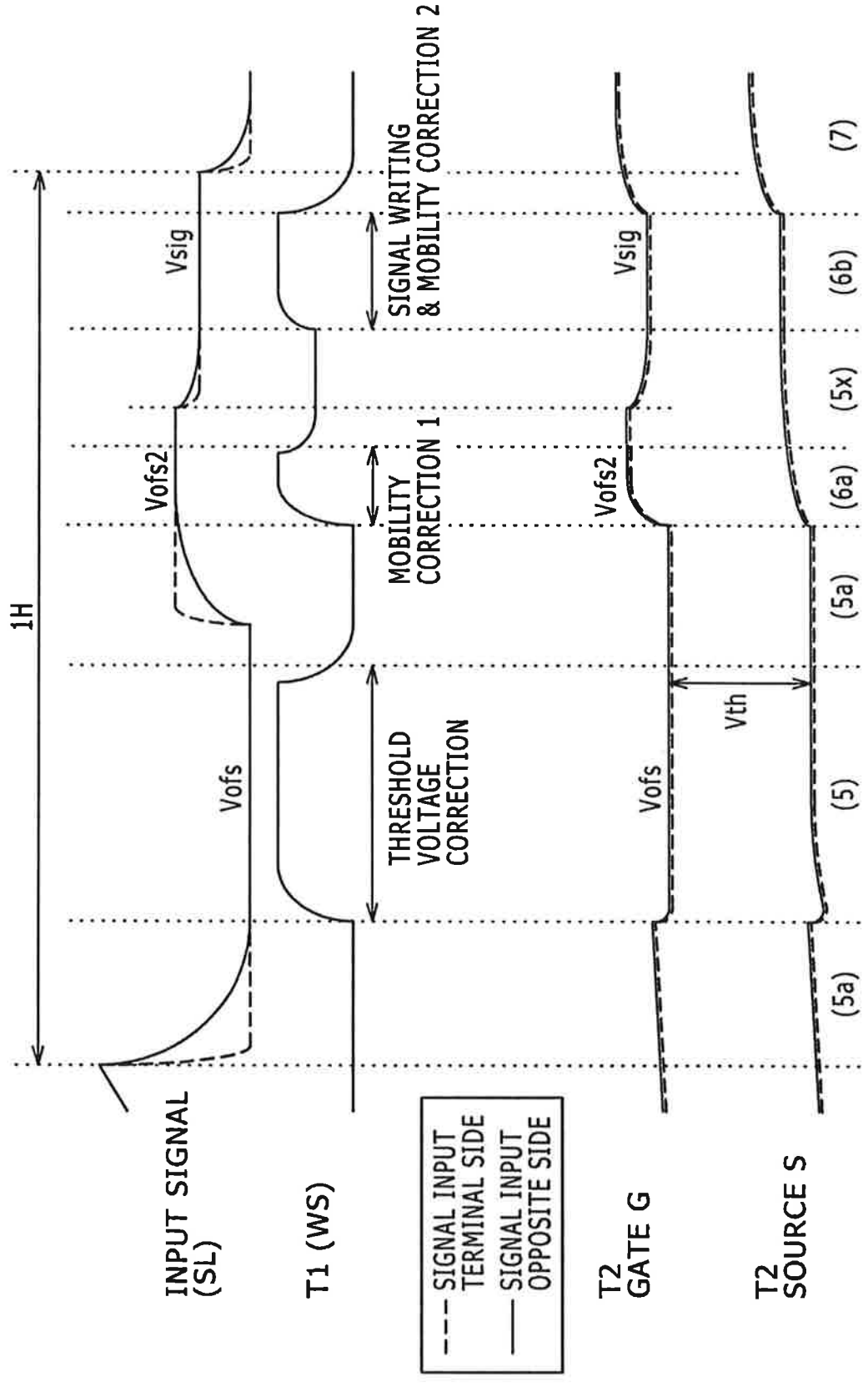

INPUT SIGNAL (SL)
T1 (WS)
T2 GATE G
T2 SOURCE S
1H
Vofs
Vofs2
Vsig
THRESHOLD VOLTAGE CORRECTION
MOBILITY CORRECTION 1
SIGNAL WRITING & MOBILITY CORRECTION 2
Vth
(5a)
(5)
(5a)
(6a)
(5x)
(6b)
(7)
SIGNAL INPUT TERMINAL SIDE
SIGNAL INPUT OPPOSITE SIDE

FIG.21

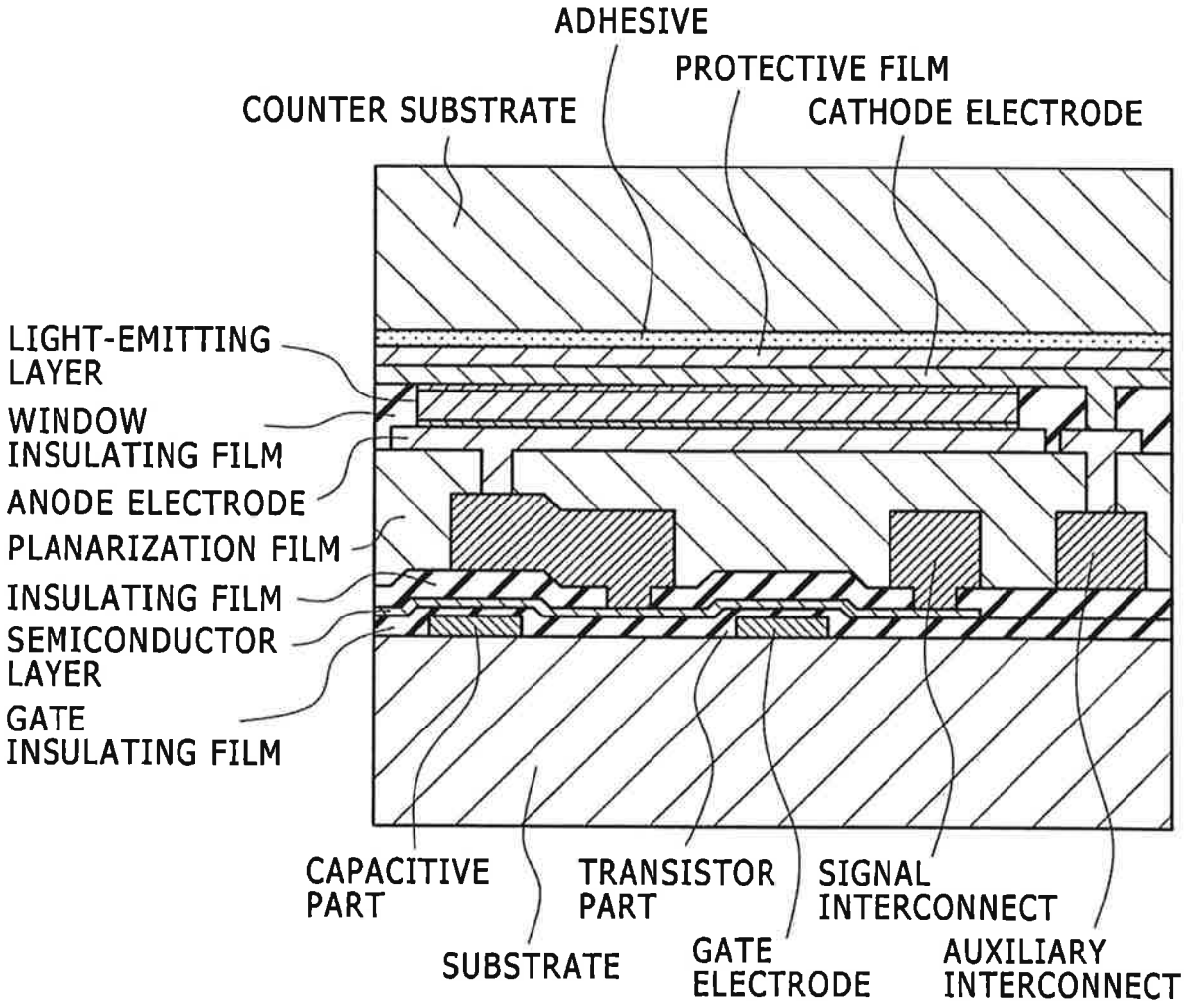

ADHESIVE
PROTECTIVE FILM
COUNTER SUBSTRATE
CATHODE ELECTRODE
LIGHT-EMITTING LAYER
WINDOW INSULATING FILM
ANODE ELECTRODE
PLANARIZATION FILM
INSULATING FILM
SEMICONDUCTOR LAYER
GATE INSULATING FILM
CAPACITIVE PART
TRANSISTOR PART
SIGNAL INTERCONNECT
SUBSTRATE
GATE ELECTRODE
AUXILIARY INTERCONNECT

FIG.22

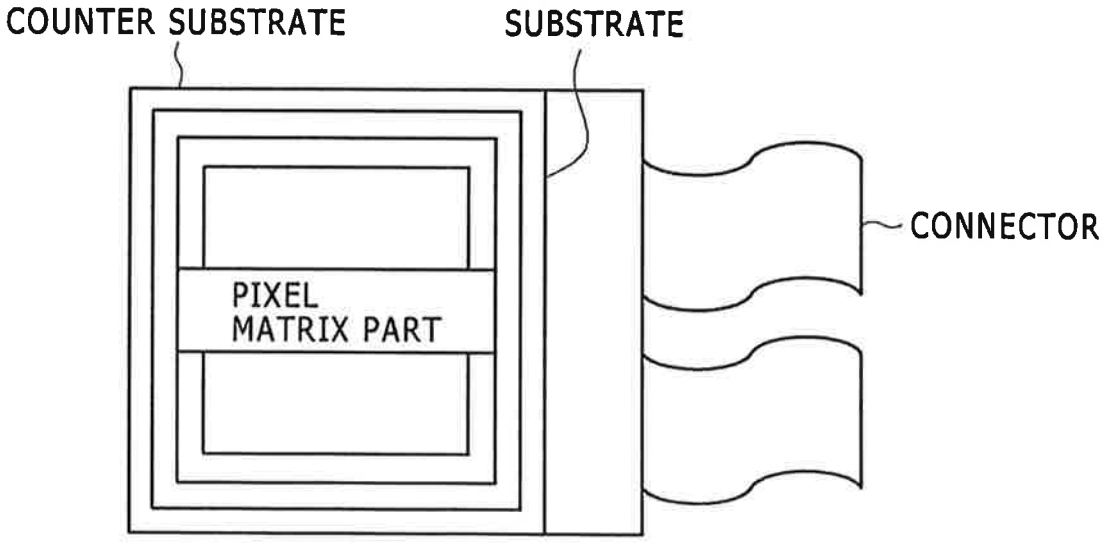

COUNTER SUBSTRATE
SUBSTRATE
CONNECTOR
PIXEL MATRIX PART

FIG.23

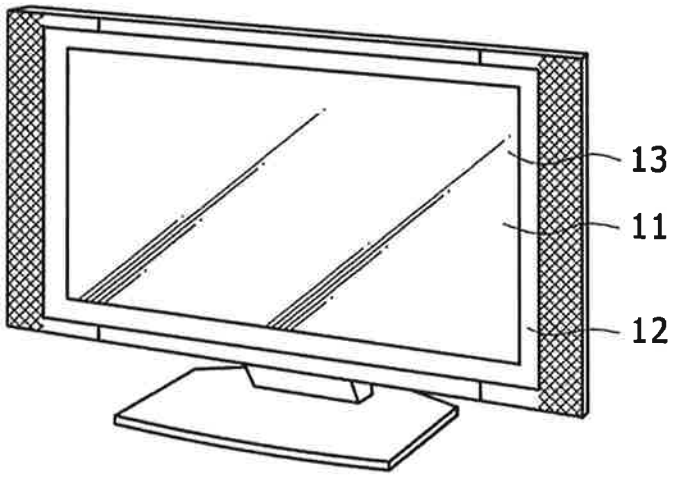


FIG.24

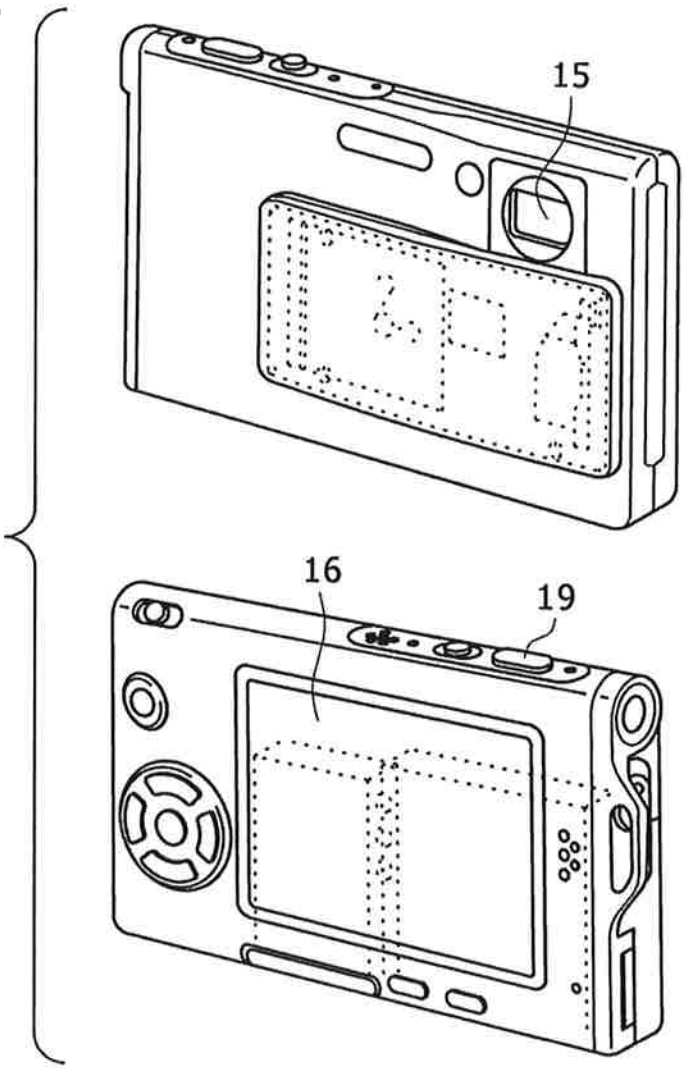


FIG.25

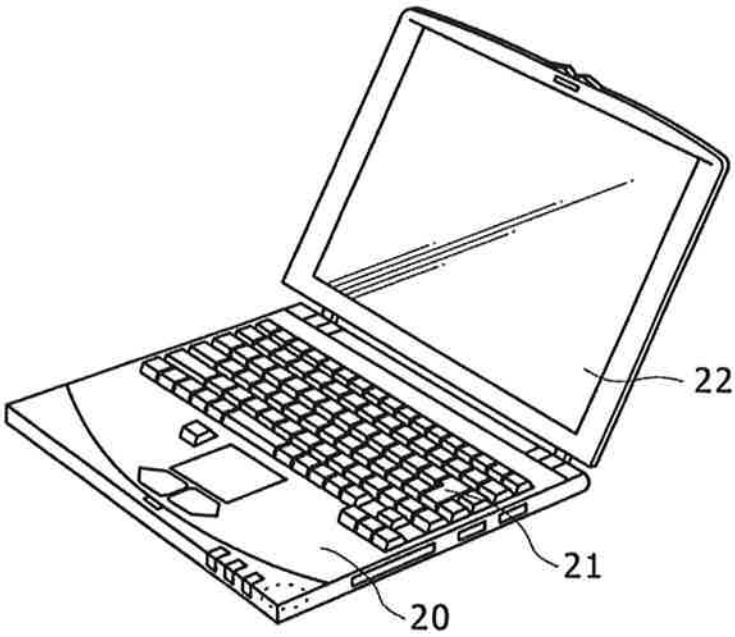


FIG.26

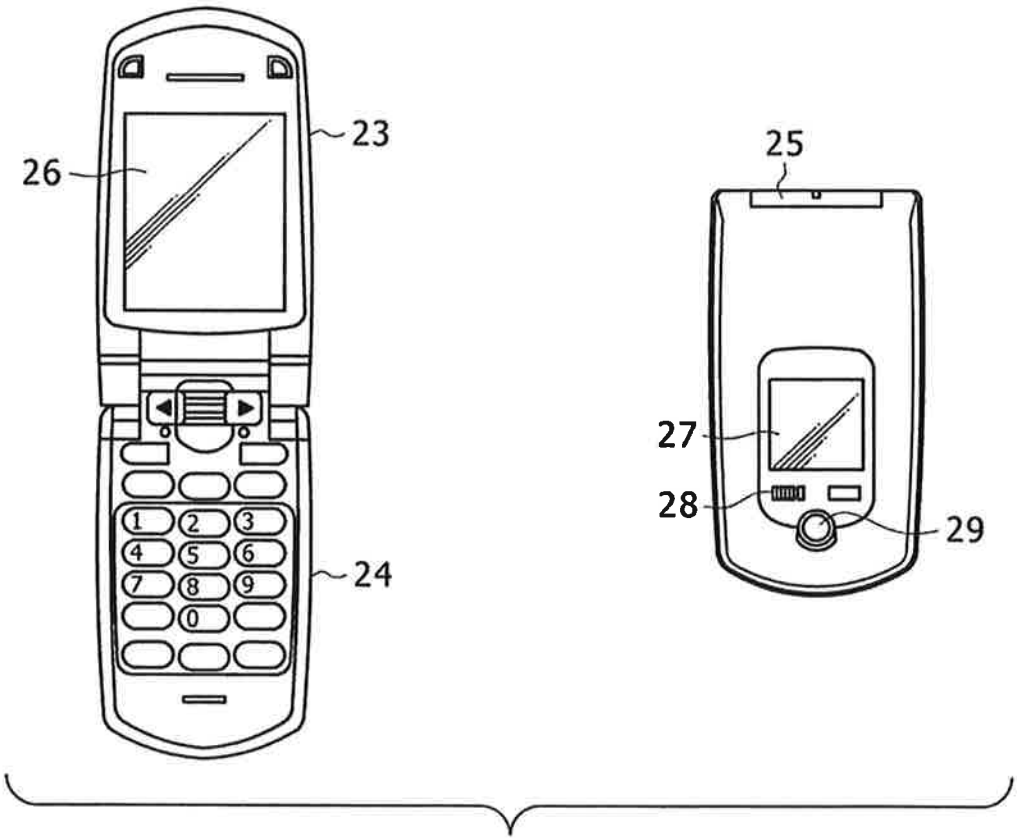


FIG.27

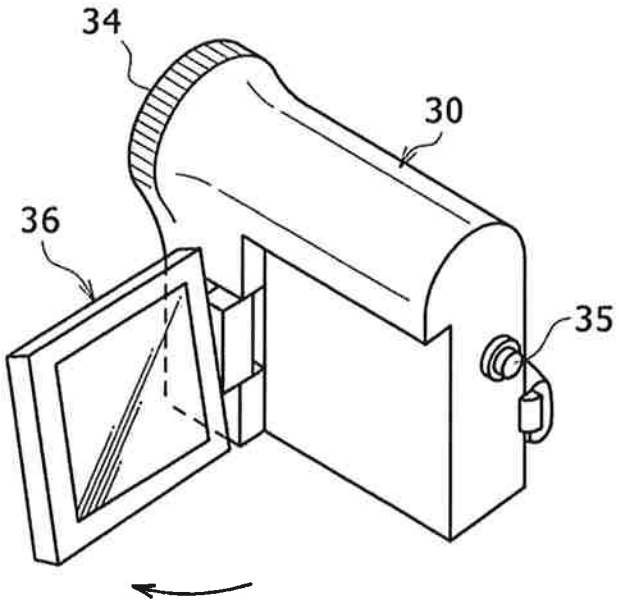


FIG.28

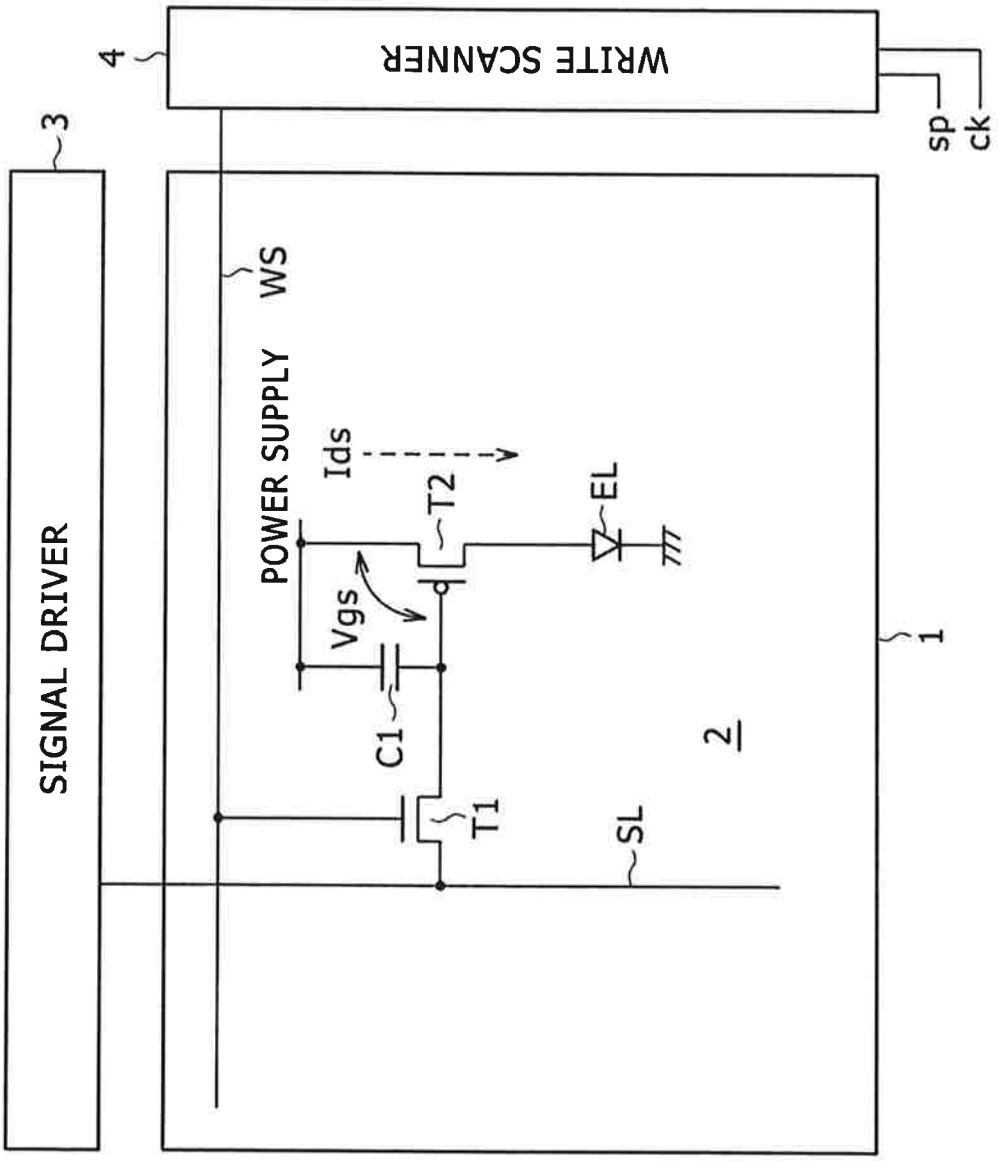

WRITE SCANNER
4
sp
ck
3
SIGNAL DRIVER
WS
POWER SUPPLY
Ids
T2
EL
Vgs
C1
T1
SL
2
1

FIG.29

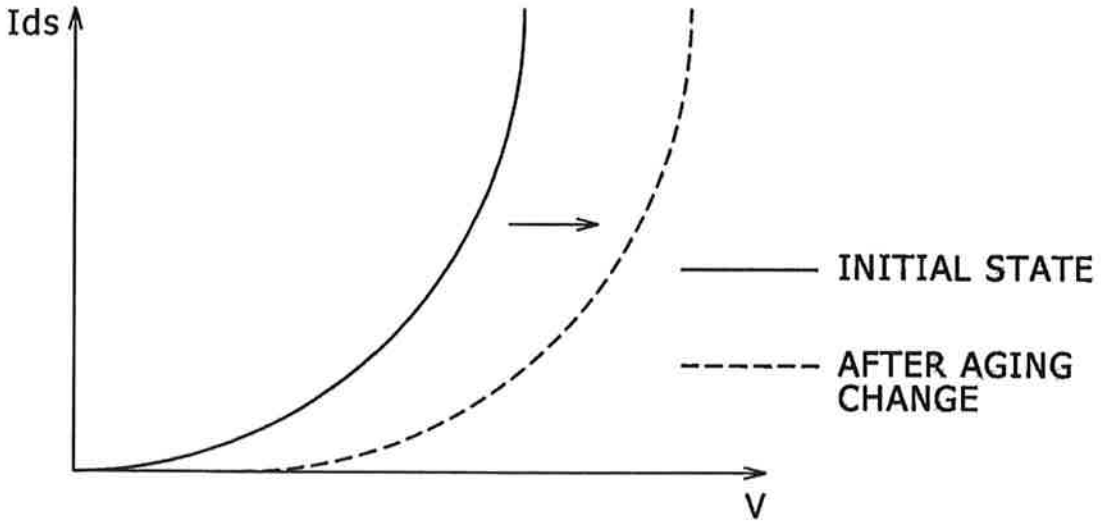
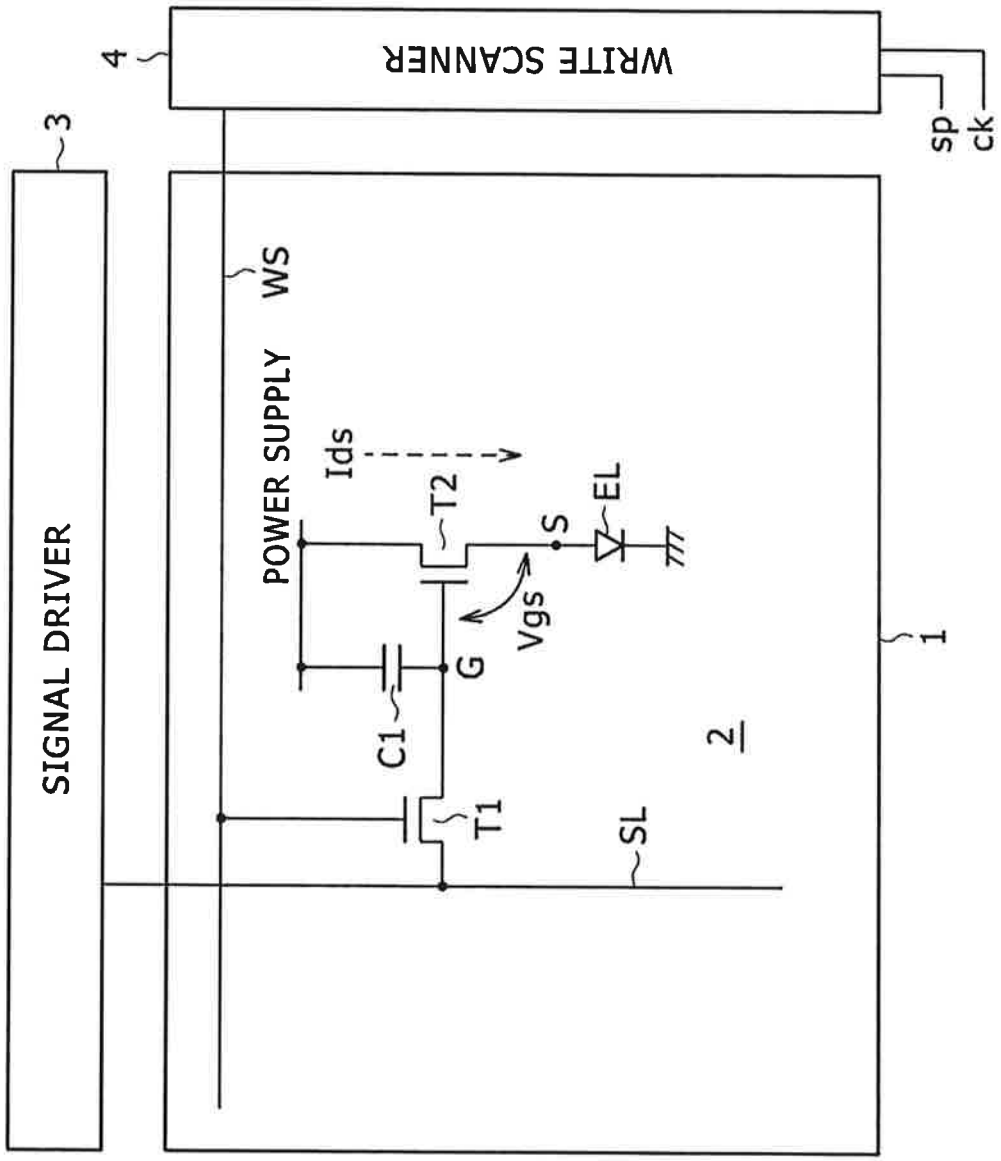


FIG.30


WRITE SCANNER
4
sp
ck
3
SIGNAL DRIVER
WS
POWER SUPPLY
Ids
T2
S
EL
Vgs
G
C1
T1
SL
2
1