

WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:
 - a first substrate;
 - a first semiconductor chip disposed on and mounted to the first substrate;
 - an interposer chip on the first semiconductor chip;
 - a first pad disposed on the interposer chip;
 - a second pad disposed on the interposer chip and spaced apart from the first pad; and
 - a bonding wire electrically connected to the second pad and the first substrate,wherein the second pad is electrically connected through the interposer chip to the first pad, and
the interposer chip has a footprint greater than that of the first semiconductor chip, and has a thermal conductivity greater than that of the first substrate such that heat generated from the first semiconductor chip is released through the interposer chip.
2. The semiconductor package of claim 1, wherein the interposer chip has a thermal conductivity in a range of 30 W/mK to 2000 W/mK.
3. The semiconductor package of claim 1 or claim 2, further comprising a solder ball on the first pad.
4. The semiconductor package of any one of claims 1 to 3, wherein the

interposer chip completely covers a top surface of the first semiconductor chip.

5. The semiconductor package of any one of claims 1 to 4, further comprising a substrate pad on the first substrate and coupled to the bonding wire,

wherein the first pad constitutes one of a plurality of first pads adjacent one side of the semiconductor package, the substrate pad constitutes one of a plurality of substrate pads adjacent said one side of the semiconductor package, the plurality of first pads have a first pitch by which the first pads are spaced from each other in a direction parallel to said one side of the semiconductor package, the plurality of substrate pads have a second pitch by which the plurality of substrate pads are spaced from each other in the direction parallel to said one side of the semiconductor package, and the first pitch is greater than the second pitch.

6. The semiconductor package of any one of claims 1 to 5, further comprising a molding layer on the first substrate and the interposer chip,

wherein the molding layer covers the second pad but not the first pad.

7. The semiconductor package of any one of claims 1 to 6, further comprising:

an upper package on the interposer chip; and

a connection structure interposed between and electrically connecting the upper package and the first pad.

8. The semiconductor package of claim 7, wherein the upper package includes:

a second substrate;
a second semiconductor chip disposed on and mounted to the second substrate;
a plurality of upper pads on a top surface of the second substrate, the upper pads electrically connected to the second semiconductor chip; and
a plurality of lower pads on a bottom surface of the second substrate and electrically connected to the upper pads,
wherein a pitch of the lower pads is greater than a pitch of the upper pads.

9. The semiconductor package of claim 8, wherein the second semiconductor chip is a memory chip, and the semiconductor package includes at least one other memory chip disposed on and mounted to the second substrate.

10. The semiconductor package of any one of claims 1 to 9, wherein, when viewed in plan, the first pad lies within a region bounded by the first semiconductor chip.

11. A semiconductor package, comprising:
a first substrate;
a first semiconductor chip disposed on and mounted to the first substrate;
a dummy chip disposed on the first semiconductor chip and having a footprint greater than that of the first semiconductor chip;
a redistribution layer on a top surface of the dummy chip;
a plurality of solder ball pads on the redistribution layer;
a bonding wire pad connected to the redistribution layer and electrically

connected through the redistribution layer to at least one of the solder ball pads; and

a molding layer disposed on the first substrate and covering the redistribution layer and the bonding wire pad,

wherein the molding layer has a plurality of openings that lead to and open at the solder ball pads, and

the dummy chip has a thermal conductivity greater than that of the first substrate such that heat generated from the first semiconductor chip is released through the dummy chip.

12. The semiconductor package of claim 11, wherein

when viewed in plan, at least one of the solder ball pads lies within a region bounded by the first semiconductor chip, and another of the solder ball pads is spaced apart from the region bounded by the first semiconductor chip.

13. The semiconductor package of claim 11 or claim 12, further comprising:

a plurality of substrate pads on a top surface of the first substrate; and

a bonding wire coupled to the bonding wire pad and one of the substrate pads,

wherein a pitch of the solder ball pads is greater than a pitch of the substrate pads.

14. The semiconductor package of any one of claims 11 to 13, further comprising:

an upper package; and

a plurality of connection structures interposed between the upper package and the solder ball pads,

wherein the upper package is electrically connected through the connection structures to the redistribution layer.

15. The semiconductor package of claim 14, wherein the molding layer and the upper package have a gap therebetween.

16. A semiconductor package, comprising:

a first substrate including a substrate pad;

a first semiconductor chip disposed on and mounted to the first substrate;

an interposer chip disposed on the first semiconductor chip and including a redistribution layer comprising a wiring pattern;

a solder ball on a top surface of the interposer chip; and

a bonding wire extending from the top surface of the interposer chip, the bonding wire coupled to the substrate pad,

wherein the solder ball is electrically connected through the redistribution layer to the bonding wire,

the interposer chip has a width, in a direction parallel to an upper surface of the first substrate, greater than a width of the first semiconductor chip in said direction, and

the interposer chip has a thermal conductivity greater than that of the first substrate such that heat generated from the first semiconductor chip is released through the interposer chip.

17. The semiconductor package of claim 16, wherein, when viewed in plan, the first semiconductor chip lies completely in a region bounded by the interposer chip.

18. The semiconductor package of claim 16 or claim 17, further comprising an adhesive layer between the first semiconductor chip and the interposer chip,

wherein the adhesive layer has a thermal conductivity in a range of 0.2 W/mK to 10 W/mK.

19. The semiconductor package of any one of claims 16 to 18, further comprising:

a first pad between the interposer chip and the solder ball;

a second pad on the top surface of the interposer chip, the second pad coupled to the bonding wire; and

a molding layer on the interposer chip,

wherein the molding layer covers the second pad but not the solder ball.

20. A semiconductor package, comprising:

a first substrate including an insulating body, and first substrate pads and second substrate pads of electrically conductive material at a top surface of the insulating body;

a first semiconductor chip flip-chip mounted to the first substrate as disposed on and electrically connected to the first substrate pads of the first substrate;

an interposer on the first semiconductor chip, the interposer having an upper

portion including a redistribution layer comprising wiring patterns;

a plurality of first pads of electrically conductive material disposed on the interposer;

a plurality of second pads of electrically conductive material disposed on the interposer and spaced laterally outwardly of the plurality of first pads;

bonding wires electrically connecting the second pads disposed on the interposer and the second substrate pads, respectively; and

a molding layer disposed on the first substrate and in which the interposer, the first semiconductor chip and the bonding wires are encapsulated,

wherein the second pads are electrically connected by the wiring patterns of the redistribution layer of the interposer to the first pads,

the molding layer has a plurality of openings therein that leads to and opens at the plurality of first pads disposed on the interposer, and

the interposer has a footprint greater than that of the first semiconductor chip, and has a thermal conductivity greater than that of the first substrate such that heat generated from the first semiconductor chip is released through the interposer.