

The invention concerns a circuit for the generation of a line blanking impulse in picture reproduction devices.

In picture reproduction devices with line scanning pattern, the electron beam, for example, is blanked during the horizontal retrace in order to avoid disturbing stripes upon reproduction of the picture. A line blanking impulse is required for this blanking. This is normally generated from the horizontal flyback (horizontal retrace) impulse which is often additionally loaded by diodes for the high voltage rectification and gives a correspondingly deformed flyback impulse. The flyback impulse (Fig. 1) approximately consists of a negative direct voltage which is overlaid by positive half sine wave shaped impulses during the line retrace, whereby the greater part of the half sine waves has a positive voltage.

However, the line output transformer (under load) generates undesirable preshoots and backlashes (ringing) in the flyback impulse.

There are comparator circuits known, for example, TEA 2029 from the Thomson Semiconducteurs Data Book 1986, consumer IC's, which obtain a line blanking impulse from the flyback impulse by means of a threshold voltage and a comparator. However, for the size of this threshold voltage, one must normally make a compromise: one either sets the threshold voltage higher, thereby advantageously gaining a clean but relatively short and late starting line blanking impulse input, or one sets the threshold voltage lower, thereby advantageously gaining a line blanking impulse with an early start and longer duration but with the qualified risk of after-blanking because of dispersion. This means that the threshold voltage of the comparator circuit is momentarily exceeded by impulse peaks at the end of the half sine wave and the comparator circuit generates additional output impulses through which the active frame is blanked at the edge in some places.

It is the object of the invention to indicate an improved line blanking circuit which generates an early starting line blanking impulse without disturbing additional output impulses.

This task is solved by the features given in patent claim 1. Further advantageous developments of the invention are given in the subclaims.

The solution consists of the fact that the threshold voltage is set low and from a point in time where the descending edge of the half sine wave starts, respectively for a certain duration within which the ringing has safely decayed, a new setting of the comparator circuit is prevented by a supplementary circuit within the comparator circuit.

In the following, an embodiment example of the invention is illustrated by means of the drawings. These show in:

Fig. 1 a flyback impulse with ringing,

Fig. 2 the line blanking circuit according to the invention.

Fig. 1 shows a typical flyback impulse. The amplitude has a value of, for example, $63 V_{ss}$, whereby the positive peak of the flyback impulse has a voltage of about 60 V. A 0 V line is shown. At the rear end of the flyback impulse one can see some ringings, the first of which projects above the 0 V line. The flyback impulse can also have a reversed polarity and be correspondingly inverted.

Fig. 2 shows a line blanking circuit with a flyback impulse input 21. The flyback impulse is connected to the input 21 via a non-illustrated protective resistor. The transistors Q21 and Q23 form a comparator. The flyback impulse is fed to the base of transistor Q23 and a threshold voltage of, for example, 1.3 V, is fed to the base of Q21 as a reference. The emitter of transistor Q20 then has a voltage of about 0.6 V. According to the above example, the flyback voltage is -3 V during the line trace. The voltage over the protective resistor (about 3.6 V) and its resistance value determine the load independent current which flows into the input 21.

A phil signal, which is present in the picture reproduction device anyway, is fed to input 22. The phil signal is a square wave signal at line frequency and

changes its logic level approximately in the temporal middle of the flyback impulse. The flyback impulse is to be expected in the area of, for example, ± 5 micro-seconds, around this phil edge.

The essence of the invention consists in the following: a capacitor C1 is charged to a certain level by the load independent current at input 21 during the line trace. If the ascending edge of the flyback impulse causes a, for example, 5 per cent lower load independent current, then the line blanking impulse becomes active. The charging of the capacitor C1 is maintained from a following first point in time until a second point in time. If the load independent current again climbs above, for example, 95 per cent of the value it had during the line trace, then the line blanking impulse is terminated. The edge of the phil signal located in the middle of the flyback impulse advantageously prevents, for the duration of the impulse, a new start of the line blanking impulse caused by ringing in the flyback impulse. Following this period, a start of the line blanking impulse is again enabled, for example, through the phil signal.

The capacitor has, for example, a value of 10 - 15 pF. Due to the fact that this capacity is small (and is therefore, easily integrated), the charging current supplied by Q12 and the discharging current should also have a corresponding value of only about one micro-ampere. The output 23 supplies a square wave form phi2 signal which is derived from the flyback impulse and whose switch edges lie within the line blanking impulse to be generated. The phi2 signal is internally used to limit the charging and discharging process of C1 to particular time segments. Therefore, sensible charging and discharging voltages are the advantageous result despite the small capacity of C1. The first point in time coincides, for example, with the ascending edge and the second point in time with the correspondingly descending edge of the phi2 signal.

Before the start of the flyback impulse, the capacitor C1 in the line blanking circuit charges itself on the voltage which ensues from the load independent current at the base of Q13. The load independent current is determined by the protective resistor and the negative direct voltage of the flyback impulse during the line trace. The voltage at C1 practically represents a reference voltage. The line blanking circuit is advantageously self-adjusting and adjusts itself to level tolerances of the flyback impulse automatically because it is clamped to this reference voltage during the line trace. An alignment is no longer necessary. Ringing in the line

output transformer is no longer disturbing because of the momentary blocking of the start of a further line blanking impulse carried out by the phi2 signal.

The transistors Q10 and Q13 form a difference amplifier; the transistors Q11 and Q14 represent a current reflector (current mirror). The ratio of the resistors R9 to R10 (for example, 500 / 10,000 corresponding to 5 per cent) determines the amount by which the voltage at the base of Q9 must increase in comparison to the voltage over the capacitor C1 to activate the line blanking impulse. If the voltage at the base of Q9 falls short of the voltage over the capacitor C1 then the line blanking impulse is terminated. At this time, the voltage at the base of Q13 is higher by 5 per cent than the voltage over the capacitor C1.

The base of transistor Q20 is clamped with the resistors R7 and R8 to a voltage of 1.3 V. As soon as the positive edge of the flyback impulse passes over the threshold voltage of 1.3 V, the voltage at the resistor R6 is raised via the comparator Q21, Q23. Thus, an image of the phi2 signal emerges at the resistor R6 which lies partly within the line blanking impulse which is to be formed and is derived from a section of the flyback impulse which is guaranteed to be free from ringing.

The difference amplifier Q10, Q13 is supplied with a current of, for example, one micro-ampere, and the capacitor C1 is charged or discharged respectively according to the voltages at the bases of Q10 and Q13 so long as the phi2 signal is not active. A reference voltage adjusts itself via the capacitor C1 during the line trace. This reference voltage is to be maintained during the flyback impulse.

Therefore, the current supply of the difference amplifier Q10, Q13 is switched off when the phi2 signal appears (first point in time). The stored value of the reference voltage over the capacitor C1 could change in the time span between the start of the line blanking impulse and the first point in time. A corresponding alteration can also appear if the second point in time does not exactly coincide with the end of the line blanking impulse. However, due to the steep ascending or, respectively, descending edges of the flyback impulse, the 15 pF capacity for capacitor C1, the small charging current of one micro-ampere and the negligible leakage current of the capacitor C1, the reference voltage stored by the capacitor C1 is advantageously practically unaffected during this short time span.

The two transistors Q3 and Q6 and the two resistors R3 and R4 form a flip-flop which is triggered by the transistor Q5 and by the phil signal via transistor Q1. The phil signal prevents an undesired setting of the line blanking impulse through ringing of the flyback impulse. The line blanking signal is available as an output signal of this flip-flop at the output 24.

The line blanking circuit can be modified accordingly for the processing of an inverted flyback impulse at the input 21.

Claims



1. Self-adjusting line blanking circuit with integrated electronic components for generating line blanking impulses at an output (24), said circuit being fed with line flyback impulses (Fig. 1) at a first input (21) and a first switching signal with line frequency (Φ_{11}) at a second input (22), the first switching edge of said switching signal always lying approximately in the temporal center of the flyback impulses and the second switching edge of it always lying between two flyback impulses, and whereby said circuit evaluates a second switching signal with line frequency (Φ_{12}) whose switching edges always lie, temporally, within the line blanking impulses,
said circuit being provided with comparator means (Q10, Q11, Q13, Q14) connected to memory means (C1), said comparator means comparing a reference value contained in the memory means (C1) against a deviation through the signal progression of the flyback impulses determined by means of generator means (R10, R9), and said circuit comprising blocking means (Q12, R6) connected to the comparator means (Q10, Q11, Q13, Q14) which block an alteration of the reference value between the associated switching edges with the aid of the second switching signal (Φ_{12}), and comprising switching means (R1, Q1, Q3, R3, R4, Q6) connected to the comparator means (Q10, Q11, Q13, Q14) to which a third switching signal, resulting from the deviation from the reference value, and the first switching signal (Φ_{11}) are fed, and which generate the line blanking impulses at their output, whereby in the switching means (R1, Q1, Q3, R3, R4, Q6), additional generation of line blanking impulses owing to repeated deviation from the reference value and dependent on the



ringing at the backward edge of the flyback impulses is suppressed with the aid of the first switching signal (Phi1).

2. Line blanking circuit according to claim 1, characterized in that the memory means contain a capacitor (C1).
3. Line blanking circuit according to claim 2, characterized in that the blocking means (Q12, R6) periodically disconnect the current supply for the comparator means (Q10, Q11, Q13, Q14) and the charging current for the capacitor (C1) correspondingly.
4. Line blanking circuit according to claim 2 or 3, characterized in that the capacitor (C1) is charged mainly during the line trace.
5. Line blanking circuit according to one or more of the claims 1 through 4, characterized in that the second switching signal (Phi2) is obtained using a comparator (Q21, Q23) from the flyback impulses applied to the first input (21), whereby one output of the comparator (Q21, Q23) is connected to the blocking means (Q12, R6).
6. Line blanking circuit according to claim 5, characterized in that a further input of the comparator (Q21, Q23) is connected to the generator means (R10, R9).