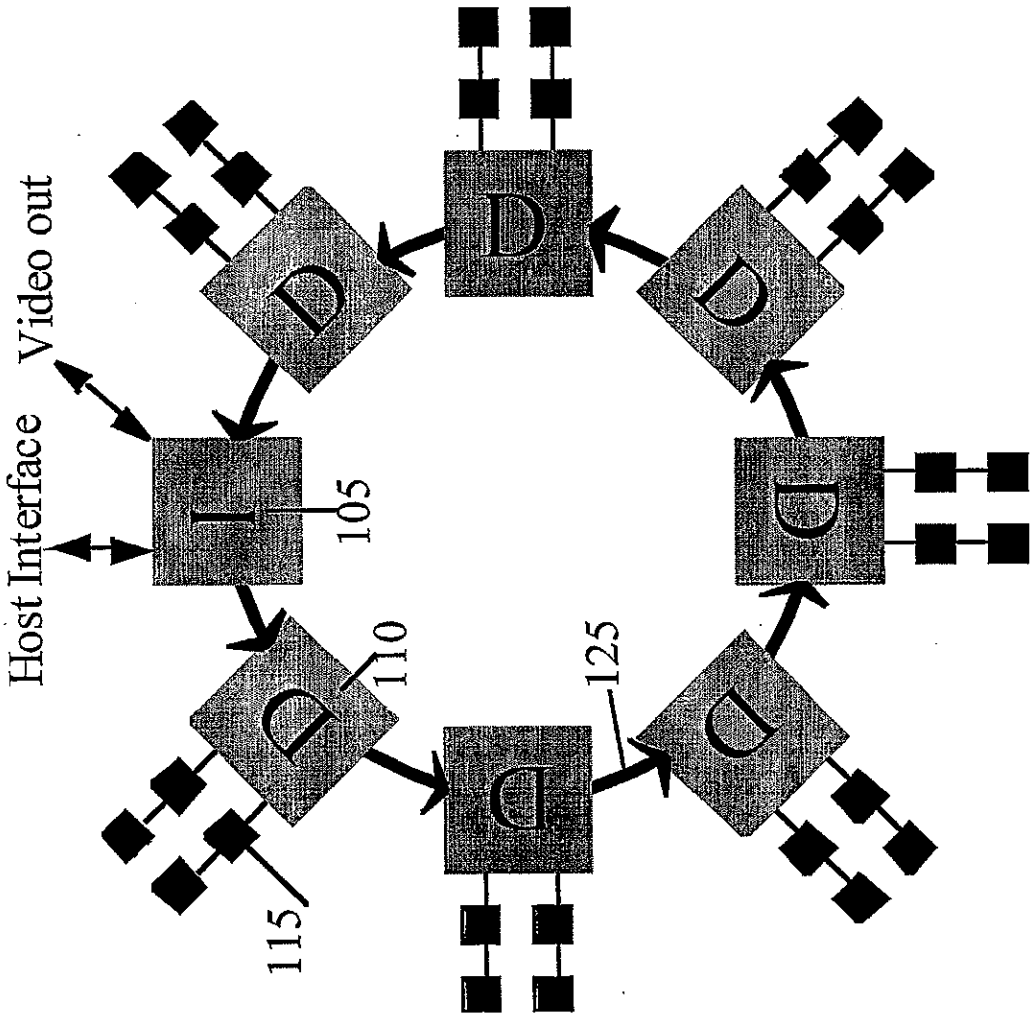


Fig. 1
Basic Loop Architecture Interconnect

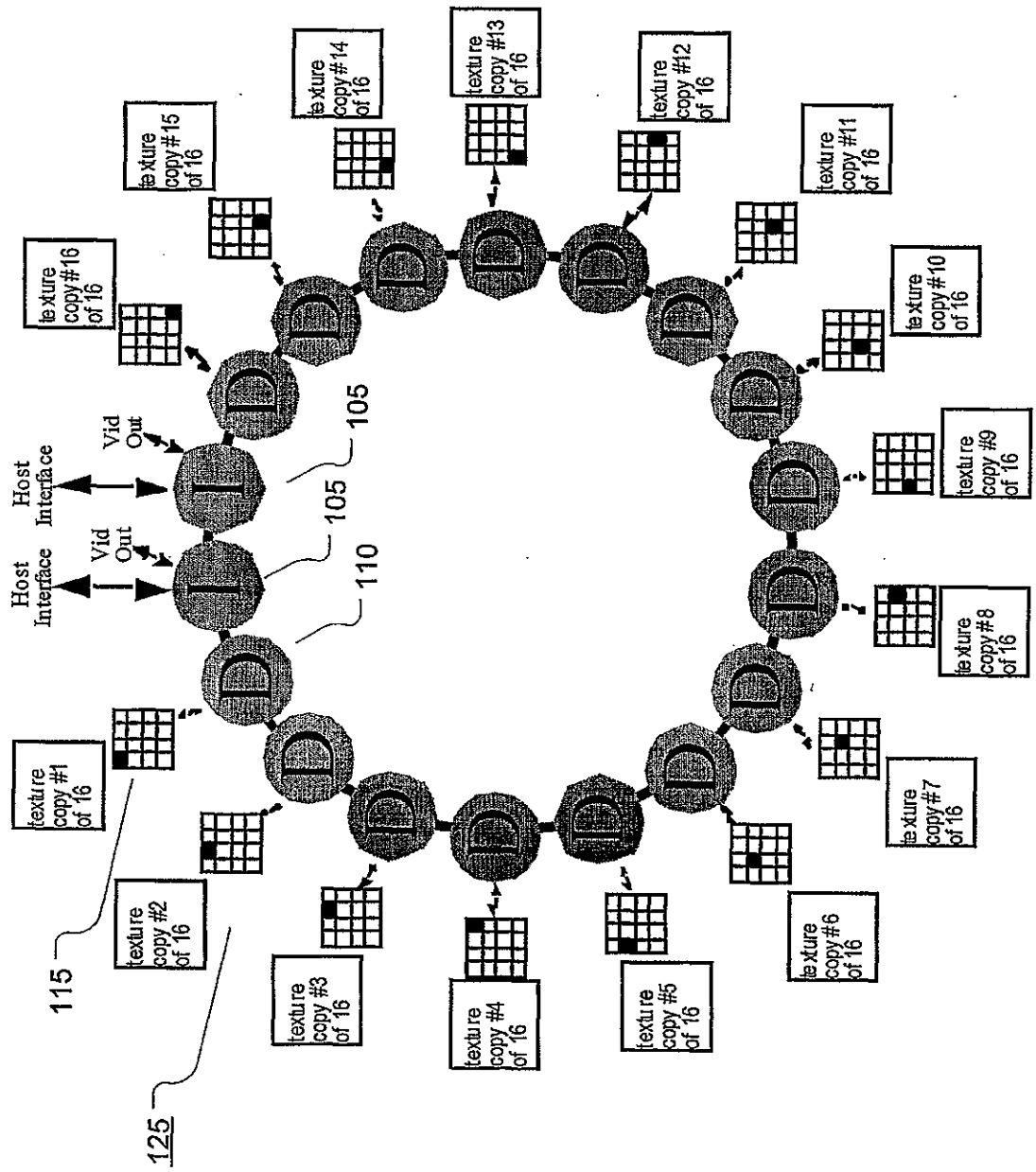


Fig. 2

Texture and Frame Buffer Memory Allocation and Partitioning

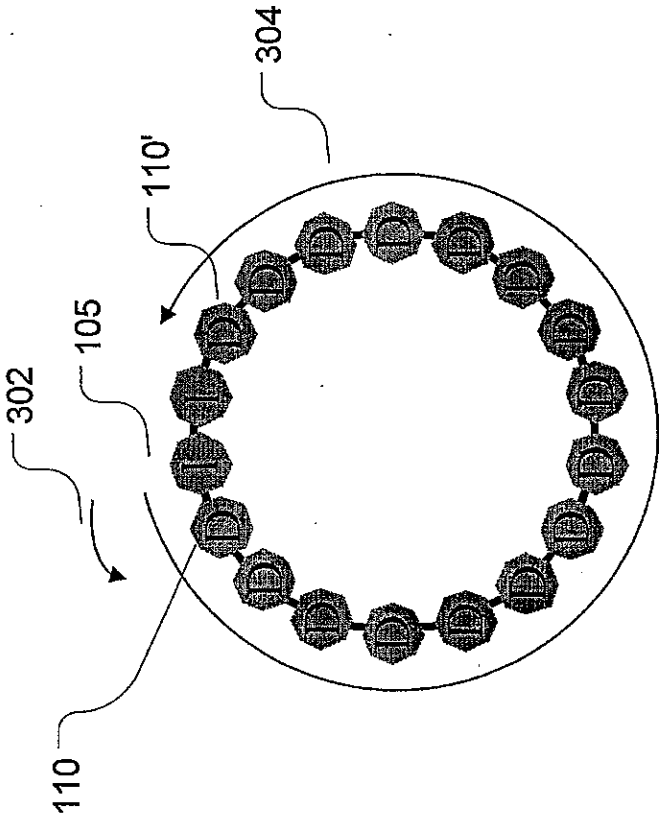


Fig. 3
Longest and Shortest Path of Unicast GraphicsCommand Loop Packets from a LoopInterface Chip to Possible Destination LoopDraw chips

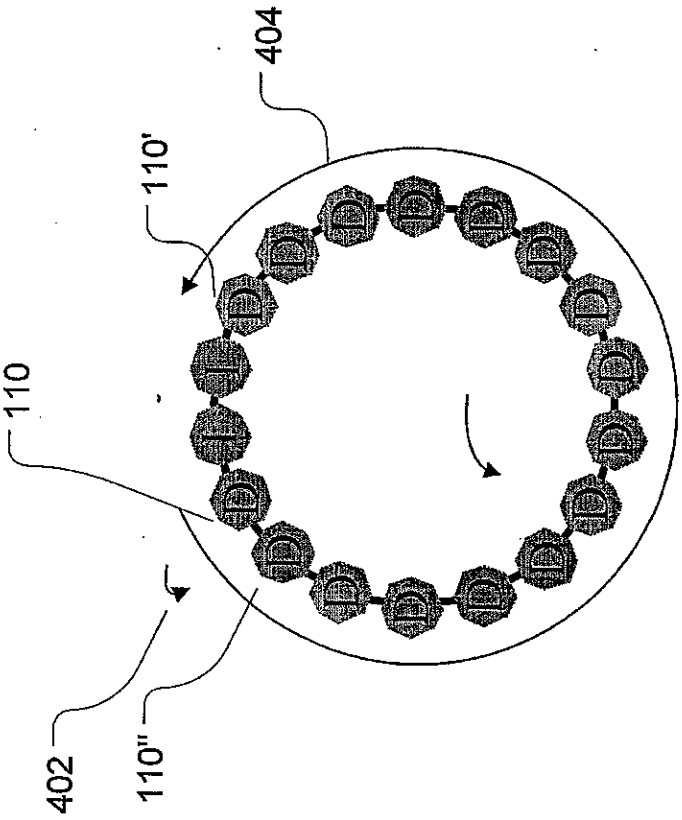


Fig. 4
Longest and Shortest Path of a DrawPixel Loop Packet from a LoopDraw Chip to Possible Destination LoopDraw Chips

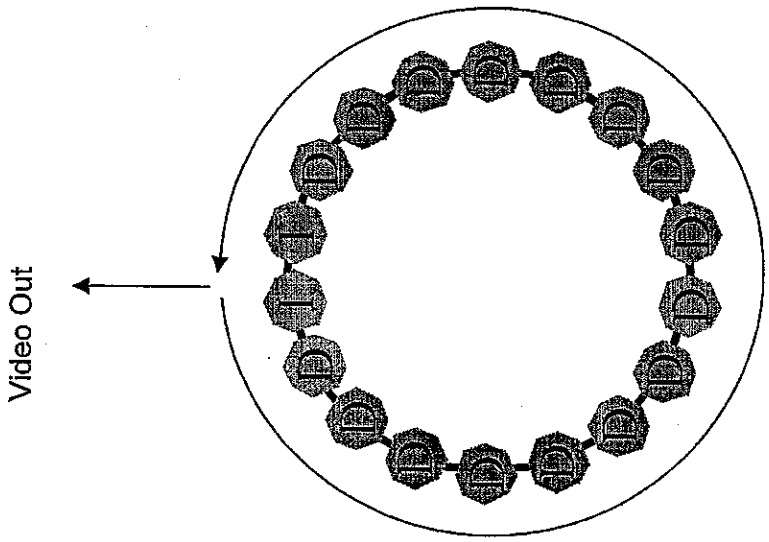


Fig. 5
Path of VideoPixel Loop Packet from a LoopInterface Chip through all the LoopDraw Chips, and Back to the Original LoopInterface Chip

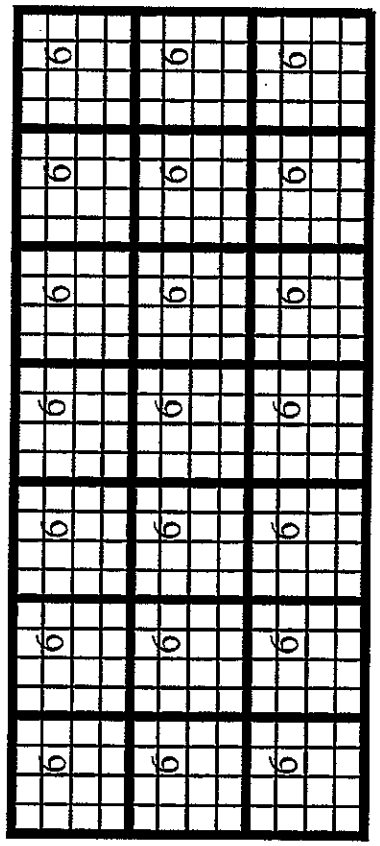


Fig. 6
All the Pixels in a Sixteen LoopDraw chip System
Owned by LoopDraw chip #6 (of 0-15)

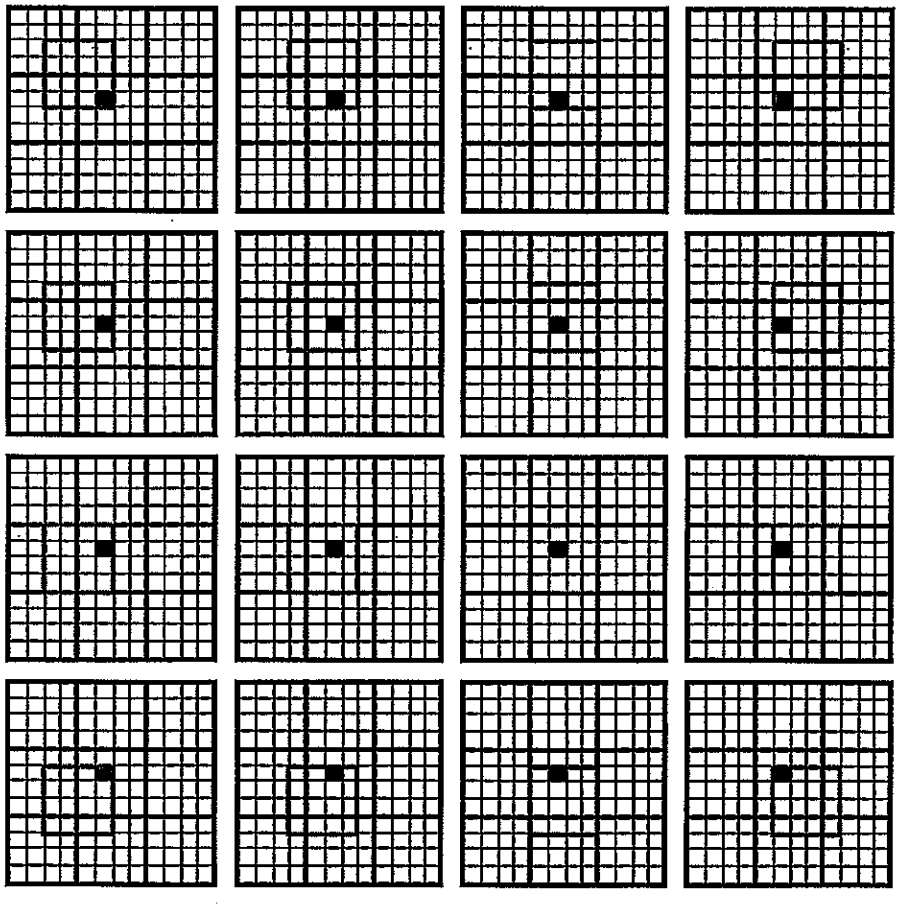


Fig. 7
All Sixteen VideoPixel Loop Packets Whose 4x4 Convolution Windows Require include Processing of one Specific Pixel from LoopDraw chip #6

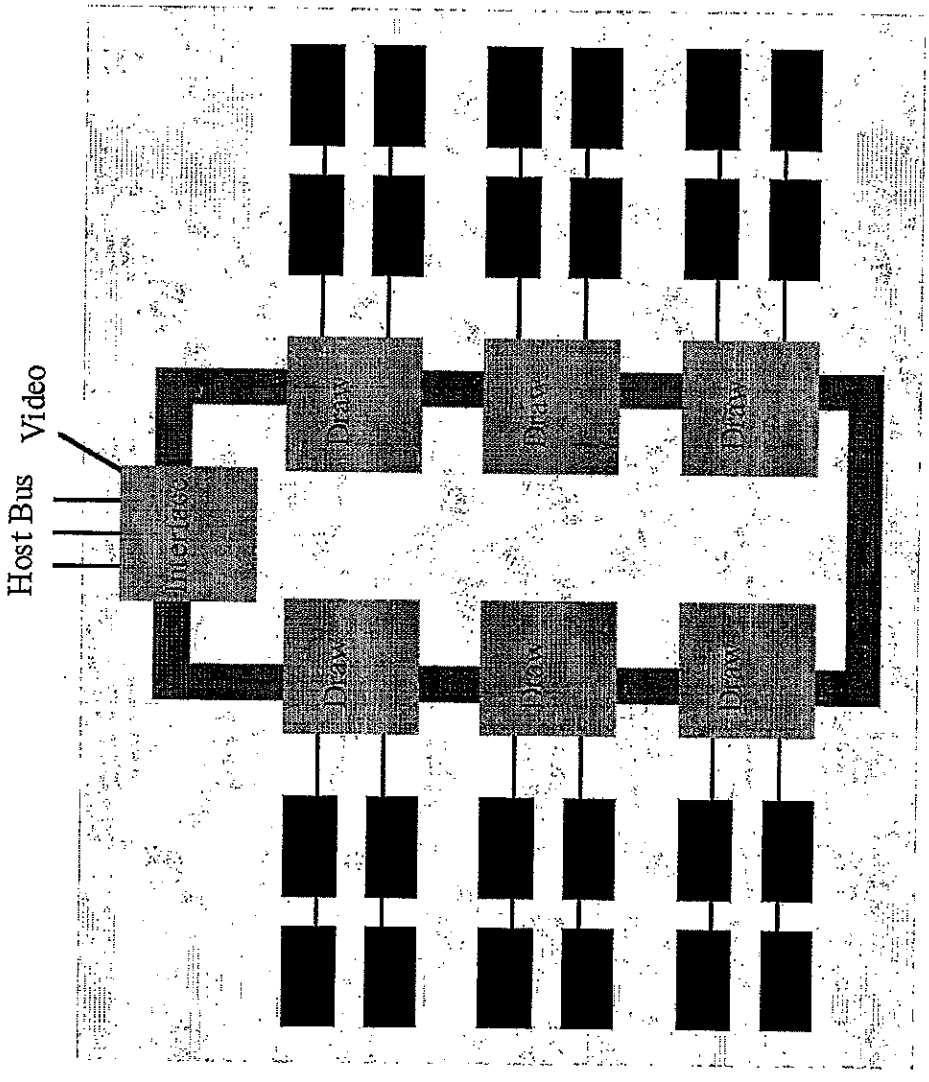


Fig. 8
Six LoopDraw Chip Layout

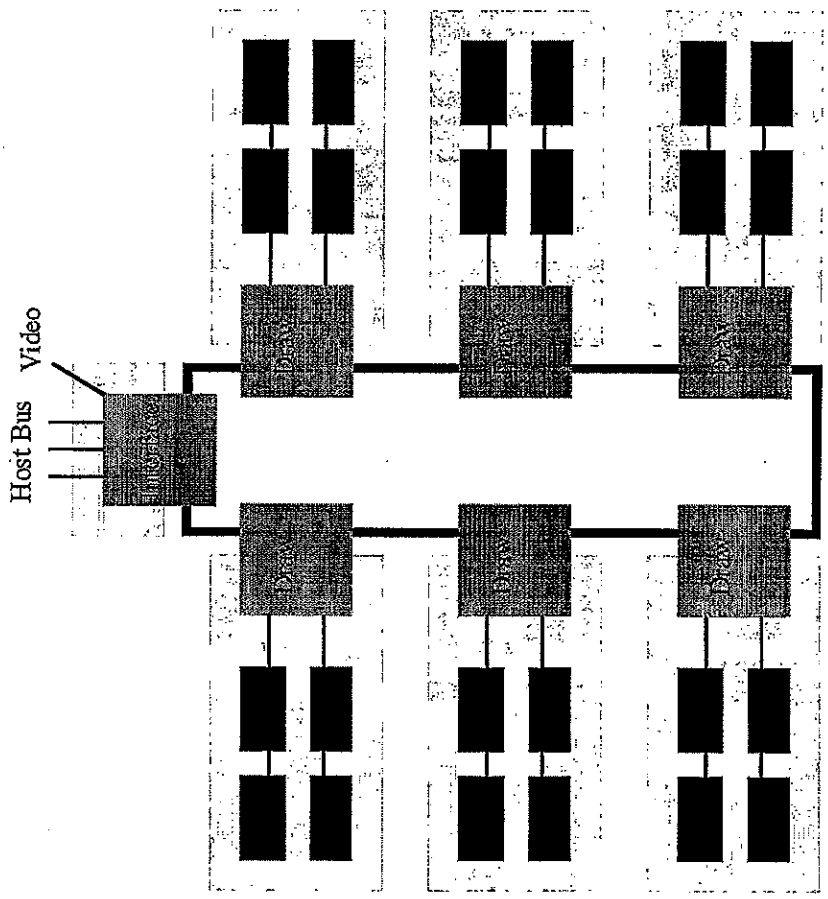
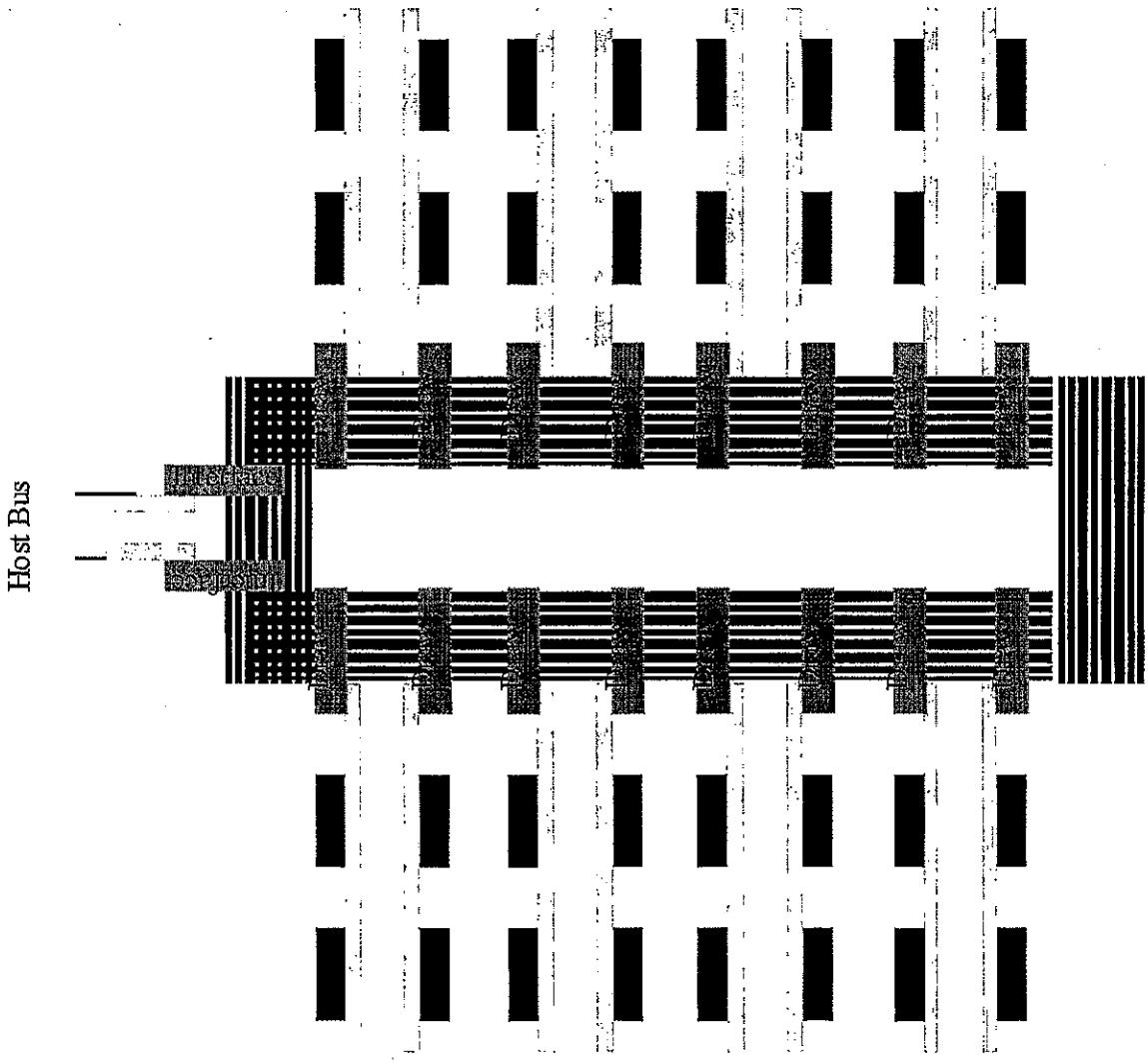


Fig. 9
Six LoopDraw Chip Printed Circuit Daughter Board Layout

Fig. 10
16 LoopDraw, 2
LoopInterface Chip
Printed Circuit
Daughter Board on
Edge Layout



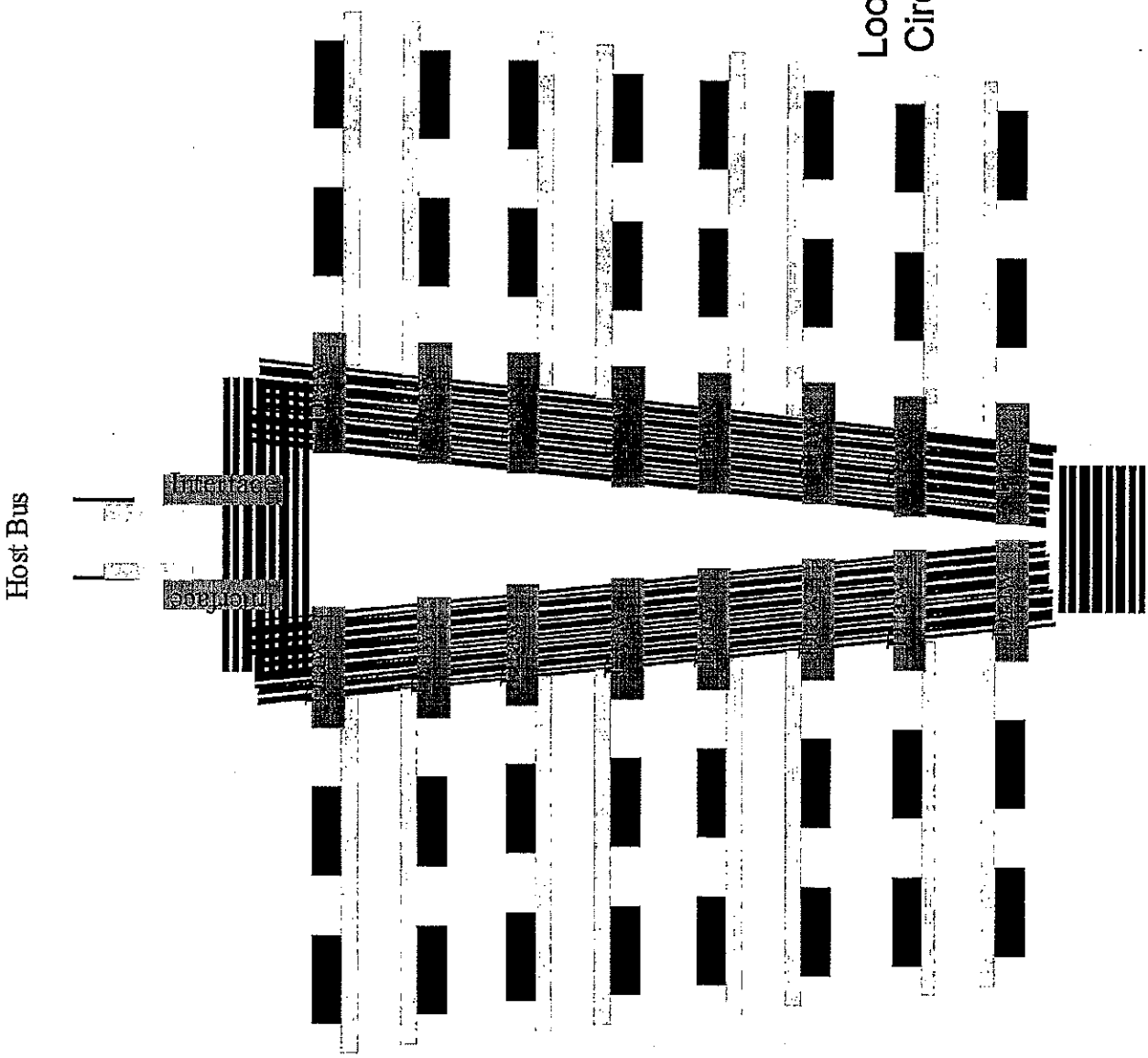


Fig. 11
16 LoopDraw, 2
LoopInterface Chip Printed
Circuit Daughter Board on
Edge 'V' Layout

Fig. 12
16 LoopDraw, 2
LoopInterface Chip
Printed Circuit
Daughter Board Radial
on Edge Layout

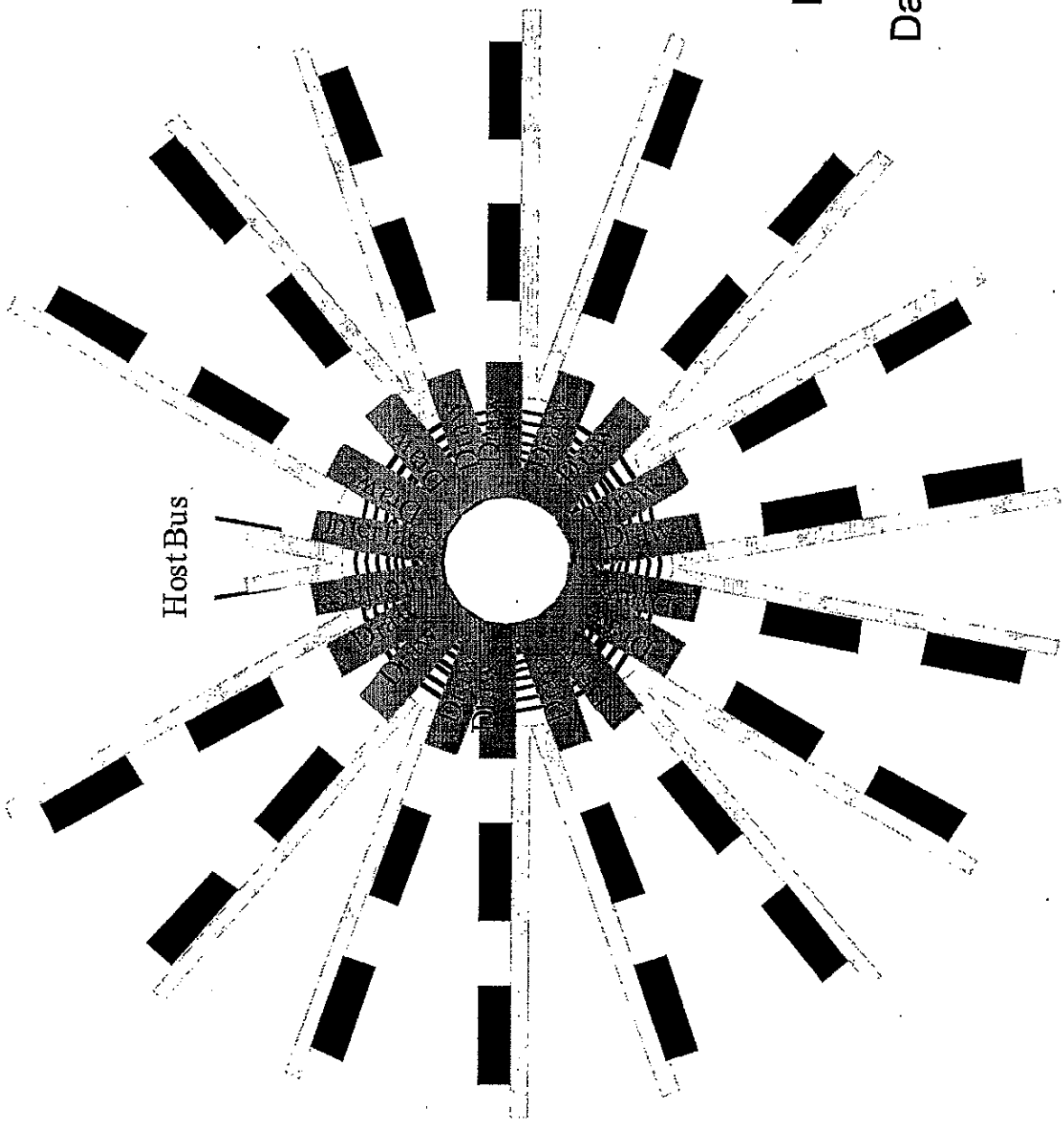


Fig. 13(a)
Positions of Pads on Bottom Side of Chip Package for Flipped Back-to-back LoopLink Connections

Fig. 13(b)
Positions of Pads on Top Side of Chip Package for Flipped Back-to-back LoopLink Connections

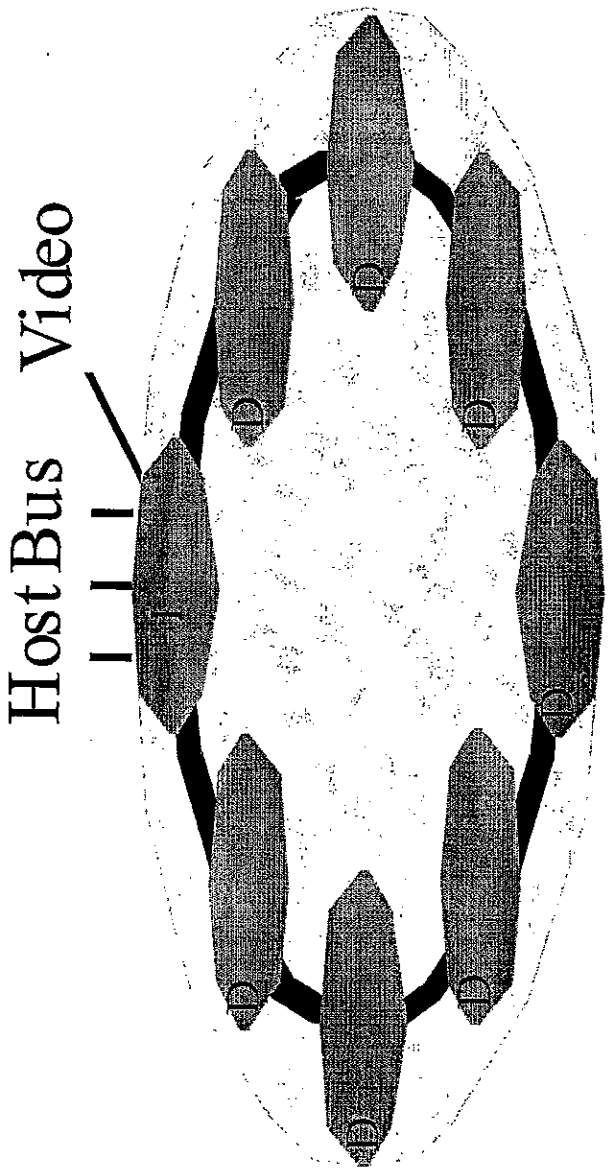


Fig. 14
Single Ring Schematic

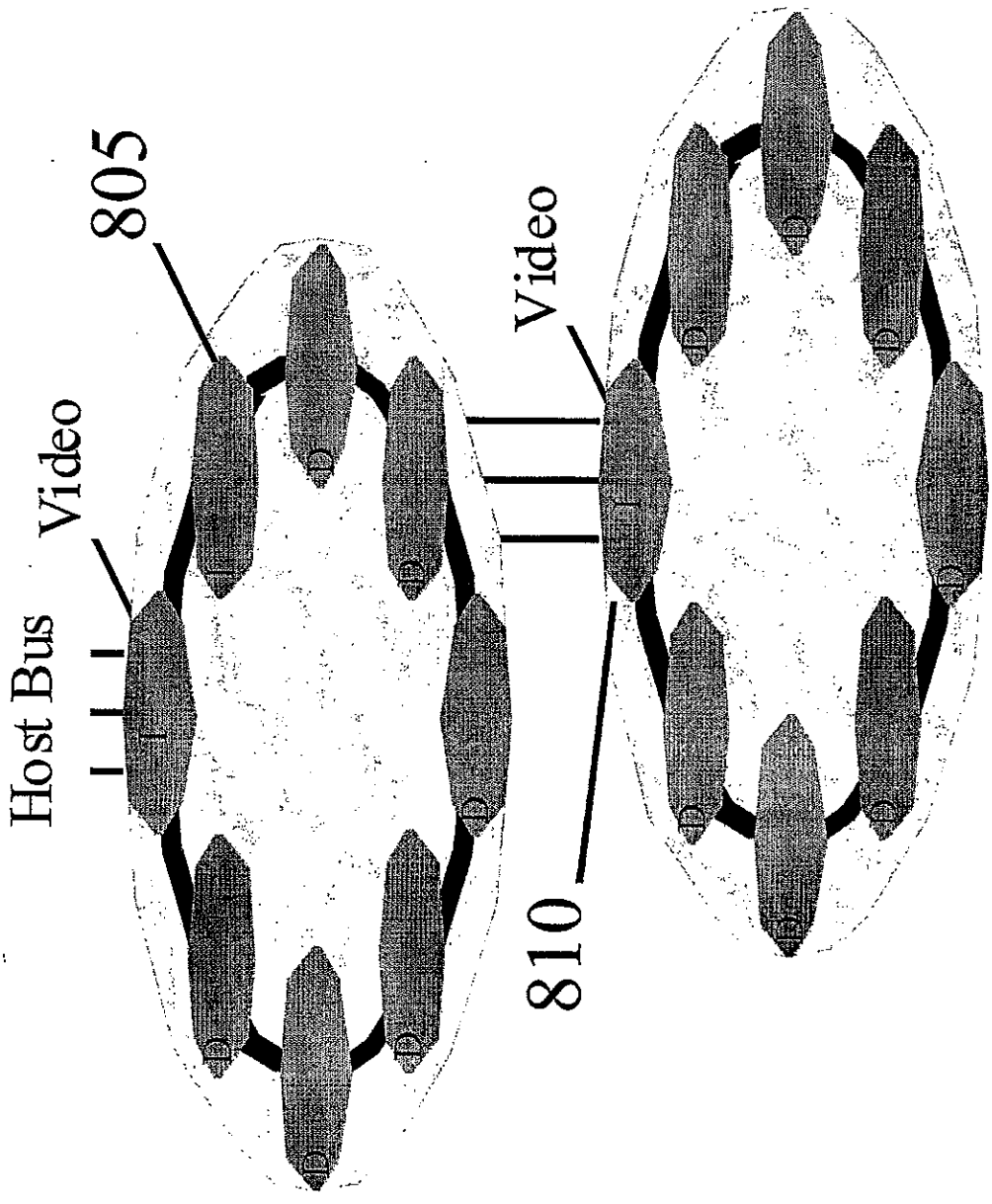
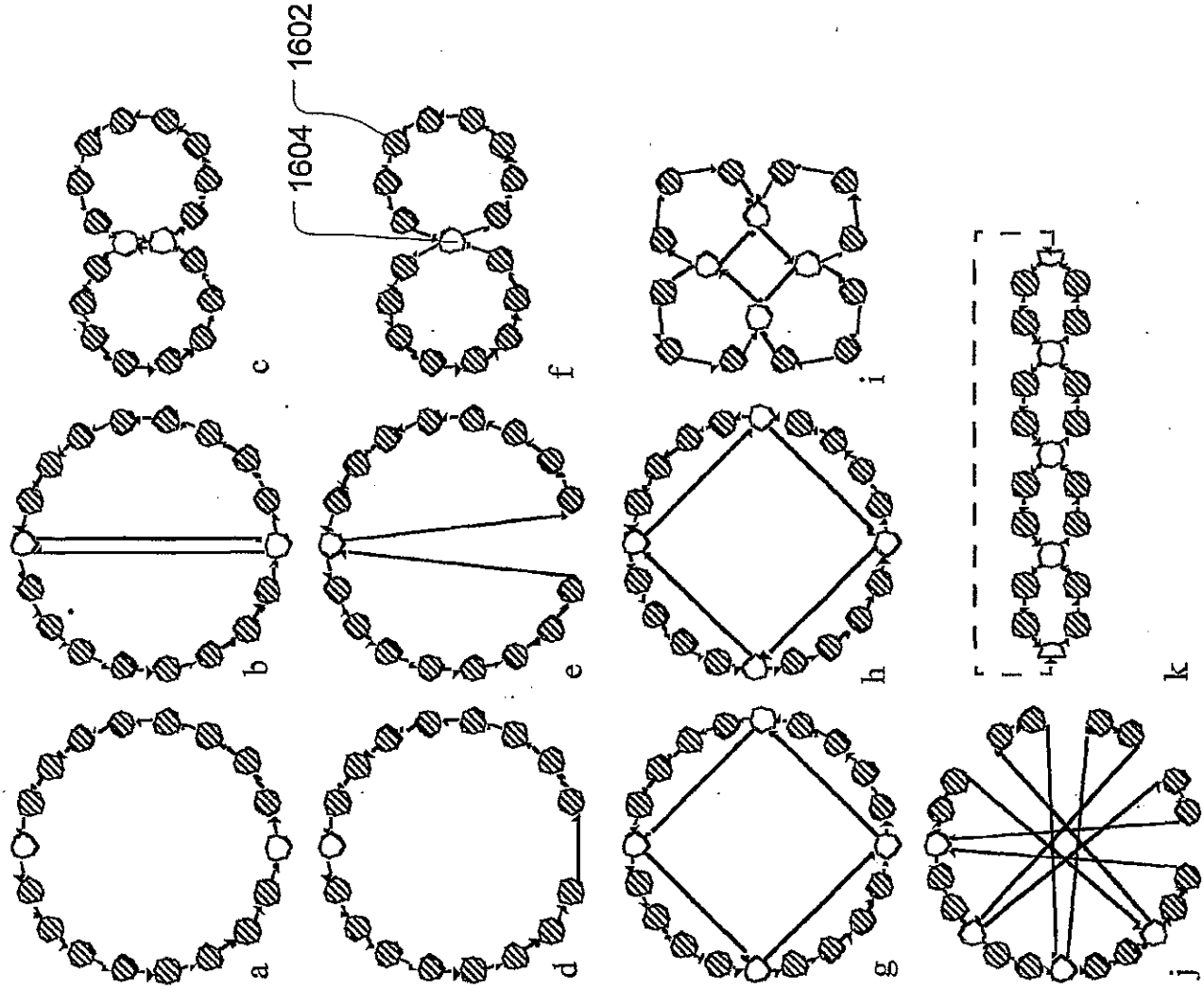


Fig. 15
Double Ring Schematic



Figs. 16(a)-16(k) Different Shortcut Connections, and Different Ways of Drawing the Same Connections.

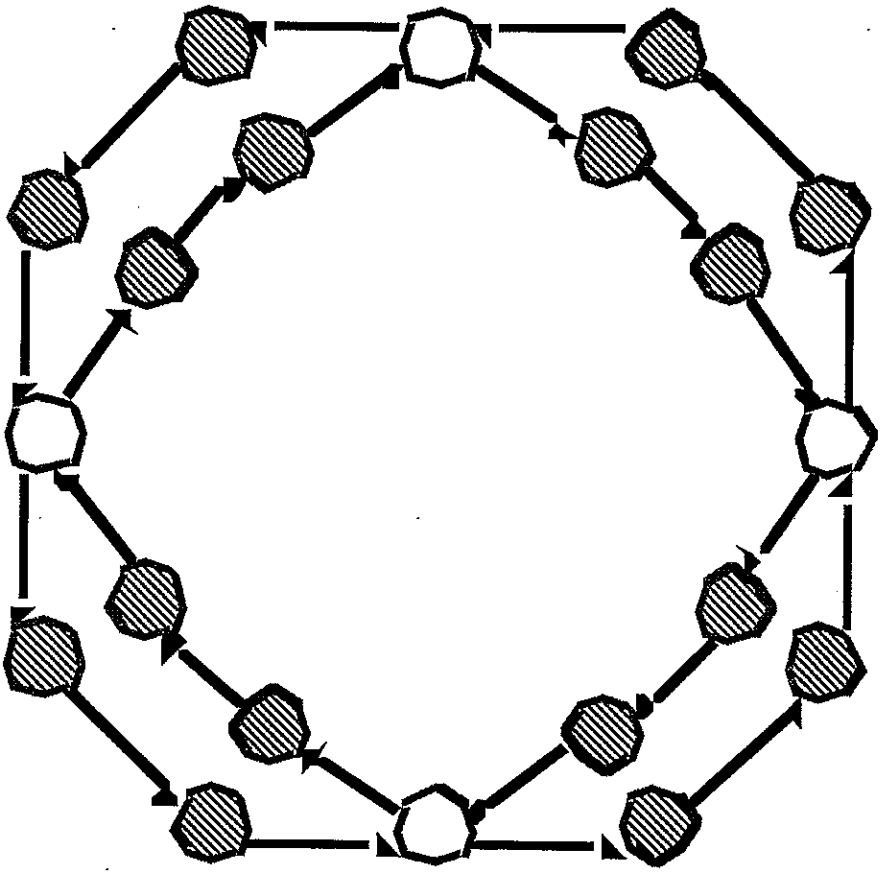


Fig. 17
Redrawing of Fig.16: a Double Simple Ring

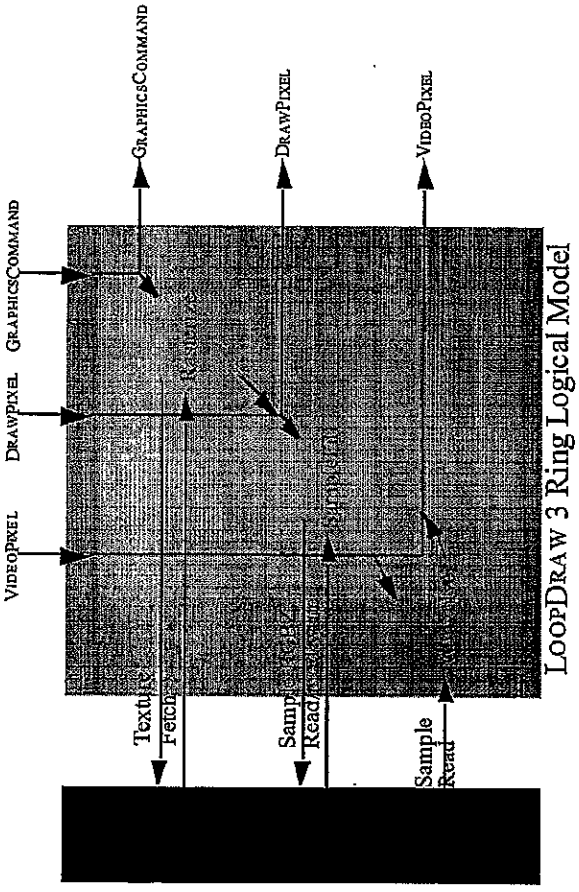


Fig. 18(a)

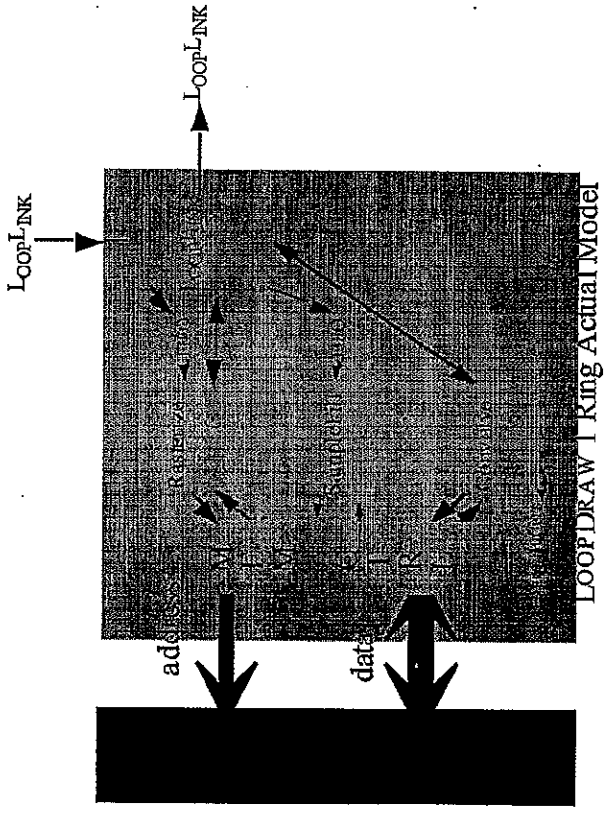


Fig. 18(b)