

MULTIACCUMULATOR SIGMA DELTA FRACTIONAL
N SYNTHESIS

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Abstract of the Invention

10 A fractional-N synthesizer employing at least a second
order sigma-delta modulator is disclosed. The most
significant bits from the output accumulator (1011) of the
sigma-delta modulator are used as the carry out control for
the variable divisor of the loop divider (103). Modulation to the
15 synthesizer is introduced as part of the digital number input
to the sigma-delta modulator and spurious signal output is
realized by selection of a large number as the denominator of
the fractional portion of the loop divider divisor.

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FIG. 9 accompanies this abstract.