

**TITLE OF INVENTION: SHADOW STACK ISA EXTENSIONS
TO SUPPORT FAST RETURN AND EVENT DELIVERY (FRED) ARCHITECTURE**

ABSTRACT

An apparatus and method for efficiently managing shadow stacks. For example, one embodiment of a processor comprises: a plurality of registers to store a plurality of shadow stack pointers (SSPs), each SSP associated with a different event priority; event processing circuitry to select a first SSP of the plurality of SSPs from a first register of the plurality of registers responsive to receipt of a first event associated with a first event priority level, the first SSP usable to identify a top of a first shadow stack; verification and utilization checking circuitry to determine whether the first SSP has been previously verified, wherein if the first SSP has not been previously verified then initiating a set of atomic operations to verify the first SSP and confirm that the first SSP is not in use, the set of atomic operations using a locking operation to lock data until the set of atomic operations are complete, and wherein if the first SSP has been previously verified, then re-verifying the first SSP and confirming that the first SSP is not in use without using the locking operation.

Fig. 1A