

CLAIMS:

1. A package-on-package stacked microelectronic structure, comprising:

a first microelectronic package, comprising a substrate having a first surface and a second surface opposite the first surface, and at least one package connection bond pad formed on the microelectronic package substrate first surface, and having at least one microelectronic device electrically connected to the first microelectronic package substrate first surface;

a second microelectronic package, comprising a substrate having a first surface and a second surface opposite the first surface, and at least one package connection bond pad formed on each second microelectronic package substrate first surface, and having at least one microelectronic device electrically connected to the second microelectronic package substrate first surface, and having at least two microelectronic devices electrically connected to the second microelectronic package substrate second surface, the at least two microelectronic devices co-planar with one another on the second microelectronic package substrate second surface, and the at least two microelectronic devices electrically coupled to the at least one microelectronic device of the second microelectronic package by conductive routes through the second microelectronic package substrate, wherein a first of the conductive routes couples a first microelectronic device of the at least two microelectronic devices to a microelectronic device of the at least one microelectronic device, and a second of the conductive routes couples a second microelectronic device of the at least two microelectronic devices to the microelectronic device of the at least one microelectronic device; and

at least one package-to-package interconnection structure extending between the first microelectronic package connection bond pad and the second microelectronic package connection bond pad.

2. The package-on-package stacked microelectronic structure of claim 1, further including an encapsulation material disposed between the first microelectronic package substrate first surface and the second microelectronic package substrate first surface.

3. The package-on-package stacked microelectronic structure of claim 1, wherein at least one of the first microelectronic package microelectronic device and the second microelectronic package microelectronic device is attached to its respective substrate with a plurality of interconnects in a flip-chip configuration.
4. The package-on-package stacked microelectronic structure of claim 3, further including at least one of a first underfill material disposed between the first microelectronic package microelectronic device and the first microelectronic package substrate, and a second underfill material disposed between the second microelectronic package microelectronic device and the second microelectronic package substrate.
5. The package-on-package stacked microelectronic structure of claim 1, wherein at least one of the first microelectronic package microelectronic device and the second microelectronic package microelectronic device is attached to its respective substrate with a plurality of wirebonds.
6. The package-on-package stacked microelectronic structure of claim 1, wherein a back surface of the first microelectronic package microelectronic device is attached to a back surface of the second microelectronic package microelectronic device with an adhesive material.
7. The package-on-package stacked microelectronic structure of claim 1, wherein the first microelectronic package substrate includes a second surface and the second microelectronic package substrate includes a second surface, and further including a plurality of external bond pads in or on at least one of the first microelectronic package substrate second surface and the second microelectronic package substrate second surface.
8. A method of forming a package-on-package stacked microelectronic structure, comprising:
forming a first microelectronic package, comprising a substrate having a first surface and at least one package connection bond pad formed on each microelectronic

package substrate first surface; electrically connecting at least one first microelectronic device to the microelectronic package substrate first surface;

forming a second microelectronic package, comprising a substrate having a first surface and at least one package connection bond pad formed on each microelectronic package substrate first surface;

electrically connecting at least one second microelectronic device to the second microelectronic package substrate first surface;

electrically connecting at least one third microelectronic device and one fourth microelectronic device to the second microelectronic package substrate second surface, the at least one third and one fourth microelectronic devices coplanar with one another on the second microelectronic package substrate second surface, and the at least one third and one fourth microelectronic devices electrically

coupled to the at least one second microelectronic device of the second microelectronic package by conductive routes through the second microelectronic package substrate, wherein a first of the conductive routes couples a first microelectronic device of the at least one third and one fourth microelectronic devices to a microelectronic device of the at least one second microelectronic device, and a second of the conductive routes couples a second microelectronic device of the at least one third and one fourth microelectronic devices to the microelectronic device of the at least one second microelectronic device;

orienting the second microelectronic package first surface to face the first microelectronic package first surface; and

forming at least one package-to-package interconnection structure between the first microelectronic package connection bond pad and the second microelectronic package connection bond pad.

9. The method of claim 8, wherein forming at least one package-to-package interconnection structure between the first microelectronic package connection bond pad and the second microelectronic package connection bond pad comprises forming a package interconnection material bump on its respective first microelectronic package connection bond pad, forming a package interconnection material bump on the second

microelectronic package connection bond pad, and attaching the first microelectronic package interconnection material bump with the second microelectronic package interconnection material bump.

10. The method of claim 9, wherein forming the package interconnection material bump on its respective first microelectronic package connection bond pad, forming the package interconnection material bump on the second microelectronic package connection bond pad, and attaching the first microelectronic package interconnection material bump with the second microelectronic package interconnection material bump comprises forming a package interconnection solder bump on its respective first microelectronic package connection bond pad, forming the package interconnection solder bump on the second microelectronic package connection bond pad, and reflowing the first microelectronic package interconnection solder bump with the second microelectronic package interconnection solder bump.

11. The method of claim 8, further including disposing an encapsulation material between the first microelectronic package substrate first surface and the second microelectronic package substrate first surface.

12. The method of claim 8, wherein electrically connecting the first microelectronic device to the microelectronic package substrate first surface comprises electrically connecting the first microelectronic device to the first microelectronic package substrate first surface with a plurality of interconnects in a flip-chip configuration.

13. The method of claim 12, further including disposing a first underfill material between the first microelectronic package microelectronic device and the first microelectronic package substrate.

14. The method of claim 8, wherein electrically connecting the second microelectronic device to the microelectronic package substrate first surface comprises electrically connecting the second microelectronic device to the second

microelectronic package substrate first surface with a plurality of interconnects in a flip-chip configuration.

15. The method of claim 14, further including disposing a second underfill material between the second microelectronic package microelectronic device and the second microelectronic package substrate.

16. The method of claim 8, wherein at least one of electrically connecting the first microelectronic device to the microelectronic package substrate first surface and electrically connecting the second microelectronic device to the microelectronic package substrate comprises at least one of electrically connecting the first microelectronic device to the first microelectronic package substrate first surface with a plurality of wirebonds and electrically connecting the second microelectronic device to the second microelectronic package substrate first surface with a plurality of wirebonds.

17. The method of claim 8, further comprising attaching a back surface of the first microelectronic package microelectronic device to a back surface of the second microelectronic package microelectronic device with an adhesive material.

18. The method of claim 8, wherein the first microelectronic package substrate includes a second surface and the second microelectronic package substrate includes a second surface, and further including forming a plurality of external bond pads in or on at least one of the first microelectronic package substrate second surface and the second microelectronic package substrate second surface.

19. A computing device, comprising: a board; and
a package-on-package stacked microelectronic structure attached to the board, wherein the package-on-package stacked microelectronic structure comprises:
a first microelectronic package, comprising a substrate having a first surface and at least one package connection bond pad formed on the microelectronic package substrate first surface, and having at least one microelectronic device electrically connected to the microelectronic package substrate first surface;

a second microelectronic package, comprising a substrate having a first surface and at least one package connection bond pad formed on the second microelectronic package substrate first surface, and having at least one microelectronic device electrically connected to the second microelectronic package substrate first surface, and having at least two microelectronic devices electrically connected to the second microelectronic package substrate second surface, the at least two microelectronic devices co-planar with one another on the second microelectronic package substrate second surface, and the at least two microelectronic devices electrically coupled to the at least one microelectronic device of the second microelectronic package by conductive routes through the second microelectronic package substrate, wherein a first of the conductive routes couples a first microelectronic device of the at least two microelectronic devices to a microelectronic device of the at least one microelectronic device, and a second of the conductive routes couples a second microelectronic device of the at least two microelectronic devices to the microelectronic device of the at least one microelectronic device; and

at least one package-to-package interconnection structure extending between the first microelectronic package connection bond pad and the second microelectronic package connection bond pad.

20. The computing device of claim 19, further including an encapsulation material disposed between the first microelectronic package substrate first surface and the second microelectronic package substrate first surface.

21. The computing device of claim 19, wherein at least one of the first microelectronic package microelectronic device and the second microelectronic package microelectronic device is attached to its respective substrate with a plurality of interconnects in a flip-chip configuration.

22. The computing device of claim 21, further including at least one of a first underfill material disposed between the first microelectronic package microelectronic device and the first microelectronic package substrate, and a second underfill material

disposed between the second microelectronic package microelectronic device and the first microelectronic package substrate.

23. The computing device of claim 19, wherein at least one of the first microelectronic package microelectronic device and the second microelectronic package microelectronic device is attached to its respective substrate with a plurality of wirebonds.

24. The computing device of claim 19, wherein a back surface of the first microelectronic package microelectronic device is attached to a back surface of the second microelectronic package microelectronic device with an adhesive material.

25. The computing device of claim 19, wherein the first microelectronic package substrate includes a second surface and the second microelectronic package substrate includes a second surface, and further including a plurality of external bond pads in or on at least one of the first microelectronic package substrate second surface and the second microelectronic package substrate second surface.