

IMPROVED LASER METALLISATION CIRCUIT FORMATION AND CIRCUITS FORMED THEREBY

Field of the Invention

This invention relates to the formation of circuits through the use of laser metallization, and to circuit structures formed thereby. Applications of the invention include rapid prototyping of printed wire circuits, wafer level chip scale packaging.

Background of the Invention

In some applications it is useful to form circuit interconnections through laser induced metal deposition, rather than other techniques such as sputtering, chemical vapour deposition, masking and etching which is relatively expensive. Laser induced deposition of copper from a metalorganic precursor in gas, liquid film or solid film is known as a promising technique for repair and rapid prototyping of conductive tracks and circuits. For example, US patents 5,378,508 and 4,880,959 and international patent publication WO 92/06782 describe various approaches for circuit formation by laser-assisted copper deposition. However, presently known techniques have several drawbacks that have thus far hindered practical application of the technology. Such drawbacks include limitations in copper adhesion, line resolution and electrical conductivity.

Summary of the Invention

In accordance with present invention, there is provided a method of forming circuit interconnections on a substrate, including:

directing a laser beam to trace a predetermined circuit interconnection pattern on a surface of said substrate to thereby effect laser-induced deposition of a seed metal layer in said predetermined circuit interconnection pattern on said substrate surface; and

performing electroless metal plating on said seed metal layer to form said circuit interconnections on said substrate.

One form of the invention includes applying a metalorganic film to said substrate surface, wherein the laser-induced deposition comprises heating of selected portions of the

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metalorganic film with said laser beam so as to cause thermal decomposition thereof according to said predetermined circuit interconnection pattern.

Preferably the remainder of the metalorganic film is removed from the substrate
5 following the laser induced deposition process.

In a preferred implementation the metalorganic film comprises a film of copper formate.

10 Another form of the invention involves laser-catalyzing of selected portions of said substrate surface and application of a metal electrolyte solution to the laser-catalyzed substrate surface.

The substrate might comprise a circuit board, for example, or may comprise an
15 integrated circuit wafer. In the case of an integrated circuit wafer or die, the method of a preferred embodiment can be used to perform water level chip scale packaging (WLCSP).

In accordance with the present invention, there is also provided a method of forming circuit interconnections on a substrate, including:

20 directing a laser beam to trace over selected portions of the substrate to activate a predetermined circuit interconnection pattern on a surface of said substrate;

forming a metallic circuit interconnection seed layer on said substrate surface corresponding to said predetermined circuit interconnection pattern; and

depositing metal onto said circuit interconnection seed layer in an electroless
25 plating process.

The present invention further provides a method of forming I/O contacts on an integrated circuit wafer, the integrated circuit wafer having a passivation layer with apertures formed therein at which contact pads for integrated circuits on the wafer are
30 exposed, the method including:

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forming a metallic seed layer on the wafer by laser-induced metal deposition, the seed layer being formed in a predetermined circuit connection pattern between respective said contact pads and I/O contact locations;

5 depositing a second metal layer onto said seed layer using an electroless metal plating process; and

forming I/O contacts at said I/O contact locations, wherein said seed layer and said second metal layer provide electrical interconnection between the I/O contacts and respective integrated circuit contact pads.

10 In one form of the invention the laser-induced metal deposition includes applying a metalorganic precursor film over said wafer passivation layer, effecting thermal decomposition of selected portions of the precursor film according to the predetermined circuit connection pattern using a laser beam, and removing the remainder of the precursor film.

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In another form of the invention the laser-induced deposition comprises applying an organic passivation layer to said wafer, laser-catalyzing selected portions of said organic passivation layer surface and application of a metal electrolyte solution to the laser-catalyzed surface so as to form metal deposits thereon according to said
20 predetermined circuit connection pattern.

A preferred implementation includes application of an organic passivation layer to the wafer prior to said laser-induced metal deposition, the organic passivation layer being patterned for exposure of said contact pads.

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A second passivation layer may be applied said electroless metal plating process, the second organic passivation layer being patterned for exposure of said second metal layer at said I/O contact locations.

30 Preferably the said I/O contacts comprise solder bumps formed at said I/O contact locations on the wafer.

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There is also provided, in accordance with the present invention a circuit board including a substrate having a dielectric substrate surface, the circuit board further including a first metallic seed layer on said substrate surface in a predetermined circuit interconnection pattern, the seed layer being formed by laser-induced metal deposition, and
5 a second metal layer deposited on said seed layer by electroless metal plating.

Brief Description of the Drawings

The invention is described in greater detail hereinafter, by way of example only, through description of a preferred embodiment thereof and with reference to the
10 accompanying drawings, in which:

Figure 1 is a flowchart diagram illustrating a general circuit formation process according to an embodiment of the present invention;

Figure 2 is a series of diagrammatic cross-sectional views of circuit element
15 formation on a substrate corresponding to the process steps of Figure 1;

Figure 3 is a graph of laser transmission through copper formate film of various laser wavelengths;

Figure 4 is a graph of circuit track width against laser beam scanning speed;

Figure 5 is a diagrammatic plan view of a fabricated integrated circuit die showing
20 contact pads therefor;

Figure 6 is a diagrammatic plan view of the integrated circuit die with a redistribution metal layer formed thereon;

Figures 7 to 14 are cross-sectional diagrams illustrating the formation of circuit interconnections on an integrated circuit die for water level chip scale packaging; and

25 Figure 15 is a flow chart diagram of a procedure for water level chip scale packaging according to an embodiment of the present invention.

Figure 16 shows an example of a conductive circuit formed in accordance with the present invention.

30 Detailed Description of the Preferred Embodiments

Embodiments of the present invention provide a laser metallisation process that is

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useful in rapid prototyping of printed wire circuits, circuit repair, mask making and repair, and devices requiring in-mould circuits. The laser metallisation process can also be applied to wafer level chip scale packaging (WLCSP), to produce an improved WLCSP that facilitates standard surface mount technology (SMT) without under fill material
5 between chip and substrate. The basic process for circuit formation by way of laser metallisation is illustrated in Figures 1 and 2.

Figure 1 is a flow chart diagram illustrating a general circuit formation process 10 according to an embodiment of the present invention. Figure 2 illustrates a series of
10 diagrammatic cross-sectional view of circuit element formation on a substrate 30 corresponding to the process steps of Figure 1. The substrate 30 provides a base upon which circuit interconnections are to be formed. The substrate 30 may be of any suitable construction, such as those materials known for use in printed circuit boards, or the passivation layer of an integrated circuit die in the case of implementation for wafer level
15 chip scale packaging.

The substrate surface is preferably treated to facilitate adhesion of metal deposits thereto, such as by plasma, chemical and/or ultrasonic rinsing of the substrate surface before application of a precursor film as described below. As water has a very high
20 surface tension, achieving a uniform coating of a water-based precursor film solution such as copper formate can be difficult. Surface cleaning and pretreatment of the substrate using detergents, chemicals or plasma before applying the solution onto the substrate are found to improve the wettability and thus the film adhesion to the substrate.

25 A liquid precursor film 32 is applied to the surface of the substrate 30, at step 12 in process 10. In the preferred embodiment the liquid precursor comprises a metal organic solution such as copper formate. An appropriate metallorganic solution may be prepared by dissolving 1.25g commercially available copper formate ($\text{Cu}(\text{HCOO})_2 \cdot 2\text{H}_2\text{O}$, Aldrich Chemical) into 10ml deionised water. (The solubility of copper formate is 12.5 g in 100
30 ml DI water). A small amount (0.5-1ml) of 10% glycerol is then added in the solution to avoid the formation of copper formate crystals in the film (anti-crystallisation). Spin

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coating, spraying or brushing technique may be used to apply the solution onto the substrate. An amorphous (paste-like or solid) copper formate film 34 is formed on the substrate 30 (step 14) after baking in an oven at 70 – 75°C for about 30 minutes or drying by hot air to partially remove the water.

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Following formation of the precursor film 34 on the substrate 30, a circuit pattern is written on the film using a computer controlled laser (step 16). The circuit pattern traced by the laser beam may be controlled according to a CAD circuit configuration, for example. The action of the laser beam effects laser thermal decomposition of the copper formate film, leaving a copper track 36. The deposited copper 36 provides a seed layer for the circuit formation on the substrate 30.

In prior art laser metallisation processes, scattered copper deposits are normally found around the deposited lines due to non-uniform beam profiles. This is a major concern as the scattered deposits are causes of faulty circuits, and places limitations on the line/spacing design. Process studies have been carried out using different laser wavelengths to address the above issues. It is found that the fundamental Nd: YAG laser at the wavelength 1064 nm and its 2nd harmonic at the wavelength of 532nm performed the best.

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A study of optical transmission of the copper formate film with respect to laser wavelengths revealed that both the 1064 nm beam and the 2nd harmonic green beam (532nm) transmit the majority of the beam energy. As the laser beam has a near Gaussian beam profile, only the central portion of the beam has sufficient energy to decompose the copper formate. The resulting copper line is thus clean (no scattered copper deposits after water rinsing) and narrower. The line width is further controlled by the film thickness (thinner film leads to finer lines) and the beam scan speed (higher speed leads to finer lines).

30 2nd harmonic ND:YAG laser

The laser beam has a wavelength of 532nm. Under the following conditions, the

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laser beam irradiates on the substrate and heats it up to the decomposition temperature of the copper formate (around 200°C). Copper deposits on the substrate. The laser parameters are: average power=2.5 W, Repetition rate 10KHz, and beam scanning speed = 1mm/s. The remaining copper formate film is then dissolved by rinsing the substrate in
5 water or diluted formic acid.

Fundamental Nd:YAG laser

The laser beam has a wavelength of 1064nm. Under the following conditions, the laser beams irradiates on the substrate and heats it up to the decomposition temperature of
10 the copper formate (around 200°C). Copper deposits on the substrate. The laser parameters are: average power = 2.5 W, repetition rate = 20KHz, and beam scanning speed = 10mm/s. The remaining copper formate film is then dissolved by rinsing the substrate in water or diluted formic acid.

15 Figure 3 is a graph of laser transmission through copper formate film according to various laser wavelengths. As shown in the graph, the copper formate is fairly transparent to both the laser radiation at 1064 nm and 532 nm. It is seen that the 2nd harmonic Nd:YAG laser beam at the wavelength of 532 nm transmits about 90% of the beam through the copper formate film, whereas about 80% of the 1064nm beam can be
20 transmitted. Therefore, the absorption coefficient of the substrate controls the temperature rise and distribution, which in turn controls the decomposition process of the copper formate film. The transmission curve also implies that a thick film can be used to produce thick copper deposits with both laser beams.

25 Testing of laser thermal decomposition of copper formate (or other metalorganical films) has revealed the following conditions that may be applied in implementing embodiments of the present invention.

Other processing parameters can also effect the achievement of narrow clean
30 deposited copper lines. For example, increasing the scanning speed of the laser beam generally leads to reduced line width. This is illustrated in the graph shown in Figure 4,

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which indicates copper track width obtained at various laser scanning speeds, using a 532nm laser beam.

It is also possible to form the metal seed circuit layer on the substrate using laser assisted copper deposition from solution. For example, it is possible to form circuit interconnections using laser assisted copper deposition on polyimide substrate from copper electrolyte solution, such as a commercially available Coppermerse solution from LeaRonol. A 532nm pulse-mode Nd:YAG laser can be used instead of CW Ar⁺ laser for the process. In testing, the deposition process was initiated by laser-catalyzing of the polyimide surface and a photothermal reaction of a tartarate-complex solution of Cu²⁺ ions in an alkaline and reducing environment. The dependence of the characteristics of deposited copper line on the laser Q-switch frequency, scanning speed of the laser beam, and scanning times was investigated, and the optimum laser conditions were found to be I=31A, Scanning speed: 0.01mm/s-0.06mm/s, and Rep. Rate: 10K-40K.

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Referring again to Figures 1 and 2, where a circuit pattern is written on a precursor film such as copper formate, it is desirable to remove the remainder of the film before further processing. This is achieved at step 18, where the portion of the precursor film not exposed to the laser beam is dissolved by rinsing the substrate in water or diluted formic acid. This leaves only the circuit interconnection seed tracks 36 formed on the substrate 30, as illustrated in Figure 2.

The following removal of the excess precursor film, circuit interconnection tracks are built upon the seed layer 36 using an electroless plating process, depositing copper or nickel, for example. This process step is illustrated at step 20 in Figure 1, and correspondingly the electroless copper plating layer 38 is shown formed on substrate 30 in Figure 2. The copper 36 deposited at step 16 acts as a seeding layer for the further electroless copper or nickel plating, which provides additional interconnection layer thickness and electrical conductivity. Using the electroless plating process, the interconnection tracks can be formed having a thickness range from 5 micrometres to 10 micrometers, with electrical conductivity of the order of 5 μ Ohms-cm, that is sufficiently

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low for practical purposes.

The recent emergence and rapid growth of array packaging such as chip-scale packaging (CSP) and flip chip (FC) technologies open new pathways for electronic packaging that promise profound change the design and manufacturing of integrated circuits. IBM introduced flip chip into manufacturing during the early 1960's primarily as a solution for what at the time seemed like intractable problems that had beset wire bonding. While the idea of using a solder to solve the interconnect reliability problems associated with this direct connection technology was also realised area array connections.

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According to one definition "CSP is categorised as semiconductor chip structures that have been ruggedized to facilitate the ease of chip handling, testing and chip assembly. The CSP have common attributes of minimal size, no more than 1.2X the area of the original die size, and are direct surface mountable". US Patent 6,138,348 and US Patent 5,776,796 shows the cross section of CSP packages using redistribution and flex interposer from Flip Chip Technologies and Tessera respectively. Array packaging technologies shrink the package to the size of the die itself allows the package to be fabricated on the wafer before dicing. Wafer Level Packaging (WLP) allows IC components to be shipped directly from the fab fully tested, packaged and ready for mounting by standard surface mount or flip chip bonding technique.

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A particularly advantageous implementation of the circuit interconnection formation technology of the present invention involves the formation of circuit interconnections for wafer level chip scale packaging (WLSCP). This enables the production of integrated circuit dies with interconnections for standard surface mount technology without under fill material between the chip and substrate. The improved WLCSP enables reduction of investment cost in fabrication equipment, in that the redistribution layer and interconnections can be deposited without the need of vacuum coating equipment such as evaporator, sputter machine and chemical vapour deposition apparatus. Furthermore packaging size of the integrated circuit is reduced to the original bare integrated circuit die, which has hitherto been unachievable.

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Figure 15 is a flow chart diagram of the preferred WLSCP process according to 200, according to an embodiment of the present invention. The process begins at 202 with a fabricated integrated circuit die or wafer having a passivation layer formed thereon to protect the integrated circuit but having apertures formed therein to expose the contact pads. At 204 an organic passivation layer is applied over the existing passivation layer of the integrated circuit in order to improve adhesion for the interconnection layer. The organic passivation layer is patterned so as to expose the contact pads. A precursor film, such as a metalorganic film is applied over the organic passivation layer at step 206. Selected portions of the precursor film are caused to undergo thermal decomposition, so as to form copper interconnection tracks according to a desired circuit interconnection pattern. This is performed at 208 of the process 200, according to the laser writing processes described hereinabove. The remainder of the precursor film is then removed, leaving a metal seed layer on the integrated circuit die/wafer according to the desired circuit interconnection pattern (step 210).

Following formation of the metal seed layer (210), an electroless metal plating process is utilised (step 212) to deposit an additional thickness of conducting metal onto the seed layer circuit interconnection pattern. Another organic passivation layer is then applied and patterned (214) leaving exposed I/O contact openings to portions of the electroless metal layer. A second electroless metal plating process is employed at 216 to apply additional metal at the exposed I/O contact opening. This is followed by an immersion gold layer applied at 218 over the electroless metal portions at the I/O contact openings. Finally, interconnection pads in the form of solder bumps are applied over the I/O contact metal portions, using the screen printing techniques or the like.

Details of the WLCSP process according to the preferred embodiment of the present invention are presented hereinbelow with reference to Figures 5 to 14.

Figure 5 illustrates a plan view of a fabricated integrated circuit 50 having a plurality of contact pads 102. The contact pads 102 may be aluminium, aluminium alloys

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(typically Al/Cu0.5 or Al/Si0.5/Cu0.5) or copper or other suitable materials. The contact pads are typically spaced peripherally along the four sides of the chip 50. The pitch of the contact pads may be of the order of 100 microns.

5 Figure 7 is a cross-sectional view through 7-7 of the chip 50 illustrating an integrated circuit wafer or die 100 having contact pads 102 and a passivation layer 104. A conventional integrated circuit packaging might involve mounting the integrated circuit 50 to a lead frame or the like with gold wires being coupled between respective contact pads and external leads. Then, the integrated circuit and inner portions of the lead frame may be
10 encapsulated in a plastics material, for example, with ends of the leads extending therefrom. The WLCSP construction of the preferred embodiment, on the other hand, involves the formation of interconnection pads (e.g. solder bumps) directly on the integrated circuit chip, with connecting tracks coupling respective contact pads and interconnection pads. This arrangement is illustrated in Figure 6, which shows the chip 50
15 having interconnection pads 122 formed thereon and coupled to the contact pads 102 by interconnection tracks 112.

As shown in Figure 7, the passivation layer 104 is patterned to expose the pads 102. The passivation layer apertures can be round or square shape. The passivation layer may
20 be silicon nitride or silicon oxide layer, for example, patterned with reactive ion etching or other techniques.

An organic passivation layer 106 is formed on the surface of passivation layer 104, as shown in Figure 8. The organic passivation layer is preferable to improve adhesion
25 between the adjacent layers. The organic passivation layer may include Benzocyclobutene (BCB) or polyimide or other suitable materials. As shown in Figure 8, the passivation layer 106 is patterned to expose the contact pads 102. The organic passivation layer 106 such as BCB and polyimide can be prepared by spin coating the liquid photoimageable materials on the passivation layer 104. The liquid photoimageable materials are baked to evaporate the
30 solvent and followed by photolithography process to pattern the apertures on the contact pads. Further curing forms the organic passivation layer.

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As shown in Figure 6, the redistribution of the electrical connections is formed inward from the contact pads 102. To form the redistributed electrical connections layer, a copper formate dry film 108 is formed on the organic passivation layer as described previously and shown in Figure 9. A laser writing process described hereinabove may be used to transform the selected portions of copper formate dry film 108 to a copper seed layer 110. Figure 10 illustrates the copper seed layer 110 after removal of the remaining film. Electroless copper plating process is performed to deposit a copper layer 112 on the seed layer 110 to reach thickness of around 5 micron as shown in Figure 11.

Another organic passivation layer 114 is then formed on the surface of the die. The organic passivation layer 114 can include BCB or polyimide or other suitable materials. As shown in Figure 12, apertures 116 are patterned in the passivation layer 114 to expose portions of the electroless metal plate 112 for interconnection pads 122. The passivation layer apertures 116 can be any described shape such as round or square. The organic passivation layer 114 such as BCB and polyimide can be prepared by spin coating the liquid photoimage materials on the passivation layer 114. The liquid photoimageable materials are baked to evaporate the solvent and followed by photolithography process to pattern the apertures 116 for the interconnection pads. Further curing forms the organic passivation layer. The organic passivation layer can be formed with thickness range from 5 to 40 microns, for example.

As shown in Figure 13 nickel under-bump metallization 118 can then be deposited in an electroless process to provide sufficient adhesion for interconnection pad solder bumps while protecting the copper redistribution tracks. The electroless nickel portions 118 also serves as a barrier layer to prevent copper diffusion in the solder bumps. Electroless nickel plating is a method that can be selectively deposit onto desired locations by controlling the surface preparation and conditioning by means of an autocatalytic chemical reaction. An immersion gold layer 120 (Figure 13) is also applied to prevent the electroless nickel 118 from oxidation.

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The solder bumps 122 comprising the interconnection pads can be formed (Figure 14) by screen printing of solder paste on the electroless nickel/immersion gold contacting portions. Suitable solder alloys include, but are not limited to eutectic tin-lead alloys, tin-lead alloys contain 95% tin and tin-copper contain 99.3% tin. The solder paste is screen
5 printed and melted with suitable temperature to form the solder bumps.

The WLCSP processing steps described hereinbefore can be performed at the semiconductor wafer level or before the wafer is singulated. The semiconductor wafer can then dice to individual chips with conventional dicing methods. The chip is then ready to
10 mount on a conventional printed circuit board or substrate with conventional pick and place or flip-chip mounting method.

An example of a conductive circuit, formed in accordance with the invention, is shown in Figure 16.
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The foregoing detailed description of the invention has been presented by way of example only, and is not intended to be considered limiting to the invention as defined in the claims appended hereto.

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Claims:

1. A method of forming circuit interconnections on a substrate, including:
directing a laser beam to trace over selected portions of the substrate to activate a predetermined circuit interconnection pattern on a surface of said substrate;
forming a metallic circuit interconnection seed layer on said substrate surface corresponding to said predetermined circuit interconnection pattern; and
depositing metal onto said circuit interconnection seed layer in an electroless plating process.
2. A method as claimed in claim 1, including applying a metalorganic film to said substrate surface before activating said predetermined circuit interconnection pattern with said laser beam.
3. A method as claimed in claim 2, wherein the step of activating said predetermined circuit interconnection pattern with said laser beam comprises heating the selected portions of the substrate surface with said laser beam so as to cause thermal decomposition of corresponding portion of the metalorganic film thereon.
4. A method as claimed in claim 3, including removal of the remainder of the metalorganic film from said substrate.
5. A method as claimed in claim 2, wherein said metalorganic film comprises a film of copper formate.
6. A method as claimed in claim 1, wherein the step of activating said predetermined circuit interconnection pattern comprises laser-catalyzing of the selected portion of the substrate surface with said laser beam.

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7. A method as claimed in claim 6, including applying a metal electrolyte solution to the activated substrate surface to form said metallic circuit interconnection seed layer.

8. A method as claimed in claim 1, wherein said laser beam is generated using a Nd:YAG laser apparatus.

9. A method of forming circuit interconnections on a substrate, including:
directing a laser beam to trace a predetermined circuit interconnection pattern on a surface of said substrate to thereby effect laser-induced deposition of a seed metal layer in said predetermined circuit interconnection pattern on said substrate surface; and
performing electroless metal plating on said seed metal layer to form said circuit interconnections on said substrate.

10. A method as claimed in claim 9, including applying a metalorganic film to said substrate surface, wherein the laser-induced deposition comprises heating of selected portions of the metalorganic film with said laser beam so as to cause thermal decomposition thereof according to said predetermined circuit interconnection pattern.

11. A method as claimed in claim 10, including removal of the remainder of the metalorganic film from said substrate.

12. A method as claimed in claim 10, wherein said metalorganic film comprises a film of copper formate.

13. A method as claimed in claim 9, wherein said laser-induced deposition comprises laser-catalyzing of selected portions of said substrate surface and application of a metal electrolyte solution to the laser-catalyzed substrate surface.

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14. A method as claimed in claim 13, wherein the substrate comprises polyimide.
15. A method as claimed in claim 9, wherein said laser beam is generated using a Nd:YAG laser apparatus.
16. A method as claimed in claim 9, wherein the substrate comprises an integrated circuit wafer.
17. A method as claimed in claim 9, wherein the substrate comprises an integrated circuit die.
18. A method as claimed in claim 16, wherein said substrate surface comprises the surface of a passivation layer on said integrated circuit wafer.
19. A method as claimed in claim 18, wherein the circuit interconnections comprise input/output contact redistribution tracks for wafer level chip scale packaging of integrated circuits on said wafer.
20. A method as claimed in claim 19, including the formation of I/O contact pads on said input/output contact redistribution tracks for, in use, coupling the integrated circuits on the wafer to external circuitry.
21. A method as claimed in claim 20, wherein said I/O contact pads comprise solder bumps for, in use, surface mounting of said integrated circuit on a circuit board.
22. A circuit board including a substrate having a dielectric substrate surface, the circuit board further including a first metallic seed layer on said substrate surface in a predetermined circuit interconnection pattern, the seed layer being formed by laser-induced metal deposition, and a second metal layer deposited on said seed layer by electroless metal plating.

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23. A circuit board as claimed in claim 22, wherein the metallic seed layer comprises copper.

24. A circuit board as claimed in claim 23, wherein the second metal layer comprises copper.

25. A circuit board as claimed in claim 23, wherein the second metal layer comprises nickel.

26. A circuit board as claimed in claim 22, wherein the metallic seed layer is formed by applying a metalorganic film onto said substrate surface and thermal decomposition of portions of the metalorganic film according to said predetermined circuit interconnection pattern using a laser beam.

27. A circuit board as claimed in claim 23, wherein the metallic seed layer is formed by applying a film of copper formate onto said substrate surface and thermal decomposition of portions of said film according to said predetermined circuit interconnection pattern using a laser beam.

28. A circuit board as claimed in claim 27, wherein a Nd:YAG laser is used in the laser-induced metal deposition.

29. A method of forming I/O contacts on an integrated circuit wafer, the integrated circuit wafer having a passivation layer with apertures formed therein at which contact pads for integrated circuits on the wafer are exposed, the method including:

forming a metallic seed layer on the wafer by laser-induced metal deposition, the seed layer being formed in a predetermined circuit connection pattern between respective said contact pads and I/O contact locations;

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depositing a second metal layer onto said seed layer using an electroless metal plating process; and

forming I/O contacts at said I/O contact locations, wherein said seed layer and said second metal layer provide electrical interconnection between the I/O contacts and respective integrated circuit contact pads.

30. A method as claimed in claim 29, wherein the laser-induced metal deposition includes applying a metalorganic precursor film over said wafer passivation layer, effecting thermal decomposition of selected portions of the precursor film according to the predetermined circuit connection pattern using a laser beam, and removing the remainder of the precursor film.

31. A method as claimed in claim 30, wherein said precursor film comprises a film of copper formate.

32. A method as claimed in claim 29, wherein said laser-induced deposition comprises applying an organic passivation layer to said wafer, laser-catalyzing selected portions of said organic passivation layer surface and application of a metal electrolyte solution to the laser-catalyzed surface so as to form metal deposits thereon according to said predetermined circuit connection pattern.

33. A method as claimed in claim 29, including application of an organic passivation layer to the wafer prior to said laser-induced metal deposition, the organic passivation layer being patterned for exposure of said contact pads.

34. A method as claimed in claim 33, including application of a second organic passivation layer following said electroless metal plating process, the second organic passivation layer being patterned for exposure of said second metal layer at said I/O contact locations.

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35. A method as claimed in claim 34, wherein said I/O contacts comprise solder bumps formed at said I/O contact locations on the wafer.
36. A method as claimed in claim 35, including a second electroless metal plating process performed after application of the second passivation layer and before formation of said solder bumps.
37. A method as claimed in claim 35, including applying an immersion gold layer over the metal deposited in said second electroless plating process before formation of said solder bumps.
38. An integrated circuit wafer construction including a plurality of integrated circuits and a passivation layer thereon, the wafer construction including a metallic seed layer formed on the passivation layer by laser-induced metal deposition in a predetermined circuit connection pattern between contact pads of the integrated circuits and respective I/O contact locations, the wafer construction further including a second metal layer deposited onto the seed layer by an electroless metal plating process.
39. An integrated circuit wafer construction as claimed in claim 38, wherein the metallic seed layer is formed by applying a metalorganic film onto said passivation layer and thermal decomposition of portions of the metalorganic film according to said predetermined circuit interconnection pattern using a laser beam.
40. An integrated circuit wafer construction as claimed in claim 39, wherein said metalorganic film comprises a film of copper formate.
41. An integrated circuit wafer construction as claimed in claim 38, wherein said passivation layer includes an organic passivation layer.

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42. An integrated circuit wafer construction as claimed in claim 38, further including a second passivation layer over said second metal layer, the second passivation layer having apertures formed at said I/O contact locations.

43. An integrated circuit wafer construction as claimed in claim 42, further including I/O contacts formed at said I/O contact locations.

44. An integrated circuit wafer construction as claimed in claim 43, wherein said I/O contacts include solder bumps.

45. An integrated circuit wafer construction as claimed in claim 44, wherein the I/O contacts include a further electroless metal layer applied after said second passivation layer.

46. An integrated circuit wafer construction as claimed in claim 45, including an immersion gold layer applied over said further electroless metal layer.

47. An integrated circuit package formed from dicing an integrated circuit wafer construction as claimed in claim 38.

48. An integrated circuit package formed according to the method as claimed in claim 29.