

PATENT SPECIFICATION

(11) 1 536 001

1 536 001

- (21) Application No. 44637/76 (22) Filed 27 Oct. 1976
 (31) Convention Application No. 50/129577
 (32) Filed 28 Oct. 1975 in
 (33) Japan (JP)
 (44) Complete Specification published 13 Dec. 1978
 (51) INT CL² G04C 23/08 23/12
 (52) Index at acceptance
 G3T 605.608 S1



(54) DIGITAL ALARM TIMEPIECE

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA a Japanese Company of 31-1 6-chome Kameido Koto-ku Tokyo Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to digital alarm timepieces.

In a conventional digital alarm timepiece which has a timekeeping circuit and which displays an actual time of day indication on a twenty-four-hour basis, the actual time of day indication 00:00 is the same as the display 00:00 when the timekeeping circuit is reset so that it is very difficult to distinguish at this time whether the actual time of day indication is being displayed or whether the time keeping circuit has just been reset.

According to one aspect of the present invention there is provided a digital alarm timepiece comprising: a timekeeping circuit for producing a time indication on a twenty-four hour basis; a memory means for memorising an alarm time; alarm producing means for producing an alarm when the alarm time and an actual time of day indication coincide; a digital display device for displaying the actual time of day indication and the contents of the memory means; and setting means for setting the memory means to zero and for causing the display device to produce a non-digital display when the memory means is so set.

Preferably, the timekeeping circuit includes an oscillator as a standard time generator and a frequency dividing circuit.

The memory means may comprise a plurality of memory circuits.

The setting means, in the preferred embodiment, includes a NOR circuit. The display device may be arranged to be driven by signals having the same frequency but of opposite polarity.

According to a further aspect of the present invention there is provided a digital alarm timepiece comprising: at least one

memory circuit for memorising an alarm time; setting means for setting the or each memory circuit to zero; a switching circuit, including a plurality of transmission gates and an inverter, connected to said memory circuit or circuits; a minutes decoder and an hours decoder; a switching means connected to the output of each decoder, each switching means being composed of a pair of AND circuits and a NOR circuit, the AND circuits being connected to receive as inputs signals having frequencies of 32 Hz and $\frac{32}{3}$ Hz; a display device, for displaying a plurality of digits of a time indication, composed of a plurality of segment electrodes and a common electrode, the arrangement being such a display of "----" is produced only when the memory circuits are set to zero.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:—

Figure 1 is a block diagram of part of an embodiment of a digital alarm timepiece according to the present invention; and

Figure 2 illustrates a display device of the digital alarm timepiece of Figure 1.

Referring to the drawings, there is illustrated an embodiment of a digital alarm timepiece according to the present invention having three memories M1, M2, M3 each of the same construction for memorising an alarm time, an alarm being produced by means (not shown) when the alarm time and the actual time of day indication coincide.

In the case of displaying the content of a memory, a signal of logical 0 from a NOR circuit 1 is applied to a NAND circuit 6 whose output signal thus becomes logical 1. The output signal from the NAND circuit 6 is applied to a NAND circuit 8 whose output signal becomes logical 0. This causes transmission gates 22, 24 to go into the ON state.

An input signal AC-1 (having a frequency of 32 Hz) is applied to one input of an AND circuit 11 via the transmission gate 22 and

also to a common electrode 34 of a display device. The input signal AC-1 is inverted by an inverter 20 and is applied to one input of an AND circuit 12 via the transmission gate 24.

A signal of logical 1 from the memory M1 is applied to an NOR circuit 25 which generates an output signal of logical 0 which is applied to the other input of the AND circuit 12 which is thus closed whereby the inverted input signal AC-1 is not applied to a channel display electrode S1. The output signal from the NOR circuit 25 is inverted by an inverter 28 so that a logical 1 signal is applied to the other input of the AND circuit 11 which thus opens to pass the input signal AC-1. The input signal AC-1 appearing at the output of the AND circuit 11 is inverted by a NOR circuit 31 whereby the inverted input signal AC-1 is applied to the channel display electrode S1.

The common electrode 34 receives the input signal AC1 whereby the display device displays the memorised contents of the memory M1.

The memory M1 is set to zero by a signal logical 1 whereby the time display becomes 00:00. At this time, the signal of logical 1 from the NOR circuit 1 is applied to the NAND circuit 6 and the NAND circuit 8 produces a signal of logical 0 whereby the transmission gates 21, 23 go into the ON state. The input signal AC-1 is applied to the AND circuit 12 via the transmission gate 23. The input signal AC-1 is inverted by the inverter 20 and is applied to the AND circuit 11 and to the common electrode 34 via the transmission gate 21. A signal of logical 1 from the memory M1 becomes logical 0 via the NOR circuit 25 whereby the AND circuit 12 is closed.

The signal of logical 0 on the NOR circuit 25 is inverted into a logical 1 signal by the inverter 28, whereby the AND circuit 11 is opened. The inverted input signal AC-1 is supplied to the NOR circuit 31 so that the channel display electrode S1 receives the input signal AC-1. Further, the common electrode 34 receives the inverted input signal AC-1 so that the contents of the memory M1 are displayed.

A minutes decoder 35 and an hours decoder 41 cause a signal applied to a segment g of each section (one shown in Figure 2) of the display device to become logical 1 via inverters 36, 42 so that AND circuits 38, 44 are opened. A signal AC-2 which is identical to the inverted input signal AC-1 when inverted is applied to NOR circuits 39, 45 whereby a signal identical to the input signal AC-1 is produced and applied to electrodes S2, S3 corresponding to segment g of the minutes and hours sections of the display device. The common electrode 34 continues to

receive the inverted input signal AC-1 therefore only segment g is energised. As a result, when the signal from the minutes and hours decoders 35, 41 is maintained to g=0, the display becomes --- when the memories M1, M2, M3 are set to zero.

When segments a to f are maintained at logical 1, AND circuits 37, 43 are opened whereby the input signal AC-1 is passed and the signal AC-2 is applied to the other electrodes a to f via NOR circuits 39, 45. In this case, the common electrode 34 is maintained with the inverted input signal AC-1 whereby the display portion is not operated when the memories are set to zero.

The memories M2, M3 are operated in the same manner described above in relation to the memory M1.

In the embodiment of the present invention described above, when the memory circuits are set to zero, i.e. 00:00 it is possible to produce a distinct display, namely --- which is distinguished from the normal time display 00:00.

WHAT WE CLAIM IS:—

1. A digital alarm timepiece comprising: a timekeeping circuit for producing a time indication on a twenty-four hour basis; a memory means for memorising an alarm time; alarm producing means for producing an alarm when the alarm time and an actual time of day indication coincide; a digital display device for displaying the actual time of day indication and the contents of the memory means; and setting means for setting the memory means to zero and for causing the display device to produce a non-digital display when the memory means is so set.

2. A timepiece as claimed in Claim 1 in which the timekeeping circuit includes an oscillator as a standard time generator and a dividing circuit.

3. A timepiece as claimed in Claim 1 or 2 in which the memory means comprises a plurality of memory circuits.

4. A timepiece as claimed in any preceding claim in which the setting means includes a NOR circuit.

5. A timepiece as claimed in any preceding claim in which a display device is arranged to be driven by signals having the same frequency but of opposite polarity.

6. A digital alarm timepiece comprising: at least one memory circuit for memorising an alarm time; setting means for setting the or each memory circuit to zero; a switching circuit, including a plurality of transmission gates and an inverter, connected to said memory circuit or circuits; a minutes decoder and an hours decoder; a switching means connected to the output of each decoder, each switching means being

(12)



also to a common electrode 34 of a display device. The input signal AC-1 is inverted by an inverter 20 and is applied to one input of an AND circuit 12 via the transmission gate 24.

5 A signal of logical 1 from the memory M1 is applied to an NOR circuit 25 which generates an output signal of logical 0 which is applied to the other input of the
10 AND circuit 12 which is thus closed whereby the inverted input signal AC-1 is not applied to a channel display electrode S1. The output signal from the NOR circuit 25 is inverted by an inverter 28 so that a
15 logical 1 signal is applied to the other input of the AND circuit 11 which thus opens to pass the input signal AC-1. The input signal AC-1 appearing at the output of the AND circuit 11 is inverted by a NOR circuit 31
20 whereby the inverted input signal AC-1 is applied to the channel display electrode S1.

The common electrode 34 receives the input signal AC1 whereby the display device displays the memorised contents of the memory M1.

25 The memory M1 is set to zero by a signal logical 1 whereby the time display becomes 00:00. At this time, the signal of logical 1 from the NOR circuit 1 is applied to the
30 NAND circuit 6 and the NAND circuit 8 produces a signal of logical 0 whereby the transmission gates 21, 23 go into the ON state. The input signal AC-1 is applied to the AND circuit 12 via the transmission
35 gate 23. The input signal AC-1 is inverted by the inverter 20 and is applied to the AND circuit 11 and to the common electrode 34 via the transmission gate 21. A signal of logical 1 from the memory M1 becomes
40 logical 0 via the NOR circuit 25 whereby the AND circuit 12 is closed.

The signal of logical 0 on the NOR circuit 25 is inverted into a logical 1 signal by the inverter 28, whereby the AND circuit 11 is
45 opened. The inverted input signal AC-1 is supplied to the NOR circuit 31 so that the channel display electrode S1 receives the input signal AC-1. Further, the common electrode 34 receives the inverted input
50 signal AC-1 so that the contents of the memory M1 are displayed.

A minutes decoder 35 and an hours decoder 41 cause a signal applied to a segment g of each section (one shown in
55 Figure 2) of the display device to become logical 1 via inverters 36, 42 so that AND circuits 38, 44 are opened. A signal AC-2 which is identical to the inverted input signal AC-1 when inverted is applied to
60 NOR circuits 39, 45 whereby a signal identical to the input signal AC-1 is produced and applied to electrodes S2, S3 corresponding to segment g of the minutes and hours sections of the display device.
65 The common electrode 34 continues to

receive the inverted input signal AC-1 therefore only segment g is energised. As a result, when the signal from the minutes and hours decoders 35, 41 is maintained to g=0, the display becomes --- when the memories M1, M2, M3 are set to zero.

When segments a to f are maintained at logical 1, AND circuits 37, 43 are opened whereby the input signal AC-1 is passed and the signal AC-2 is applied to the other electrodes a to f via NOR circuits 39, 45. In this case, the common electrode 34 is maintained with the inverted input signal AC-1 whereby the display portion is not operated when the memories are set to zero.

The memories M2, M3 are operated in the same manner described above in relation to the memory M1.

In the embodiment of the present invention described above, when the memory circuits are set to zero, i.e. 00:00 it is possible to produce a distinct display, namely --- which is distinguished from the normal time display 00:00.

WHAT WE CLAIM IS:—

1. A digital alarm timepiece comprising: a timekeeping circuit for producing a time indication on a twenty-four hour basis; a memory means for memorising an alarm time; alarm producing means for producing an alarm when the alarm time and an actual time of day indication coincide; a digital display device for displaying the actual time of day indication and the contents of the memory means; and setting means for setting the memory means to zero and for causing the display device to produce a non-digital display when the memory means is so set.

2. A timepiece as claimed in Claim 1 in which the timekeeping circuit includes an oscillator as a standard time generator and a dividing circuit.

3. A timepiece as claimed in Claim 1 or 2 in which the memory means comprises a plurality of memory circuits.

4. A timepiece as claimed in any preceding claim in which the setting means includes a NOR circuit.

5. A timepiece as claimed in any preceding claim in which a display device is arranged to be driven by signals having the same frequency but of opposite polarity.

6. A digital alarm timepiece comprising: at least one memory circuit for memorising an alarm time; setting means for setting the or each memory circuit to zero; a switching circuit, including a plurality of transmission gates and an inverter, connected to said memory circuit or circuits; a minutes decoder and an hours decoder; a switching means connected to the output of each decoder, each switching means being



11

3

1,536,001

3

- 5 composed of a pair of AND circuits and a NOR circuit, the AND circuits being connected to receive as inputs signals having frequencies of 32 Hz and 32 Hz; a display device, for displaying a plurality of digits of a time indication, composed of a plurality of segment electrodes and a common electrode, the arrangement being such a display of "----" is produced only
- 10 when the memory circuits are set to zero.

7. A digital alarm timepiece substantially as herein described with reference to and as shown in the accompanying drawings.

J. MILLER & CO.,
Chartered Patent Agents,
Agents for the Applicants,
Lincoln House,
296—302 High Holborn,
London, WC1V 7JH.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1978
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from
which copies may be obtained.