SYSTEM AND METHOD USING SELF-ASSEMBLED NANO STRUCTURES IN THE DESIGN AND FABRICATION OF AN INTEGRATED CIRCUIT MICRO-COOLER

by inventor

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BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the removal of heat generated by an integrated circuit and the components used in chip assembly and packaging to facilitate said heat removal. More specifically, this invention discloses the application of self-assembled nano-structures for improving the performance of heat sink structures coupled to integrated circuit devices.

2. Description of the Related Art

Prior art used to cool semiconductor ICs incorporates the use of large and expensive chip packaging having externally mounted, finned heat sinks coupled to the ceramic or plastic encapsulated IC chip. As the speed and density of modern integrated circuits increase, the power generated by these chips also increases, often in geometric proportion to increasing density and functionality. In the video processing and CPU application areas, the ability to dissipate the heat being generated by current ICs is becoming a serious limitation in the advance of technology. In the current art, relatively large interface-thermal-resistances are added when the die is 'attached' to a heat spreader, heat pipe or heat sink. These multiple interfaces have the undesired side effect of increasing total die to heat sink resistance and making heat transfer more difficult.

Figure 1 (Prior Art) is a cross section schematic view of a simplified integrated circuit structure. Transistor structure 102 is formed near the top surface of substrate 100. Electrical interconnects 106 are used to make contact with transistor 102 and numerous other similar devices (not shown) on the substrate 100. "Solder balls" 104 are utilized to complete the interconnect of the integrated circuit to a printed circuit board or wire leadframe. This type of package is often referred to as a "flip chip" device. In the current

art, heat generated by transistor 102 is extracted through the substrate 100 to the back surface of the chip. A heat transfer bonding layer 108 may be utilized to enhance heat conduction by reducing interfacial heat transfer resistance created by air gaps and surface irregularities. Typically, this layer may be composed of a thermal grease or thermally conductive epoxy. These materials, while better that solid surface/surface contact, still have a relatively poor thermal conductivity when compared to solid metals. As a result, the backside chip surface interface still presents a significant thermal resistance which limits the power that can be extracted from the chip.

Recently, US Patent Application Publication number US2003/0117770 has disclosed a process of forming a thermal interface that employs carbon nano-tubes to reduce thermal resistance between an electronic device and a heat sink. Bundles of aligned nano-tubes receive injected polymeric material in molten form to produce a composite which is placed between the electronic device and the heat sink. The nano-tubes are aligned parallel to the direction of heat energy. However, the polymeric filler does little to spread heat laterally, potentially creating localized hot spots on the device surface. The use of bundles of aligned carbon nano-tubes may result in reduced thermal conduction as well. Theoretical molecular dynamics simulations have shown that isolated carbon nano-tubes show unusually high thermal conductivity, but that the thermal conductivity degrades by an order of magnitude when carbon nano-tube bundles are formed with tube-to-tube contacts (see for example Savas Berber, et al, Physics Review Letters, 84, no.20, 4613, May 2000).

US Patent Application Publication US2003/231471 discloses an integrated circuit package that utilizes single wall or double wall carbon nano-tube arrays grown subsequent to the deposition of CVD diamond films. Due to the roughness of CVD diamond films, carbon nano-tubes are utilized to aid in making thermal contact between the surfaces of the circuit silicon die and of the integrated heat spreader. The interstitial voids between the nano-tubes are not filled in order to maintain flexibility. This disclosure, however, fails to provide any method to reduce matting and nano-tube to nano-tube contact, which reduces the effective thermal conductivity of the structure. Although CVD diamond films are good conductors, they may not be thermally compatible (from an expansion perspective) with a number of other metallic materials utilized in various heat sink structures. Additionally, commonly known techniques for growing carbon nano-tubes

would preclude carbon nanotube deposition directly on a silicon circuit die, since these techniques require temperatures in the range of 700 to 800 °C. Exposing a completed circuit die to these elevated temperatures is not a recommended practice.

What is needed is a method and structure by which interface resistances are minimized by integrating several thermal components to maximize heat transfer from hot surfaces on the integrated circuit.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a micro-cooler device structure containing a heat sink body having a heat sink surface, a plurality of individually separated, rod like nano-structures for transferring thermal energy from a surface of at least one integrated circuit chip to the heat sink surface, the plurality of individually separated, rod-like nano-structures being disposed between the heat sink surface and the heat generating surface, and a thermally conductive material disposed within interstitial voids between the rod-like nano-structures.

In one embodiment of the present invention, a method for fabricating a micro-cooler device includes fashioning a shallow cavity in a mounting surface of a heat sink body, growing rod-like nano-structures within the shallow cavity, and depositing a thermally conductive material in interstitial voids between the rod-like nano-structures.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be better understood when consideration is given to the following detailed description thereof. Such description makes reference to the annexed drawings, wherein:

Figure 1 (Prior Art) is a cross section schematic view of an integrated circuit structure;

Figure 2 is a schematic side view of integrated micro-cooler device attached to a flip chip integrated circuit according to an embodiment of the present invention;

Figure 3 is a schematic side view of integrated micro-cooler device attached to multiple flip chip integrated circuits according to an embodiment of the present invention;

Figure 4 is a cross section schematic view of a finned integrated micro-cooler device showing the details of construction according to an embodiment of the present invention;

Figure 5 is a cross section schematic view of an integrated micro-cooler device having internal flow channels according to an embodiment of the present invention;

Figure 6 is an electron microscope photo of carbon nano-tubes according to an embodiment of the present invention;

Figure 7 is a cross section schematic view of an integrated micro-cooler device bonded to multiple flip chip integrated circuits according to an embodiment of the present invention;

Figure 8 is a process flow diagram illustrating the steps for manufacture of a finned integrated micro-cooler device according to an embodiment of the present invention;

Figure 9 is a process flow diagram illustrating the steps for manufacture of an integrated micro-cooler device having internal flow channels according to an embodiment of the present invention; and,

Figure 10 is a partial cross section view of the nano-structure array subsequent to a planarization process according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 (prior art) has been addressed above in the Background section of this disclosure.

Figure 2 is a schematic side view 200 of integrated micro-cooler device 202 attached to a flip chip integrated circuit 206 according to an embodiment of the present invention. The integrated micro-cooler device 202 is a separate structure from chip 206 containing highly conductive, self assembled nano structures, integrated with heat sinking devices. It provides a low thermal resistance path for heat transferred from surface 208 of

the integrated circuit chip 206 mounted on circuit board 210 below. Thermal interface layer 204 provides a low resistance interface containing nano-structures to enhance heat conduction from chip 206, reduce the impact of local hot spots in chip 206, and laterally conduct heat to a heat sink structure 202 of greater footprint than the chip 206. Structural details of micro-cooler device 202 are disclosed below. Chip 206 and micro-cooler 202 may be bonded together using eutectic layers or thermal bonding adhesives (not shown), as is known to those skilled in the art. Additionally, micro-cooler device 202, integrated circuit chip 206, and circuit board 210 may be held together with mechanical straps, clips, or holding devices (not shown).

Figure 3 is a schematic side view 300 of integrated micro-cooler device 302 attached to multiple flip chip integrated circuits (306a-306d) according to an embodiment of the present invention. In this embodiment, both the upper and lower surfaces of micro-cooler device 302 are utilized to remove heat energy from flip chip ICs 306a-306d. Chips 306a and 306b, mounted on printed circuit board 310a, sink heat from surfaces 308a and 308b, to device 302 via interface layer 304a. Chips 306c and 306d, mounted on printed circuit board 310b, sink heat from surfaces 308c and 308d, to device 302 via interface layer 304b. Chips 306 and micro-cooler 302 may be bonded together using eutectic layers or thermal bonding adhesives (not shown), as is known to those skilled in the art. Additionally, micro-cooler device 302, integrated circuit chips 306, and circuit boards 310 may be held together with mechanical straps, clips, or holding devices (not shown). Although the embodiment shown in Figure 3 contains four integrated circuits, it should be evident to those of ordinary skill in the art that any number of additional integrated circuit flip chips 306 may be added by increasing the scale of device 302.

Figure 4 is a cross section schematic view of a finned integrated micro-cooler device 400 showing the details of construction according to an embodiment of the present invention. The device 400 comprises a heat sink body 404 for extracting thermal energy from surface 418 of flip chip 402. Heat energy is delivered to heat sink surface 420 by an enhanced heat transfer interface structure containing layers 408, 410, and 412. Heat sink body 404 is fabricated with fins 414 (or pin shaped structures) to enhance heat extraction by convection, typically forced air flow generated by fans or other devices. However, natural convection may also be employed if suitable. Also, fins 414 may be immersed in a liquid such as water or another liquid phase coolant for removal of high energy fluxes.

Heat sink body 404 may be made from silicon, metals, or heat conductive ceramics. Metals such as copper or aluminum are preferred, but structures fashioned from silicon substrates may also be used. If silicon is used, the fin surfaces may be coated with a metal to enhance lateral heat conduction. Heat spreading cavity 416 is fashioned within heat sink body 404, by methods well known to those skilled in the art, to contain heat transfer interface layers 408, 410, and 412.

Layer 408 contains individually separated, rod-like nano-structures that provide very high thermal conductivity to reduce interface contact resistance. These structures may be comprised of metallic nano-wires, or preferably multi walled carbon nano-tubes (MWCNT) or multi-wall carbon nano-fibers. Metallic nanowires (for example Au, Cu, Ni, zinc oxide, and metal borides) are metal crystals having the shape of a wire with dimensions comparable to the phonon mean free path (usually tens of nanometers at room temperature) so as to benefit from quantum confinement phenomena allowing for efficient heat transport characteristics and thermal contact. In one example, metal boride nanowires are believed to have good thermal contact resistance since low ohmic contact resistance has been demonstrated with Ni electrodes. Preferably, the MWCNTs are oriented (with their longitudinal axis) approximately perpendicular to surfaces 420 and 418, parallel to the direction of heat flow. MWCNTs have very high (on axis) thermal conductivity, generally within the range of 800 to 3000 W/m-^{o}K. They may be up to a factor of two better than solid CVD diamond films. They are preferably grown on the micro-cooler 400 surface as an array of free standing, vertically aligned, individually separated carbon nanotubes (or nanofibers) that occupy between about 15 and 40% of the surface from which they are grown. In some embodiments, the MWCNT are grown by plasma enhanced CVD (PECVD) growth methods. For example, the methods described by Jun Li et al. (Applied Physics Letters, vol. 81, no.5, July 2002) and L. Delzeit et al. (J. Appl. Physics 91, 6027, May, 2002) can be used. However, while axial thermal conduction of CNTs is very high, lateral thermal conduction (in the non-axial direction from nano-tube to nano-tube) is not as good. In fact, it has been found that lateral contact between axially aligned nano-tubes can reduce their effective axial thermal conductivity. If the number of carbon nano-tubes attached to substrate is too high (for example, > 40% CNT density) Van der Waals force will create a bundle or mat situation resulting in poor thermal conduction. If, on the other hand the coverage density is too low (for example, < 15%),

thermal conduction will also be lower due to the reduced number of conducting nano-tubes. A preferred range a coverage density is between about 15 and 40%, with 25% to 40% being most preferred. Thus, as opposed to bundle or mat of CNTs, vertically aligned, individually separated, parallel CNTs with coverage between about 15 and 40%, can provide better overall thermal conduction. To improve lateral heat conduction, a thermally conductive material is placed within the interstitial voids between the MWCNTs. The thermally conducting material provides lateral heat conduction within the nano-tube containing layer. Lateral heat conduction facilitates the spreading of heat from a relatively small silicon die surface to the much larger surface area of the heat sink body 404. It also reduces localized hot spots on surface 418 of chip 402. The thermally conductive material may be a metal or metal alloy, thermally conductive ceramics, CVD diamond, or thermally conductive polymers. Preferably, the thermally conductive material is a metal such as copper, aluminum, silver, gold, or their alloys. Of the metal materials, copper and copper alloys are the most preferable. This is generally due to the high thermal conductivity, ease of deposition via electroplating or electrochemical deposition, and low cost. Copper electroplating is well known to those skilled in the art of dual Damascene processing common in the production of modern integrated circuits. Depending on the thermal conductivity of the thermally conductive filler material, layer 408 would typically be between 50 and 1000 microns in thickness.

Another desirable feature of using metal as a filler material is that it is significantly lower in hardness than the MWCNTs. In some embodiments, planarization of layer 408 is used to maintain flatness for good "long range" contact. However, "short range" surface irregularities (on the order of a few microns) can also contribute significantly to interface thermal resistance. It is therefor desirable to have some portion of the MWCNTs extend from the bulk of layer 408 so that the exposed ends may conform to these surface irregularities and improve thermal contact. When layer 408 is planarized, the softer metal material is eroded more than the harder nanotubes, resulting in an undercutting of the metal layer. This undercutting leaves a portion of the nanotubes extending from the composite layer 408. This undercutting will automatically occur when layer 408 is planarized with CMP (chemical-mechanical planarization) or electrochemical etching techniques. An additional (optional) bonding layer 406 can be added, if eutectic metal bonding between chip 402 and layer 408 is desired. In this case, the exposed

nanotube ends would protrude into this layer and may extend through it. Preferably, bonding layer 406 is a eutectic metal, but thermal polymer based bonding compounds may also be used. Layer 412 is an interface material which can be used with a silicon heat sink body 404. Typically, layer 412 would be composed of silicon nitride compounds. For metal heat sink bodies 404, layer 412 is optional, is only required to aid in the adhesion of catalyst metal layer 410. Metal catalyst layer 410 is used to initiate and control growth of the nanotubes in layer 408. Metal catalyst layer 410 may chosen from among Ti, Co, Cr, Pt, Ni and their alloys. Preferably, metal catalyst layer 410 are Ni and Ni alloys. Further process conditions related to these layers are discussed below.

Figure 5 is a cross section schematic view of an integrated micro-cooler device 500 having internal flow channels 514 according to an embodiment of the present invention. The device 500 comprises a heat sink body 504 for extracting thermal energy from surface 518 of flip chip 502. Heat energy is delivered to heat sink surface 520 by an enhanced heat transfer interface structure containing layers 508, 510, and 512. Layers 508-512 reside in heat spreading cavity 516 fashioned in body 504. In this embodiment, heat sink body 504 contains enclosed flow passages 514 to remove the thermal energy transferred from chip 502. Both liquid and gas cooling is possible, but for this embodiment liquid cooling is preferred due to the specific heat capacity of a liquid coolant such as water. A refrigerant is also possible for use in very high heat removal systems, or where sub ambient junction temperatures are required for very high speed processors. Due to the high heat fluxes encountered by such systems, the low thermal resistances provided by embodiments of the present invention become essential to reliable operation. Layers 506-512 have the same function and are composed of the same materials as described above for corresponding layers 406-412.

Figure 6 is an electron microscope photo of carbon nano-tubes according to an embodiment of the present invention. In this figure, the aligned, individually separated, parallel nature of the MWCNTs is evident. Also evident are the interstitial voids between nanotubes that need to be filled for good lateral heat conduction.

Figure 7 is a cross section schematic view of an integrated micro-cooler device 700 attached to multiple flip chip integrated circuits according to an embodiment of the present invention. The device 700 comprises a heat sink body 704 for extracting thermal energy from heat generating multiple flip chips 702a and 702b. Heat energy is delivered

to heat sink surfaces 720a and 720b by an enhanced heat transfer interface structure containing layers 508a-512a and 508b-512b. Layers 508a-512a and 508b-512b reside in heat speading cavities 716a and 716b, respectively. In this embodiment, heat sink body 704 contains enclosed flow passages 714 to remove the thermal energy transferred from chip 502. For this embodiment, due to the increased heat loading, liquid cooling is preferred due to the specific heat capacity of a liquid coolant such as water. A refrigerant is also possible for removal of the high heat loads, or where sub ambient junction temperatures are required for very high speed processors. Layers 706a-712a and 706b-712b have the same function and are composed of the same materials as described above for corresponding layers 406-412.

Figure 8 is a process flow diagram 800 illustrating examplary steps for manufacture of a finned integrated micro-cooler device according to an embodiment of the present invention. At 802, a suitable material is selected for the substrate or heat sink body (e.g., 404). The subsequent steps refer to a process where silicon is chosen as the substrate. At 804, heat spreading cavities (e.g., 416) are patterned in a first (or bottom) surface. At 806, the heat spreading cavities are etched, and at 808, an interface material (e.g., 412) is deposited in the cavities (e.g., 416). As previously mentioned, this interface material is silicon nitride in some embodiments. Numerous techniques are known to those skilled in the art to deposit silicon nitride, examples of which are CVD, or sputtering. Alternatively, the heat spreading cavities can be fabricated by machining if the heat sink body material is chosen to be a metal or ceramic. At 810, an optional conductive layer is deposited over the interface layer, to facilitate the deposition and adhesion of the subsequent catalyst layer. The conductive layer would be composed of Ti, Cr, or Pt with thickness in the range of 3nm – 200nm. If the heat sink body is metal, a conductive layer may not be required. At 812, a catalyst material chosen from among Ti, Co, Cr, Pt, Ni, and their alloys is deposited using CVD, PVD, electroplating or electroless deposition to a layer thickness of 3 nm to 30 nm. At 814, a carbon nanotube array (e.g., as part of layer 408) of individually separated carbon nanotubes is grown. In some embodiments, the array is grown via PECVD per the method of J. Li and A. Delzeit referenced previously. At 816, a thermally conductive material is deposited between the carbon nanotubes. For a thermally conductive material that is a metal, the material is typically deposited by electrochemical deposition or CVD as is known to those skilled in the art. If a CVD

diamond interstitial material is used, CVD processes known in the art can be used. At 818, the carbon nanotube containing layer (e.g., 408) is planarized by CMP, electrochemical etching, or a combination of both. At 820, an optional eutectic bonding layer (e.g., 406) of appropriate thickness is added if desired. At 822, fins (e.g., 414) are patterned in a second (or top) surface for silicon substrates. At 824, the fins are etched by well known methods. At 826, the fins are coated with an optional metal coating or CVD diamond, deposited at the appropriate thickness required to minimize temperature gradients along the fins' surfaces. For the case of a metal heat sink body (e.g., 404), the fins are fabricated by well known machining processes.

Figure 9 is a process flow diagram 900 illustrating examplary steps for manufacture of an integrated micro-cooler device having internal flow channels according to an embodiment of the present invention. At 902, the flow passages (e.g., 514) are fabricated in the heat transfer body (e.g., 504). For metal bodies, standard machining techniques can be used. For silicon substrates, fins may be fabricated as described in the embodiments shown in figure 8. A suitable metal, ceramic, or silicon plate or cover is adhesively bonded to the top, flat surfaces of the fins to create enclosed passages (e.g., 514).

Figure 10 is a partial cross section view 1000 of the nano-structure array subsequent to a planarization process according to an embodiment of the present invention. Carbon nanotubes or nanowires 1008 are grown from the metal/catalyst layer 1002 in an approximately parallel structure as shown. As previously described, a thermally conductive filler material 1004 is placed in the voids between the nano-strucures 1008. Planarization of the nano-structures produces a gap 1006 between the ends of the nano-structures and the recessed planarized surface of the filler material. Gap 1006 results from a chemical-mechanical planarization (CMP) process when a composite material containing components of significantly different hardness is planarized. In the case where the nano-structures are MWCNTs and the filler is a metal such as copper, aluminum, or silver, the planarization process will undercut the filler since the metal is much softer than the carbon nanotubes. The same effect can be created by chemical (or electrochemical) etching of the filler metal, since base metals such as copper are more reactive and susceptible to chemical dissolution than the relatively chemically inert carbon nanotubes.

The unsupported nano-structures in gap 1006 are relatively flexible, allowing the exposed ends to twist and bend (on a micron scale) to conform to undulations and imperfections in the heat generating surface of the integrated circuit chip. This "hair brush" effect produces intimate contact with the ends of the nano-structures, allowing heat extraction along the axis of the nanotubes, where their thermal conductivity is the greatest. If a eutectic or bonding layer is used, the exposed ends of the nano-structures would protrude into this layer, and would be allowed to conform to the opposing surface when the eutectic or bonding layer is fluid, as would occur prior to bonding the two surfaces. The expected gap dimension 1006 depends on the surface flatness of the circuit, silicon die and of the planarized micro-cooler surface. The RMS value of the surface asperity is believed to lie in the range of 0.2 um to 3 um with preferred values being at the lower end of the range.

The various embodiments described above should be considered as merely illustrative of the present invention. They are not intended to be exhaustive or to limit the invention to the forms disclosed. Those skilled in the art will readily appreciate that still other variations and modifications may be practiced without departing from the general spirit of the invention set forth herein. Therefore, it is intended that the present invention be defined by the claims that follow.

What is claimed is:

CLAIMS

1. A micro-cooler device structure comprising:

a heat sink body having a heat sink surface;

a plurality of individually separated, rod like nano-structures for transferring thermal energy from a surface of at least one integrated circuit chip to said heat sink surface, said plurality of individually separated, rod-like nano-structures being disposed between said heat sink surface and said surface of at least one integrated circuit chip; and,

a thermally conductive material disposed within interstitial voids between said plurality of individually separated, rod-like nano-structures.

2. A micro-cooler device as recited in claim 1, wherein said plurality of individually separated, rod-like nano-structures are multi-walled carbon nanotubes.

3. A micro-cooler device as recited in claim 2, wherein said multi-walled carbon nano-tubes are oriented substantially perpendicular to said surface of at least one integrated circuit chip.

4. A micro-cooler device as recited in claim 1, wherein said said plurality of individually separated, rod-like nano-structures are metallic nano-wires.

5. A micro-cooler device as recited in claim 4, wherein said metallic nano-wires are oriented substantially perpendicular to said surface of at least one integrated circuit chip.

6. A micro-cooler device as recited in claim 1, wherein said thermally conductive material comprises copper.

7. A micro-cooler device as recited in claim 1, wherein said thermally conductive material comprises alloys of copper.

8. A micro-cooler device as recited in claim 1, wherein said thermally conductive material comprises silver.

9. A micro-cooler device as recited in claim 1, wherein said thermally conductive material comprises aluminum.

10. A micro-cooler device as recited in claim 1, wherein said heat sink body is cooled by fins.

11. A micro-cooler device as recited in claim 1, wherein said heat sink body is cooled by a liquid flowing through passages fashioned therein.

12. A method for fabricating a micro-cooler device, comprising:

fashioning a heat spreading cavity in a mounting surface of a heat sink body;

growing rod-like nano-structures within said shallow cavity; and,

depositing a thermally conductive material in interstitial voids between said rod-like nano-structures.

13. A method for fabricating a micro-cooler device as recited in claim 12, wherein said rod-like nano-structures are multi-walled carbon nano-tubes.

14. A method for fabricating a micro-cooler device as recited in claim 12, wherein said rod-like nano-structures are metallic nano-wires.

15. A method for fabricating a micro-cooler device as recited in claim 12, wherein said thermally conductive material comprises copper.

16. A method for fabricating a micro-cooler device as recited in claim 12, wherein said thermally conductive material comprises aluminum.

17. A method for fabricating a micro-cooler device as recited in claim 12, wherein said thermally conductive material comprises silver.

18. A method for fabricating a micro-cooler device as recited in claim 12, wherein said rod-like nano-structures are individually separated, and oriented substantially perpendicular to said mounting surface of said heat sink body.

19. A method for fabricating a micro-cooler device as recited in claim 18, further comprising:

planarizing ends of said rod-like nano-structures such that said rod-like nano-structures extend beyond a planarized surface of said thermally conductive material.

20. A method for fabricating a micro-cooler device as recited in claim 19, further comprising:

depositing a bonding layer over the ends of said rod-like nano-structures.