Method for Fabricating a Semiconductor Substrate

The invention relates to a method for fabricating a semiconductor substrate starting from a silicon on insulator (SOI) type substrate.

In the optoelectronics, special substrates are needed which are for example used for image sensors, which find their application in video or photographic cameras. In these substrates, which are based on SOI type substrates, a buried oxide (BOX) is provided on a base through which photons can be collected from the backside of the wafer. Alternatively, the image sensors formed in the device layer of the SOI substrate could be transferred to a final substrate to expose the backside of the sensors. A thin highly doped p++(or n++) first semiconductor layer is directly provided on the buried oxide and a second semiconductor layer with a lower dopant concentration (p-/n- layer) is provided on the first semiconductor layer.

In the prior art, this kind of special substrate was prepared using a highly doped substrate as the donor wafer in the conventional Smartcut™ technology. This method typically comprises the steps of providing a donor substrate, e.g. a silicon wafer, providing an insulating layer on the donor substrate and creating a predetermined splitting area inside the donor substrate, which is achieved by implanting atomic species or ions, like helium or hydrogen ions, into the donor substrate. In the next step the donor substrate is bonded to a base substrate, e.g. a further silicon wafer, such the insulating layer is sandwiched between handle and donor substrate. Subsequently, the remainder of the donor substrate is detached from the bonded donor-base substrate at the predetermined splitting area following a thermal and/or mechanical treatment upon the predetermined splitting area. As a result a semiconductor on insulator (SOI) substrate is obtained.

However, the use of a highly doped substrate can lead to the following problem: It can be observed that cross-contamination from one donor wafer, e.g. with a high dopant concentration, to another wafer, e.g. with a lower dopant concentration like in the standard SOI substrates, occurs within the production line. This leads to unsatisfying dopant profiles in both the p++ type SOI wafers and the standard p- SOI wafers. In addition, during

subsequent annealing steps during the SmartCut™ process, a diffusion of dopants out of the highly doped layer occurs which further deteriorates the substrate.

According to an alternative method a standard SOI substrate with a thin p- (or n-) semiconductor layer was used as starting material over which a further semiconductor layer with a p++ dopant concentration was provided. Finally, an additional semiconductor layer with p- concentration was provided to obtain the desired layer structure. With this method it is, however, not possible to reach a sufficient high dopant concentration in the p++ layer and furthermore the dopant concentration is not sufficiently flat, meaning that that the dopant concentration through the layer is not monotonic, but first increasing and then decreasing within the p++ layer.

Starting therefrom, embodiments of the present invention seek to provide a semiconductor substrate manufacturing process with which improved semiconductor substrates of the above described type can be achieved, thus which represent an improved dopant profile, in particular, in the highly doped p++ layer.

According to a first aspect of the present invention, there is provided a method for fabricating a semiconductor substrate comprising the steps of: a) providing a silicon on insulator (SOI) type substrate comprising a base, an insulating layer and a first semiconductor layer, b) doping the first semiconductor layer to thereby obtain a modified first semiconductor layer, and c) providing a second semiconductor layer with a different dopant concentration than the modified first semiconductor layer over, in particular on, the modified first semiconductor layer wherein doping, in particular, by diffusion doping, and growth of the second semiconductor layer occur at the same time.

According to a second aspect of the present invention, there is provided a method for fabricating a semiconductor substrate comprising the steps of: a) providing a silicon on insulator type (SOI) substrate comprising a base, an insulating layer and a first semiconductor layer, b) doping the first semiconductor layer to thereby obtain a modified first semiconductor layer, and c) providing a second semiconductor layer with a different dopant concentration than the modified first semiconductor layer over, in particular on, the modified first semiconductor layer, wherein step b) and c) are carried out in the same fabrication device, in particular an epi-reactor.

With this method an improved semiconductor substrate can be achieved as, the dopant concentration of the modified first semiconductor layer is established only once the SOI type substrate itself has been prepared. Thus, during the fabrication process of the SOI substrate itself, the same kind of donor substrates like in the standard procedure can be provided. Therefore, no cross-contamination from donor wafers with different dopant concentrations is observed and the dopant profile can not be deteriorated by annealing steps in the SOI fabrication procedure.

Preferably, the dopant concentration in the modified first semiconductor layer is higher than in the second semiconductor layer. Like already mentioned this kind of substrate plays an

important role, in particular, in optoelectronic applications and with the improved dopant concentration profile which can be achieved with the inventive method, improved final products are obtained.

Advantageously, the second semiconductor layer can be epitaxially grown over, in particular on, the modified first semiconductor layer. By doing so, the quality of the substrate can be further improved.

Preferably, the modified first semiconductor layer can be a highly doped n++ or p++ semiconductor layer, thus with a dopant concentration in the range of 10^{17} atoms/cm^3 up to 10^{20}atoms/cm^3. Thus, with this method, the high dopant concentrations necessary for high quality image sensors can be achieved with an improved dopant concentration profile through the different layers.

Preferably, in step c), the second semiconductor layer is provided as an n- or p- semiconductor layer. Dopant concentrations in the range of 1 x 10^{14} to 1 x 10^{16} atoms/cm^3 can be achieved with a clear interface between the highly doped first semiconductor layer and the second semiconductor layer. Thus again, improved substrates can be achieved.

The doping, in particular by diffusion doping, and the growth of the second semiconductor layer can occur at the same time. Thus the epitaxial deposition can be achieved with the desired dopant level in one process run which has a positive impact on the dopant profile compared to prior art process in which doping occurs by implantation after the growth of a layer.

Steps b) and c), thus the doping step of the first semiconductor layer and the second layer providing step, can be carried out in the same fabrication device, in particular an epi-reactor. By doing so, the special provision of a diffusion chamber, which is usually used to dope semiconductor layers, becomes obsolete, Using an epi-reactor for both steps, thus facilitates the production line, due to the fact that one tool, like the diffusion chamber, is no longer part of the production line. In addition, in the epi-reactor the wafers are treated one by one, whereas in the diffusion chambers about 100 wafers are treated at a time.

According to a preferable embodiment, the base can be out of a transparent material. For instance, quartz-type substrates can be employed to provide the transparency of the base substrate with respect to the visible wavelength range, which is necessary for optoelectronic applications.

Advantageously, the (modified) first semiconductor layer can have a thickness in a range of 50 nm to 800 nm, preferably 55 nm to 200 nm and/or the second semiconductor layer can have a thickness in a range of up to 8 µm, and/or the insulating layer can have a thickness of 50 nm to 1500 nm, in particular 100 nm to 400 nm. With the advantageous method, it is possible to provide highly doped and lowly doped semiconductor layers within a wide range of thicknesses. In particular, it is possible to provide a thin highly doped layer in the presence of a thicker lowly doped layer while keeping the desired dopant profile.

Advantageously, the dopants used can be Sb or As. The use of these dopants limits the impact of diffusion. Even more preferably, Sb can be used, in order to limit also the impact of a phenomenon called "autodoping". After doping the first semiconductor layer to obtain the modified first semiconductor layer and during the growth of the second semiconductor layer with its lower intentional doping concentration, an unintentional doping of the second semiconductor layer can arise from the first semiconductor layer, but also from the backside of the SOI substrate , thus from the base 3, or from a dopant release from the walls of the deposition chamber walls or other parts of the chamber. Autodoping actually leads to a certain degradation of the desired doping level in the semiconductor layers, but also of the transition region of the profile thus between the highly doped and lowly doped layer. As a consequence the electrical device characteristics become negatively affected.

Preferably, the first and/or second semiconductor layer are obtained by a CVD process using chlorine (Cl) containing precursor gases. It has been observed that the more chlorine Cl is present in the precursor gases, the less the negative impact of autodoping.

According to a preferred embodiment, the process parameters, in particular growth pressure and/or growth rate and/or deposition temperature, can be chosen such as to limit the autodoping effect. Preferably, the growth pressure can be lower than 400torr or further preferred even lower than 100torr. According to a preferred variant, the growth rate can be lower than 2 micron/min or even further preferred lower than 1 micron/min. According to

another preferred variant, the deposition temperature can be higher than 1000°C or even higher than 1075°C.

Preferably, step a) can comprise the steps of: a1) providing a donor substrate, a2) providing an insulating layer on the donor substrate, a3) creating a predetermined splitting area inside the donor substrate, a4) bonding the donor substrate to the handle substrate, and a5) detaching a remainder of the donor substrate from the bonded donor handle substrate at the predetermined splitting area to thereby form the SOI substrate. With this so called Smartcut™ technology, high quality SOI wafers can be achieved and which can serve in the advantages method, even in cases when only a part of the SOI substrate leaving the production line will be used to create the substrates according to this invention.

According to a third aspect of the invention, there is provided an optoelectronic sensor, in particular an image sensor, comprising the semiconductor substrate fabricated according to the first or second aspect. As already mentioned above, the inventive methods allows to create a superior substrate which in turn will also improve the qualities of the final product, e.g. the image sensor which uses the substrate.

Advantageous embodiments of the invention will be described in the following in relation to the Figures.

Figures 1a - 1c illustrate the steps of one embodiment according to the inventive method for fabricating a semiconductor substrate, and

Figures 2a - 2b illustrate a typical dopant concentration profile in a semiconductor substrate fabricated according to the invention in comparison to one fabricated according to the prior art process.

According to step a) of the inventive method, a SOI type substrate 1 is provided as illustrated in figure 1a. One way to fabricate such a substrate 1 is the so called SmartCut™ technology. This method typically comprises the steps of providing a donor substrate, e.g. a silicon wafer or a transparent substrate like quartz, providing an insulating layer on the donor and/or on the base substrate and creating a predetermined splitting area inside the donor substrate, which is achieved by implanting atomic species or ions, like helium or hydrogen

ions, into the donor substrate. In the next step the donor substrate is bonded to a base substrate, e.g. a further silicon wafer, such the insulating layer is sandwiched between handle and donor substrate. Subsequently, the remainder of the donor substrate is detached from the bonded donor-base substrate at the predetermined splitting area following a thermal and/or mechanical treatment upon the predetermined splitting area. As a result a semiconductor on insulator (SOI) substrate is obtained. With this method, the insulating layer finds itself between the semiconductor layer transferred from the donor substrate and the base substrate. This layer then forms the abovementioned buried oxide layer (BOX).

Accordingly the SOI type substrate 1 provided in step a) of the inventive method comprises a base 3, typically silicon. However, depending on the application also other materials are suitable, like for example transparent materials, like quartz, which find their application in optoelectronic applications.

On the base 3, or on the donor, an insulating layer 5 is provided, which is typically a silicon dioxide. However, again other insulating materials like silicon nitride or a stack of layers might also form the insulating layer 5.

Over the insulating layer 5, a first semiconductor layer 7 is provided, which is typically a silicon layer. However, also for this layer, other semiconductor materials like germanium might also be used.

The thickness of the insulating layer is from about 50 nm to 1500 nm, preferably in a range of 100 nm to 400 nm. The semiconductor layer 7 typically has a thickness of 50 nm to 800 nm, preferably 55 nm to 200 nm.

According to step b) of claim 1, illustrated in figure 1b, the next step of the inventive method consists in doping the first semiconductor layer 7 to thereby obtain a modified first semiconductor layer 9. This can for example be carried out in a diffusion chamber 11, thus leading to an in-situ doping. Typically, doping is carried out with boron or phosphorous atoms to obtain n-type or p-type kinds of doping in a flow of hydrogen with temperatures of about 900 - 1200°C, preferably 1100 - 1160°C and for a time duration of 30 seconds – 4 minutes. This treatment will turn a p- semiconductor layer into a p++ semiconductor layer with a dopant concentration of 10^{17} or more Atoms/cm^3 and in case of n- semiconductor

layer as first semiconductor layer to an n++ layer with a dopant concentration of 10^{17} or more Atoms/cm^3.

The next step according to the invention (step c of claim 1) consists in providing a second semiconductor layer 13 with a different dopant concentration than the one of the modified first semiconductor layer 9. This step is typically carried out in a epi-reactor 15 and will result in second semiconductor layer 13 achieved by epitaxial growth on the modified first semiconductor layer 9. For a silicon layer, the used precursor gases can be TCS, DCS, or silane and for doping the layer, again boron or phosphorous n-type or p-type dopants are used. The growth typically takes place at a temperature of 1000 – 1200°C and a layer with a thickness of up to 8 µm can be achieved. The dopant concentration is of the order of 1 x 10^{14} to 1 x 10^{16} atoms/cm^3. Preferably, the doping is carried out during the growth of the second semiconductor layer by in-situ doping thus based on diffusion doping.

Figures 2a and 2b illustrate dopant concentration profiles of a semiconductor substrate fabricated according to the first embodiment (Figure 2a) and a substrate fabricated according to the prior art method described further above (Figure 2b).

Figure 2a illustrates the dopant concentration on the y axis versus a cross section of the substrate on the x axis. Region I of the dopant concentration corresponds to the second semiconductor layer 13 with a fairly constant dopant concentration of about 4 x 10^{14} atoms/cm^3. The second Region II corresponds to the modified first semiconductor layer 9 with a dopant concentration going up to 8 x 10^{18} atoms/cm^3. The highly doped layer 13 has actually a dopant profile which continuously, monotonically, increases and becomes rather flat towards the subsequent buried oxide layer (BOX). This layer has a thickness of 200 nm. Then, the buried oxide insulating layer 5 is represented in Region III. In the shown example, which was fabricated according to the invention, the base substrate 3 was a silicon wafer.

In contrast thereto, Figure 2b illustrates a dopant profile that is achieved with the prior art method in which a standard SOI substrate with a thin p- (or n-) semiconductor layer is used as starting material over which a further semiconductor layer with a p++ (n++) dopant concentration is provided. Like in Figure 1, Region I illustrates the lowly doped semiconductor layer with its dopant concentration of the order of 7 x 10^{14} atoms/cm^3. Subsequently, in Region II, the highly doped layer has a dopant concentration going up to 7

x 10^{18} atoms/cm^3. Then follows the thin lowly doped semiconductor layer already present on the starting SOI substrate in Region IV. This layer is thus positioned between the Regions II and the buried oxide layer region III. Due to diffusion, the lowly doped thin semiconductor layer in Region IV has seen its dopant concentration increasing, so that, in the end, the dopant profile of the highly doped layer in Region II first grows (seen from Region I) and then decreases again towards the buried oxide layer. Comparing the two profiles, it appears the for the desired optoelectronic applications, the profile illustrated in Figure 2a is preferable.

According to a second inventive embodiment, the steps illustrated in Figures 1b and 1c are carried out in the same device, namely in the epi-reactor 15, so that, in Figure 1b instead of doping of the first semiconductor layer 7 in an additional diffusion chamber 11, doping is carried out in the epi-reactor 15. This has the advantage that only one tool needs to be provided instead of two. Furthermore, the overall fabrication process is easier to carry out as in the epi-reactor, one wafer after the other is treated, whereas in the diffusion chamber 11, approximately 100 wafers are treated at the same time. By, in particular, providing the desired dopant level of the second semiconductor layer 13 at the same time as the layer is grown, the desired abrupt change over from high to low doped regions is achieved. This abrupt change like illustrated in Figure 1 cannot be achieved with doping using implantation.

With the described inventive method, the following advantages can be achieved with respect to the known methods in the prior art. With respect to the process for fabricating a semiconductor substrate which starts from a SOI substrate with a p++ or n++ first semiconductor layer, the present invention brings the advantage that dopant cross-contamination risk between lowly doped and highly doped SOI wafers within one manufacturing line can be eliminated and furthermore, due to the doping of the first semiconductor layers 7 in an own doping step, a tailor-made dopant profile can be achieved which is independent of the starting SOI material.

With respect to the method in which the starting material is a standard SOI substrate with a p- semiconductor layer over which a p++/n++ first semiconductor layer is epitaxially grown and over which in turn the p-/n- second layer will be grown is that, with the inventive method, a higher doping concentration can be achieved inside the p++/n++ modified first semiconductor layer 9 and, in addition, the concentration profile in the p++/n++ layer 9 can

be kept essentially flat or at least evolves monotonically over its thickness (see figure 2a), whereas it decreases and then increases within the p++/n++ layer with prior art technique (see figure 2b).

Thus, with the inventive method, superior semiconductor substrates can be achieved, which find their application in optoelectronics, in particular in image sensors. With the inventive method it is furthermore possible to have a large process window in terms of doping species, which in addition do not depend on the starting SOI substrate, and to have tailor-made doping levels, which do not depend on the bulk material available.

A third inventive embodiment, further improves the dopant concentration profile by reducing the impact of a phenomenon called "autodoping".

After doping the first semiconductor layer 7 to obtain the modified first semiconductor layer 9 and during the growth of the second semiconductor layer 13 with its lower intentional doping concentration, an unintentional doping of the second semiconductor layer 13 can arise from the first semiconductor layer. Autodoping may also arise from the backside of the SOI substrate 1, thus from the base 3, but also from a dopant release from the walls of the deposition chamber walls or other parts of the chamber. Autodoping actually leads to a certain degradation of the desired doping level in the layers 9 and 13, but also of the transition region of the profile thus between the highly doped 9 and lowly doped layer 11 and which has an impact on the electrical device characteristics.

The autodoping proceeds through a two steps mechanism: out-diffusion of the dopants from the material into the chamber and then re-incorporation of the dopants during the subsequent growth of the second semiconductor layer 13.

According to the third embodiment invention out-diffusion can be reduced by optimizing the deposition parameters of the first and/or second semiconductor layer, e.g. the bake pressure, the bake temperature, the bake time, in situ etch, the deposition pressure, the deposition temperature or the surface gas velocity.

For instance with a growth pressure of lower than 400torr or even lower than 100torr, a growth rate lower than 2 micron/min or even further preferred lower than 1 micron/min and a

deposition temperature higher than 1000°C or even higher than 1075°C the autodoping effect can be reduced.

Instead or in addition, the method according to the third embodiment uses optimized deposition precursors and/or dopants. Instead of using boron or phosphorous atoms as dopants, the method according to the third embodiment uses arsenic As or even further preferred antimony Sb, for which a reduced autodoping phenomenon has been observed which is attributed to a reduced out-diffusion. On the precursor side, it is preferred to use silicon precursor molecules containing chlorine Cl instead of using silane. The more Cl atoms in the molecule the lower the impact of autodoping. Thus SiH4 is worse than SiH3Cl which in turn is worse than SiH2Cl2 which is worse than SiHCl3 which again is worse than SiCl4.

Finally, when the desired doping level and doping profile in the first and second semiconductor layer 9 and 13 are achieved, a subsequent degradation can be prevented or at least kept lower by optimizing the subsequent thermal treatments. On the one side this can be achieved by limiting the total thermal budget in time or temperature or to use the above mentioned dopants Sb or As rather than B or P with their lower diffusion coefficient.

Claims

1. Method for fabricating a semiconductor substrate comprising the steps of:
   a) providing a silicon on insulator type (SOI) substrate comprising a base, an insulating layer and a first semiconductor layer,
   b) doping the first semiconductor layer to thereby obtain a modified first semiconductor layer, and
   c) providing a second semiconductor layer with a different dopant concentration than the modified first semiconductor layer over, in particular on, the modified first semiconductor layer,

   wherein doping, in particular by diffusion doping, and growth of the second semiconductor layer occur at the same time.

2. Method for fabricating a semiconductor substrate comprising the steps of:
   a) providing a silicon on insulator type (SOI) substrate comprising a base, an insulating layer and a first semiconductor layer,
   b) doping the first semiconductor layer to thereby obtain a modified first semiconductor layer, and
   c) providing a second semiconductor layer with a different dopant concentration than the modified first semiconductor layer over, in particular on, the modified first semiconductor layer,

   wherein step b) and c) are carried out in the same fabrication device, in particular an epi-reactor.

3. Method according to claim 1 or 2, wherein the dopant concentration in the modified first semiconductor layer is higher than in the second semiconductor layer.

4. Method according to one of claims 1 to 3, wherein the second semiconductor layer is epitaxially grown over, in particular on, the modified first semiconductor layer.

5. Method according to one of claims 1 to 4, wherein after doping, the modified first semiconductor layer is a highly doped n++ or p++ semiconductor layer.

6. Method according to one of claims 1 to 5, wherein in step c) the second semiconductor layer is provided as a n- or p- semiconductor layer.

7. Method according to one of claims 1 to 6, wherein the base is out of a transparent material.

8. Method according to one of claims 1 to 7, wherein the modified first semiconductor layer has a thickness in a range of 50nm to 800nm, preferably 55 nm to 200 nm, and/or the second semiconductor layer has a thickness in a range of up to 8µm, and/or the insulating layer has a thickness of 50nm to 1500nm, in particular 100nm to 400nm.

9. Method according to one of claims 1 to 8, wherein the dopants used are Sb or As.

10. Method according to one of claims 1 to 9, wherein the first and/or second semiconductor layer are obtained by a CVD process using chlorine containing precursor gases.

11. Method according to one of claims 1 to 10, wherein the growth pressure is lower than 400torr, in particular lower than 100torr, and/or the growth rate is lower than 2 micron/min, in particular lower than 1 micron/min, and/or the deposition temperature is higher than 1000°C, in particular higher than 1075°C.

12. Method according to one of claims 1 to 11, wherein step a) comprises:
    a1) providing a donor substrate,
    a2) providing an insulating layer on the donor substrate or a base substrate,
    a3) creating a predetermined splitting area inside the donor substrate,
    a4) bonding the donor substrate to the base substrate, and
    a5) detaching a remainder of the donor substrate from the bonded donor-base substrate at the predetermined splitting area to thereby transfer a layer of the donor substrate including the insulating layer onto the base substrate to form the SOI substrate.

13. Opto-electronic sensor, in particular image sensor, comprising the semiconductor substrate fabricated according to one of claims 1 to 12.