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ACTIVE MATRIX DISPLAY DEVICE AND ITS DRIVING METHOD

BACKGROUND OF THE INVENTION

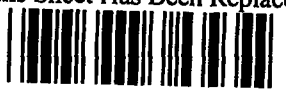
Field of the Invention

This invention relates to an active matrix display device and its driving method. More particularly, this invention relates to an anti-potential oscillation technology in a video line in a spot sequential driving operation.

Description of Related Art

Referring now to Fig. 8, a configuration of the prior art active matrix display device will be described in brief. The active matrix display device is comprised of gate lines X of row, signal lines Y of column and liquid crystal pixels LC in matrix arranged at each of crossing points of both lines. Each of the liquid crystal pixels LC is driven by a thin film transistor Tr. V driver (a vertical scanning circuit) 101 performs a line sequential scanning of each of the gate lines X and selects the liquid crystal pixel LC on one line for every one horizontal period (1H). The H driver (a horizontal scanning circuit) 102 samples in sequence the video signals VSIG in one line within 1H in each of the signal lines Y and writes the video signals

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VSIG in the liquid crystal pixels LC in one selected line in spot sequence. More practically, each of the signals lines Y is connected to the video line through the horizontal switch HSW, receives a supplying of the video signal VSIG from the signal driver 103 and in turn the H driver 102 outputs horizontal sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3}, ... ϕ_{HN} in sequence and controls ON or OFF of each of the horizontal switches HSW.

Fig. 9 expresses waveforms of sampling pulses. As the active matrix display device is made to be highly accurate in operation, the sampling rate is made fast and the sampling pulse width τ_H becomes disturbed. As the sampling pulse is outputted, its corresponding horizontal switch HSW is turned on or off and the video signal VSIG from the video line is sampling held in the corresponding signal line Y. Each of the signal lines Y has a capacitor component and its charging or discharging is produced by the sampling of the video signal VSIG. As a result, the potential in the video line is varied. As described above, as the sampling rate is made fast, the sampling pulse width τ_H is disturbed, so that a charging or discharging in respect to each of the signal lines Y is not made constant and the potential at the video line is oscillated. There

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occurs a problem that this state appears as a vertical fixed pattern and remarkably damages quality of the displayed video image. In the case of displaying in accordance with the normal NTSC Standards, the sampling rate is relatively low and shows a timing in which a next sampling pulse is raised after ending of the potential oscillation in the video line, so that a vertical fixed pattern does not appear due to no bad influence against the previous signal line. However, in the case of HDTV or a double-speed NTSC, the sampling rate is rapidly increased and an effective restriction of a potential oscillation in the video line is difficult to perform. The sampling pulse is in general generated by the H driver comprised of shift registers or the like constituted by TFTs. Since TFT has a lower mobility as compared with that of a monolithic silicon transistor and also has a higher disturbance in each of the physical constants, it is difficult to perform an accurate control over the sampling pulses generated by this circuit. In addition, a certain disturbance may occur in ON resistance of the horizontal switch HSW in addition to the disturbance of the sampling pulse width. With such an arrangement as above, there occurs a variation in charging or discharging characteristic in

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the signal line Y and the video line potential is oscillated, so that this is overlapped on the actual video signal VSIG, appears as a vertical line to make a remarkable damage in quality of displaying the video signal.

SUMMARY OF THE INVENTION

In view of the aforesaid technical problems found in the prior art, it is an object of the present invention to perform an effective restriction of a potential oscillation in the video line generated as the sampling rate is increased. In order to accomplish the aforesaid object, the present invention has provided the following means. That is, the active matrix display device of the present invention is provided with gate lines in row, signal lines in column and matrix pixels arranged at each of the crossing points of both lines as its basic configuration. In addition, there is also provided a vertical scanning circuit, wherein each of the gate lines is scanned in sequence in line and pixels in one line are selected for every one horizontal period. There is also provided a horizontal scanning circuit, wherein the video signals are sampled in sequence at each of the signal lines within one

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horizontal period, and performs writing of video signals by dot sequential scanning on the selected pixels in one line. As a feature of the present invention, there is provided a precharging means and the predetermined precharging signals are supplied in sequence to each of the signal lines prior to the sequential sampling of the video signal corresponding to each of the signal lines.

More practically, the aforesaid precharging means is comprised of a plurality of switching elements connected to each of the terminal ends of the respective signal lines and a control means for controlling in sequence ON or OFF of each of the switching elements and supplying a precharging signal to each of the signal lines. This control means is comprised of an additional horizontal scanning circuit separately installed from the horizontal scanning circuit, wherein each of the switching elements is controlled in sequence in its ON or OFF state. Alternatively, the control means may be constructed such that its output is distributed and each of the switching elements is controlled in sequence for its ON or OFF state.

The precharging means supplies a precharging signal having a grey level in respect to the video signal varying between the white level and the black

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level. Alternatively, the precharging means may be constructed to supply the precharging signal having the same polarity and the same waveform as those of the video signal.

The present invention includes a method for driving the active matrix display device. That is, the driving method in accordance with the present invention is characterized in that it performs a vertical scanning for scanning linearly in sequence of each of the gate lines and selecting pixels in one line for every one horizontal period, a horizontal scanning for sampling in sequence the video signals in one horizontal period to each of the signal lines and writing the video signals by dot sequential scanning to the pixels in one selected line, and a precharging for supplying in sequence a predetermined precharging signal to each of the signal lines prior to the sequential sampling of the video signals in respect to each of the signal lines.

According to the present invention, the charging or discharging of each of the signal lines is almost completed with the precharging signal, and the charging or discharging in case of performing the sampling of the video signals is carried out such that it may occur only at a difference between the

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precharging level and the signal level. Accordingly, the potential oscillation in the video line for supplying the video signals is restricted more as compared with that of the prior art and then the vertical fixed pattern becoming a problem in keeping video quality can be eliminated. In particular, in the present invention, the precharged signals are sampled by so-called dot sequential scanning to each of the signal lines. As compared with the case that the precharged signals are all sample held in all signal lines, the potential oscillation at the gate lines or power source line can be reduced. In addition, a less driving capability of the precharging means is also satisfactory.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram for showing the first preferred embodiment of the active matrix display device.

Fig. 2 is a timing chart applied for illustrating an operation in the first preferred embodiment.

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Fig. 3 is a circuit diagram for showing the second preferred embodiment of the active matrix display device of the present invention.

Fig. 4 is a timing chart applied for illustrating an operation of the second preferred embodiment.

Fig. 5 is a circuit diagram for showing an example of practical configuration of the second preferred embodiment.

Fig. 6 is a circuit diagram for showing another practical example of configuration of the second preferred embodiment.

Fig. 7 is a timing chart applied for illustrating an operation of the configuration shown in Fig. 6.

Fig. 8 is a circuit diagram for showing the configuration of the prior art active matrix display device.

Fig. 9 is a waveform view applied for illustrating the problem.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings, the preferred embodiments of the present invention will be described

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in detail. Fig. 1 is a circuit diagram for showing the first preferred embodiment of the active matrix display device of the present invention. The active matrix display device is comprised of gate lines X in row, signal lines Y in column and liquid crystal pixels LC in matrix arranged at each of the crossing points in both lines. In this preferred embodiment, there are provided pixels LC utilizing liquid crystal as electro-photo substance. However, the present invention is not limited to this embodiment, but other electro-optical substances may be utilized. There are provided thin film transistors Tr for use in driving each of the liquid crystal pixels LC. The source electrode of the thin film transistor Tr is connected to the corresponding signal line Y, the gate electrode is connected to the corresponding gate line X and the drain electrode is connected to the corresponding liquid crystal pixel LC.

There is provided a V driver 1 so as to constitute the vertical scanning circuit, and each of the gate lines X is scanned in line at a time and a liquid crystal pixel LC in one line is selected for every one horizontal period. More practically, the V driver 1 transfers the vertical start signal VST in

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sequence in synchronous with the vertical clock signal VCK and outputs the selection pulses ϕ_{V1}, ϕ_{V2}, ... ϕ_{VM} to each of the gate lines X. With such an arrangement as above, the thin film transistor Tr is controlled in its ON or OFF state.

In addition, there is provided a H driver 2 so as to constitute the horizontal scanning circuit in which the video signals VSIG are sampled in sequence to each of the signal lines in one horizontal period and the video signals VSIG are written by dot sequential scanning to the liquid crystals LC of selected one line. More practically, one end of each of the signal lines Y is provided with horizontal switching elements HSW1, HSW3, HSW4, ... HSWN, connected to each of the video lines 3 so as to receive the video signals VSIG. In turn, the H driver 2 transfers in sequence the horizontal start signal HST in synchronous with the predetermined horizontal clock signal HCK and outputs the sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3}, ϕ_{H4} ... ϕ_{HN}. These sampling pulses control ON or OFF of the corresponding horizontal switching elements and sample holds the video signals VSIG to each of the signal lines Y.

As a feature of the present invention, there is provided a precharging means 4, a predetermined

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precharging signal VPS is supplied in sequence to each of the signal lines Y prior to the sequential sampling of the video signal VSIG in respect to each of the signal lines Y and then a charging or a discharging of each of the signal lines Y through sampling is restricted. With such an arrangement as above, a less potential oscillation of the video line 3 occurs. More practically, the precharging means 4 has additional switching elements PSW1, PSW2, PSW3, PSW4, ... connected to the terminal end of each of the signal lines Y. In addition, there is provided a P driver 5 so as to constitute a control means for controlling in sequence ON or OFF of the additional switching elements PSW and supplying the precharging signal VPS to each of the signal lines Y. More practically, the P driver 5 has a similar configuration to that of the H driver 2, wherein the horizontal start signal PST is transferred in sequence in synchronous with the horizontal clock signal PCK, and then precharging sampling pulses ϕ_{P1}, ϕ_{P2}, ϕ_{P3}, ϕ_{P4}, ... ϕ_{PN} are outputted. The additional horizontal switching elements PSW are controlled in sequence for their ON or OFF state in response to these precharging sampling pulses. In the preferred embodiment, the control means is comprised of the horizontal scanning

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circuit having the additional P driver 5 separate from the H driver 2, wherein each of the switching elements PSW is controlled in its ON or OFF state in sequence. In addition, the horizontal scanning circuit such as the H driver 2 or the P driver 5 has as its basic configuration shift registers, wherein either the thin film transistors or monolithic silicon transistors are integrated. The switching element HSW for the video signal sampling or the switching element PSW for the precharging signal sampling can be constructed by NMOS, PMOS and CMOS. In the preferred embodiment, although the H driver 2 and the P driver 5 are separately arranged at both ends of the signal line Y, the H driver 2 and the P driver 5 may be integrated at the same side. In this case, the horizontal switches HSW and PSW are also arranged at one end of the signal line Y.

Then, referring to Fig. 2, operation of the active matrix display device shown in Fig. 1 will be described in detail. As described above, the P driver 5 transfers in sequence the start signal PST in synchronous with the horizontal clock signal PCK and outputs the precharging sampling pulses ϕ_{P1}, ϕ_{P2}, ϕ_{P3}, and ϕ_{P4}. Similarly, the H driver 2 also transfers the horizontal start signals HST in synchronous with the

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horizontal clock signal HCK and outputs the sampling pulses ϕ_{H1}, ϕ_{H2}, and ϕ_{H3}. In the preferred embodiment, as the signals HCK and PCK, the same horizontal clock signals are used. In turn, the horizontal start signal is operated such that its PST operates first and then its HST operates. With such an arrangement as above, the sampling pulse for the precharging signal is always preceded in advance only by 1 sampling timing as compared with the sampling for the video signal.

The video signal VSIG is supplied to the H driver 2 and a precharging signal VPS is supplied to the P driver 5. As shown in the timing chart of Fig. 2, the video signal VSIG has a waveform varying between a white level and a black level. In turn, the precharging signal VPS has a specified potential of a grey level. In light of this state, the precharging signal VPS having the same polarity and the same waveform as those of the video signal VSIG may be used. Applying the same waveform in VSIG and VPS reduces remarkably a charging or discharging amount at the signal line and the potential oscillation at the video line 3 can be effectively restricted. Provided in the case that the same waveform is used in VSIG and VPS, the signal is not branched from the common video driver, but it is

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necessary to prepare a respective separate signal source. In turn, in the case that the specified voltage waveform of grey level is used as the precharging signal, a slight charging or discharging is produced at the sampling time of the video signal, although the charging or discharging amount of the signal line can be remarkably reduced as compared with that of the case in which the video signal having an opposite polarity such as in the case of 1H reversing driving operation.

At the lowest stage of the timing chart shown in Fig. 2 are expressed variations of potentials VY1, VY2 and VY3 of each of the signal lines Y. Taking account of the initial signal line Y1 shows that ϕ_{P1} is outputted before ϕ_{H1} is outputted, so that the precharging level is sampled at first at the signal line Y1 and then the video signal level is sampled. This operation is performed in sequence to the second and subsequent signal lines to enable a high quality displaying having no vertical stripe to be attained. In the present invention, the charging or discharging to Y1, Y2, Y3....are almost finished with the precharging signal VPS and the charging or discharging with VSIG is produced only with a difference between the precharging level and the video signal level. At this time, the

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precharging signal VPS is sampled by so-called dot sequential scanning to each of the signal lines Y. Merits of this system consist in the fact that the precharging signal VPS is sample held at all signal lines, resulting in that the gate line X and the power source line are not oscillated. Since the load capacity as viewed from the line of the precharging signal VPS is reduced, so that a resistance in the precharging signal line, a size of the added switching element PSW and a driving capability of the P driver and the like can be reduced.

In the preferred embodiment, although the vertical scanning circuit is constructed to output selection pulses to gate lines in such a manner that each of the gate lines is scanned in sequence in a linear way and some pixels in one line are selected for every horizontal period, it may also be applicable that the pixels in more than two lines are concurrently selected.

Fig. 3 is a circuit diagram for showing the second preferred embodiment of the active matrix display device of the present invention. Basically,the second preferred embodiment has the similar configuration to that of the first preferred embodiment shown in Fig. 1,

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wherein the corresponding reference numerals are added to the corresponding portions and their understanding is facilitated. In the preferred embodiment, one end of each of the signal lines Y is provided with the sampling switching element HSW for the video signal VSIG and the sampling switching element PSW for the precharging signal VPS. These switching elements HSW and PSW are commonly controlled by the H driver 2 for their ON or OFF state. That is, the preferred embodiment is different from the previous preferred embodiment, wherein the P driver used in the sampling hold of the precharging signal VPS is eliminated and its configuration is made more simple. A sampling pulse D outputted from each of the stages of the H driver 2 is applied for use in controlling ON or OFF of HSW corresponding to each of the stages and concurrently it performs a control over ON or OFF of the PSW belonging to the next stage. In other words, the control means is assembled in the horizontal scanning circuit, its sampling pulse output is properly distributed to control in sequence ON or OFF of each of the switching elements HSW, PSW.

Referring now to the timing chart shown in Fig. 4, operation of the second preferred embodiment

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shown in Fig. 3 will be described in detail. At first, as the H driver 2 outputs the first sampling pulse D1, PSW1 is controlled for its ON or OFF state. Subsequently, as the second sampling pulse D2 is outputted, HSW1 and PSW2 are concurrently controlled for their ON or OFF state. As apparent from these facts, taking account into the first signal line Y1 causes PSW1 to be driven for its ON or OFF state, thereafter HSW1 is driven for its ON or OFF state. In addition, as the third sampling pulse D3 is outputted, HSW2 and PSW3 are concurrently driven for their ON or OFF state. Lastly, as DN is outputted, HSWN-1 and PSWN are concurrently driven for their ON or OFF state. The video signal VSIG supplied from the video line 3 and the precharging signal VPS supplied from the precharging line 6 are sampling held at each of the signal lines Y in response to the driving for ON or OFF state of these switching elements HSW and PSW. For example, taking into account the potential VY1 appeared at the first signal line causes VPS to be sampling held during a precharging period of making PSW1 to be ON and subsequently VSIG is sampled for a video writing period in which HSW1 becomes ON. In addition, taking into account the potential VY2 appearing the second signal line causes the precharging

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level to be written at a timing of making PSW2 ON and then the video signal level is written at a timing in which HSW2 subsequently becomes ON.

As described above, in the preferred embodiment, the charging or discharging for the signal line Y is almost completed through the precharging line 6, the charging or discharging through the video line 3 merely corresponds to a difference between the precharging level (VPS) and the video signal level (VSIG), resulting in that the potential oscillation of the video line 3 can be reduced and the vertical fixed pattern can be improved. In the preferred embodiment above, although the sampling pulse for driving PSW is taken out from the stage before the H driver 2, the present invention is not limited to its operation. As long as the time band is of one in which a polarity of the video signal is not changed, it is satisfactory that the sampling pulse can be taken from any stages before the H driver 2. In the preferred embodiment as above, since the precharging is carried out by dot sequential scanning for each of the signal lines, no sub-action for the video quality caused by writing of the precharging signal VPS at once is found. For example, as the precharging signals are all sampling held for all signal

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lines at once, a potential at the gate signal is oscillated due to a capacitance coupling, resulting in that a leak of the video signals written into the liquid crystal pixels may occur to cause a shading or a lateral stripe to be generated. In the worst case, a lack of bright point may occur in the case of normal white mode due to a leakage of electrical load written into it. Not only potential oscillation at the gate lines can be restricted, but also no oscillation occurs at the power source line or the earth line and an operating margin is expanded. In addition, since the capacity as viewed from the precharging line 6 is less in its value, a design margin can be expanded. With such an arrangement as above, a high quality video can be obtained and a driving margin can be expanded.

Fig. 5 is a circuit diagram for illustrating a practical example of the second preferred embodiment shown in Fig. 3. As shown in this figure, HSW and PSW are constructed as transmission gates in the preferred embodiment. In addition, the H driver 2 is comprised of the H shift register 7 and the output gate 8 connected to each of the stages. The output gate 8 forms the sampling pulse and its reversing pulse in response to the output of the H shift register 7 so as to drive for

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ON or OFF of each of HSW and PSW. As described above, the sampling pulse applied to PSW is supplied from one stage before the H shift register 7, so that the point sequential sampling hold of the precharging signal VPS is carried out prior to the point sequential sampling of the video signal VSG.

Fig. 6 shows a modified form of the preferred embodiment shown in Fig. 5, wherein some corresponding reference numerals are applied to the corresponding portions so as to facilitate its understanding. The basic configuration is similar to that of the preferred embodiment shown in Fig. 5. The different points are that the sampling pulse to be applied to PSW is not one before the stage, but supplied from the H shift register 7 of two stages before. In general, if there is a time in which polarities of VSIG and VPS are not reversed, the sampling pulse applied to PSW may be taken before any stages of the H shift register.

Lastly, referring now to Fig. 7, operation of the preferred embodiment shown in Fig. 6 will be described in detail. As described above, the sampling pulses D1, D2, D3, D4, ... DN are outputted in sequence from the H register 7 through the output gate 8. When D1 is outputted, PSW1 is turned ON. Then, when D2 is

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outputted, PSW2 is turned ON. Subsequently, when D3 is outputted, PSW3 and HSW1 are turned ON. In addition, when D4 is outputted, PSW4 and HSW2 are turned ON. Lastly, when DN is outputted, PSWN and HSWN-2 are turned ON. In turn, VSIG has a waveform in which the signal level is changed in response to a video signal. In the preferred embodiment above, since 1H reversing driving is carried out, so that its polarity is reversed for every 1H. In compliance with this operation, VPS having a predetermined precharging level is also reversed for every 1H.

Taking into account the potential VY1 appearing at the first signal line shows that a precharging level is written for a precharging period in which D1 is outputted and PSW1 is turned ON. Subsequently, after elapsing 1 sampling timing, the signal level is sampling held during a period of writing actual video signal in which HSW1 is turned ON in response to the output of D3. In this case, a charging or a discharging amount of the first signal line becomes a difference between the precharging level and the signal level and it can be restricted low. In particular, the aforesaid difference is almost eliminated in the case that the same waveform as that of

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the video signal VSIG is used as the precharging signal PS. Then, taking into account the potential VY2 appearing at the second signal line shows that the precharging level is written during a precharging period in which PSW2 is turned ON in response to D2, and the signal level is sampling held during an actual video signal writing period in which HSW2 is turned ON in response to D4 in 1 sampling timing. The potential VY3 appearing at the third signal line is also similarly processed.

As described above, according to the present invention, predetermined precharging signals are supplied in sequence prior to the sequential sampling of the video signals for each of the signal lines so as to restrict the charging or discharging of each of the signal lines through the sampling. With such an arrangement as above, since the potential oscillation in the video line (noise) is substantially reduced, it has an effect that the vertical fixed pattern can be removed from the displayed image. Since the precharging is carried out by dot sequential scanning, the shooting or lateral stripe pattern can be restricted and similarly the image quality can be improved. Due to similar reasons, it has effects that an operating margin can be

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expanded and potential oscillation at the power source line or the earth line is not found. Since the vertical fixed pattern can be removed by the pre-charging, it has some effects that it is not necessary to consider the problem of minute disturbance of the sampling pulse width and that a design margin of the horizontal scanning circuit is expanded. Due to the similar reason, it has another effect that the power source voltage can be reduced and the consumption power can be saved.



What Is Claimed Is:

1. An active matrix display device comprising:

a plurality of gate lines arranged in row;

a plurality of signal lines arranged in column;

pixels arranged at each of crossing points of said gate lines and signal lines;

a vertical scanning circuit for scanning each of the gate lines in sequence and selecting pixels of at least one line;

a horizontal scanning circuit for sampling video signals in sequence and writing the video signals in sequence in the pixels in selected line; and

a precharging circuit for supplying precharging signals in sequence to each of the signal lines prior to a sequential sampling of video signals to each of the signal lines.

2. An active matrix display device according to claim 1 in which said precharging circuit is comprised of switching elements connected to an end part of each of the signal lines, and a control circuit for controlling the switching elements and supplying a precharging signal to each of the signal lines.

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3. An active matrix display device according to claim 2 in which said control circuit is an additional horizontal scanning circuit arranged independently from said horizontal scanning circuit.

4. An active matrix display device according to claim 2 in which said control circuit is assembled in said horizontal scanning circuit, distributes its output and controls each of the switching elements in sequence for its ON or OFF state.

5. An active matrix display device according to claim 1 in which said precharging circuit supplies a precharging signal having a grey level in respect to a video signal varying between a white level and a black level.

6. An active matrix display device according to claim 1 in which said precharging circuit supplies a precharging signal having the same polarity as that of the video signal.

7. An active matrix display device according to claim 1 in which said precharging circuit is arranged in opposition to said horizontal scanning circuit.

8. An active matrix display device according to claim 1 in which said precharging circuit is arranged

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at the same side as that of said horizontal scanning circuit.

9. A method for driving an active matrix device comprising gate lines arranged in row, a plurality of signal lines arranged in column, and pixels arranged at the crossing parts between said gate lines and signal lines, comprising the following steps of:

line scanning in sequence of each of the gate lines and selecting pixels for at least one row;

sampling in sequence the video signals and writing the video signals by dot sequential scanning to the pixels in one selected row; and

providing a precharging signal to each of the signal lines prior to a sequential sampling of the video signal for each of the signal lines.

10. A method for driving an active matrix device according to claim 7 in which said precharging signal is a signal having the same polarity as that of the video signal and having a grey level.

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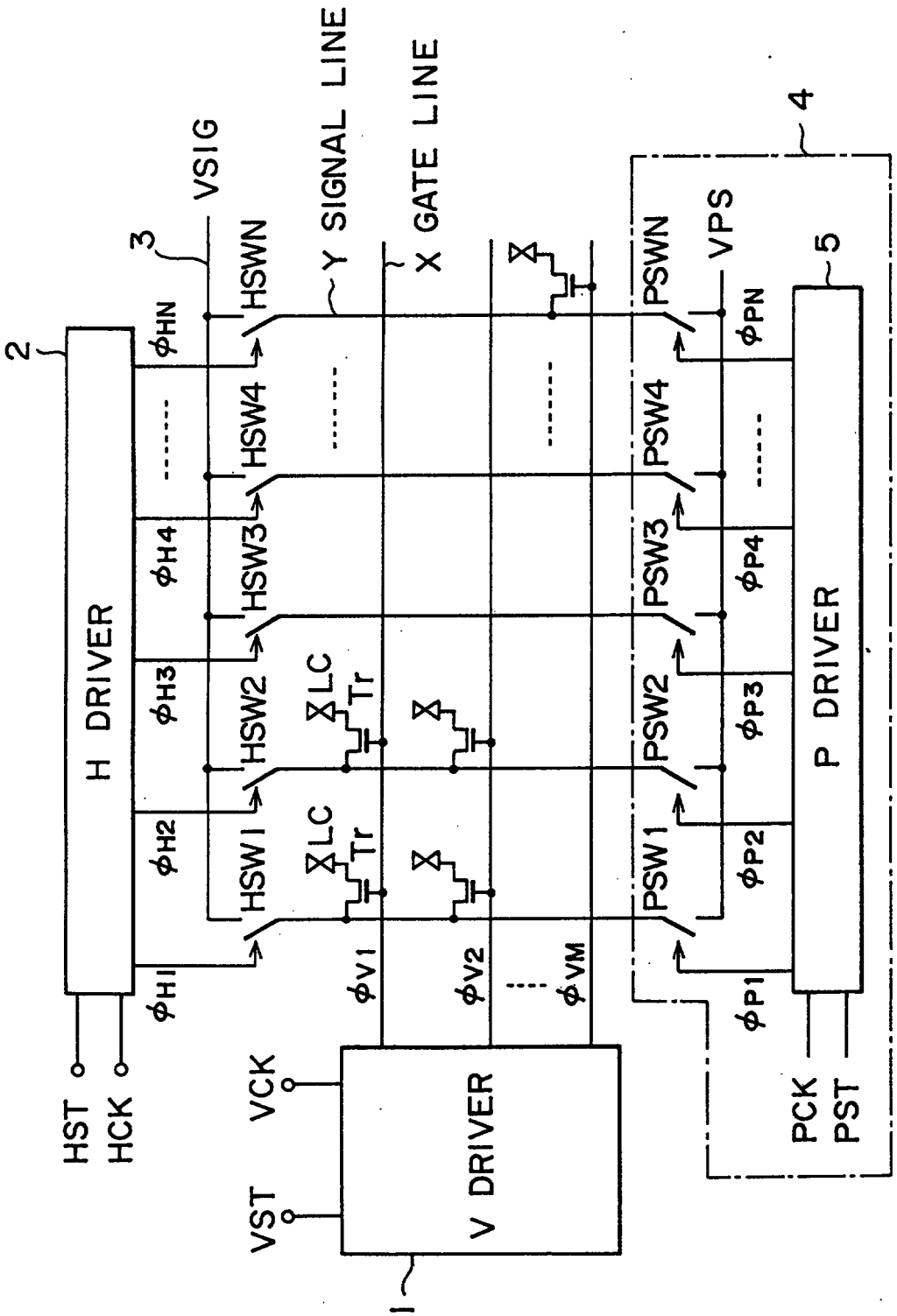
ABSTRACT OF THE DISCLOSURE

ACTIVE MATRIX DISPLAY DEVICE AND ITS DRIVING METHOD

To restrict a potential oscillation in a video line caused by a high speed sampling rate, the active matrix display device is comprised of gate lines X in row, signal lines Y in column and liquid crystal pixels LC of matrix arranged at each of the crossing points of both lines. The V driver 1 scans in line sequence each of the gate lines X and selects the liquid crystal pixels LC in one line for every one horizontal period. The H driver 2 performs in sequence samplings of the video signal VSIG within one horizontal scanning period to each of the signal lines Y and performs a writing of the video signal VSIG by dot sequential scanning to the liquid crystal pixels LC in one selected line. The precharging means 4 supplies in sequence the predetermined precharging signal VPS prior to the sequential sampling of the video signal VSIG for each of the signal lines Y. This precharging means 4 is comprised of a plurality of switching elements PSW connected to an end part of each of the signal lines Y, and of the P driver 5 for supplying the precharge signal VPS to each of the signal lines Y through sequential controlling of ON or OFF of each of the switching elements PSW.

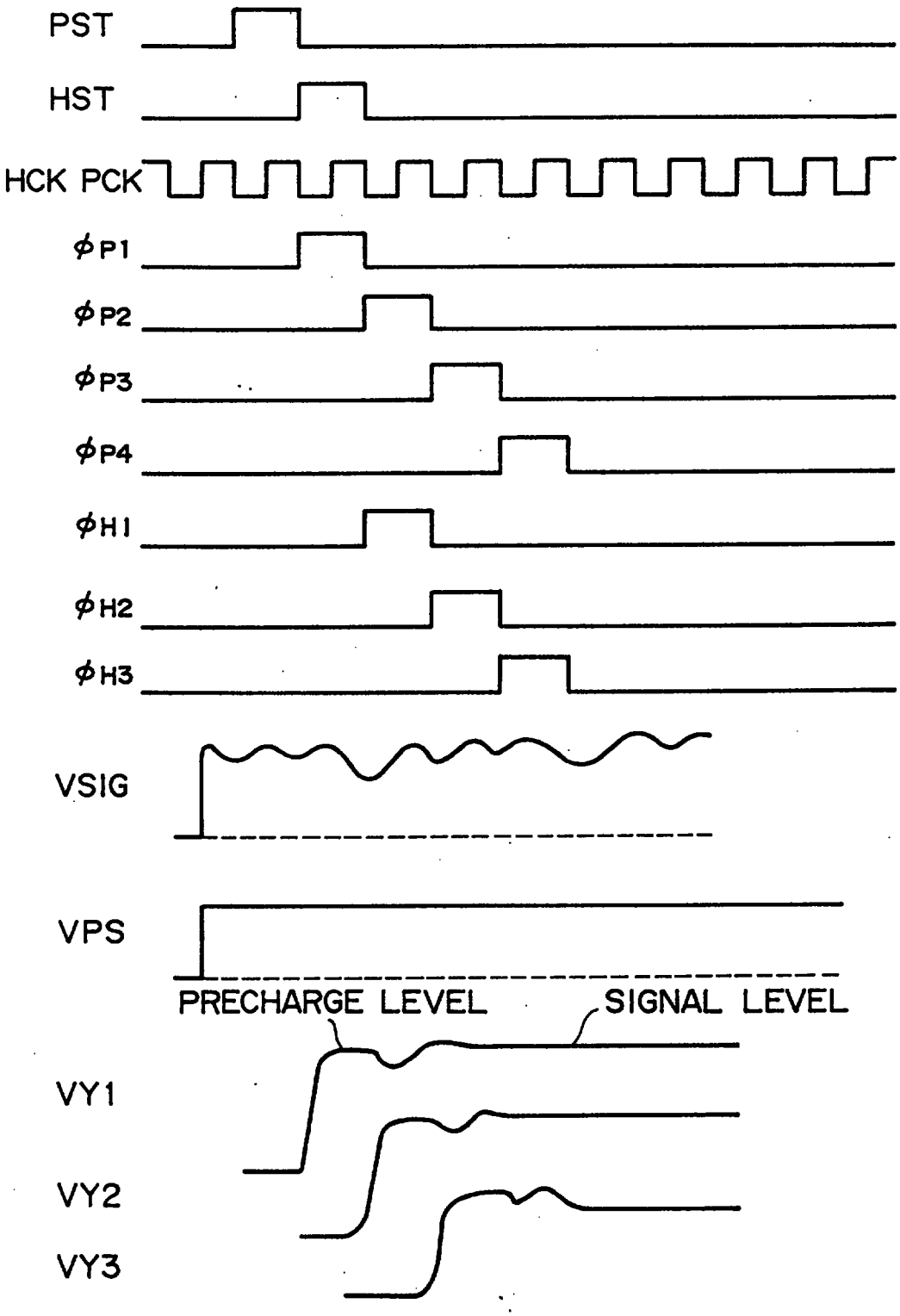
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FIG. 1



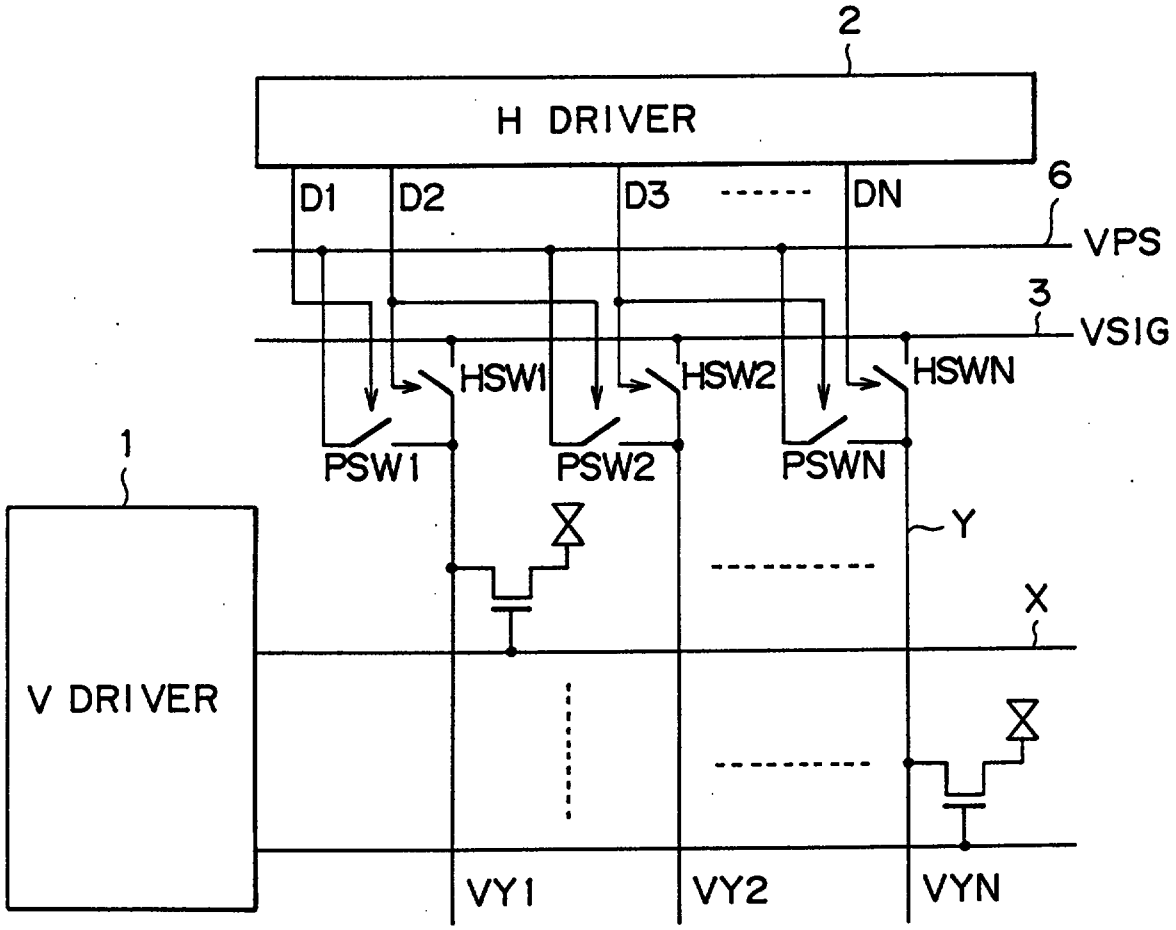
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FIG. 2



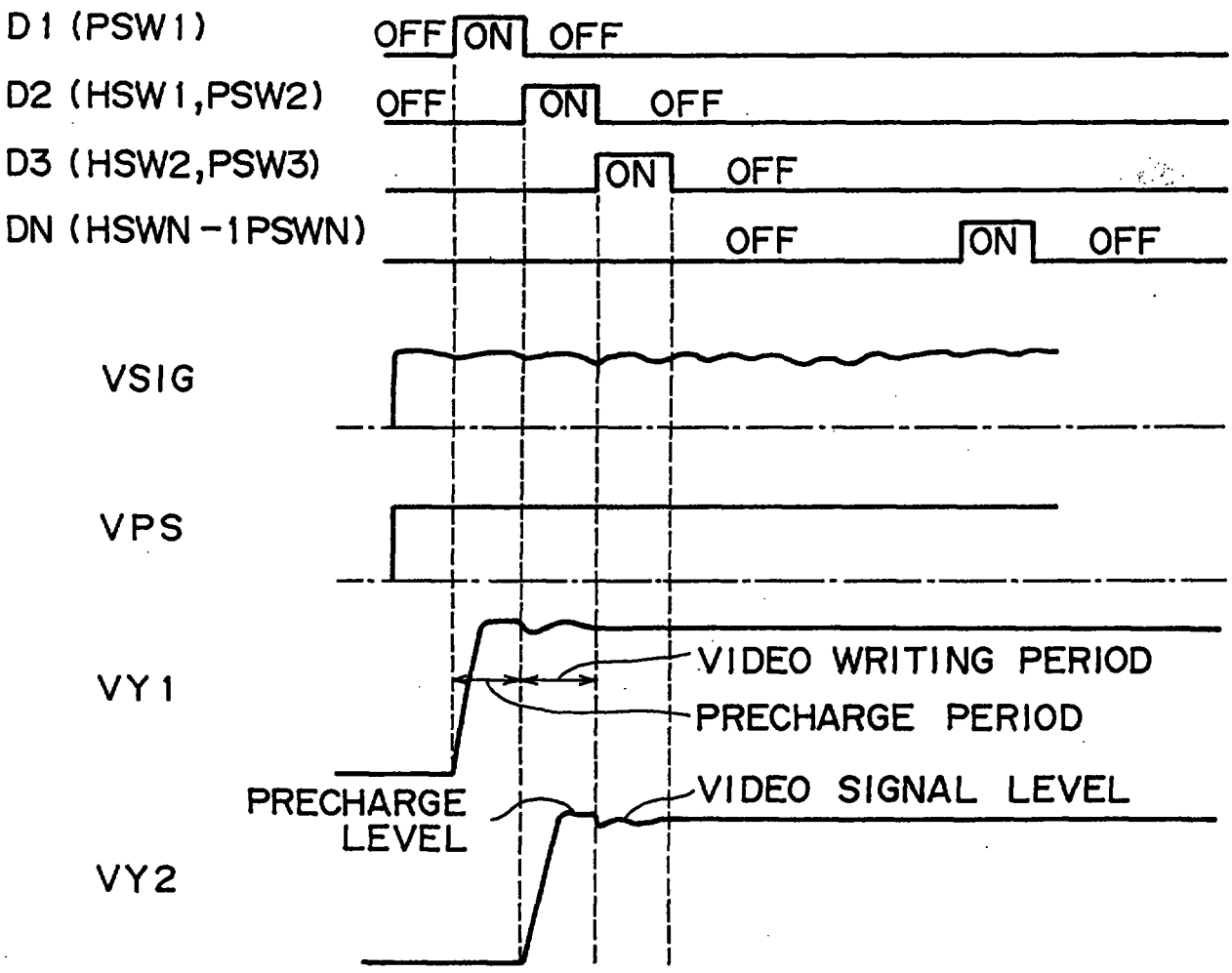
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FIG. 3



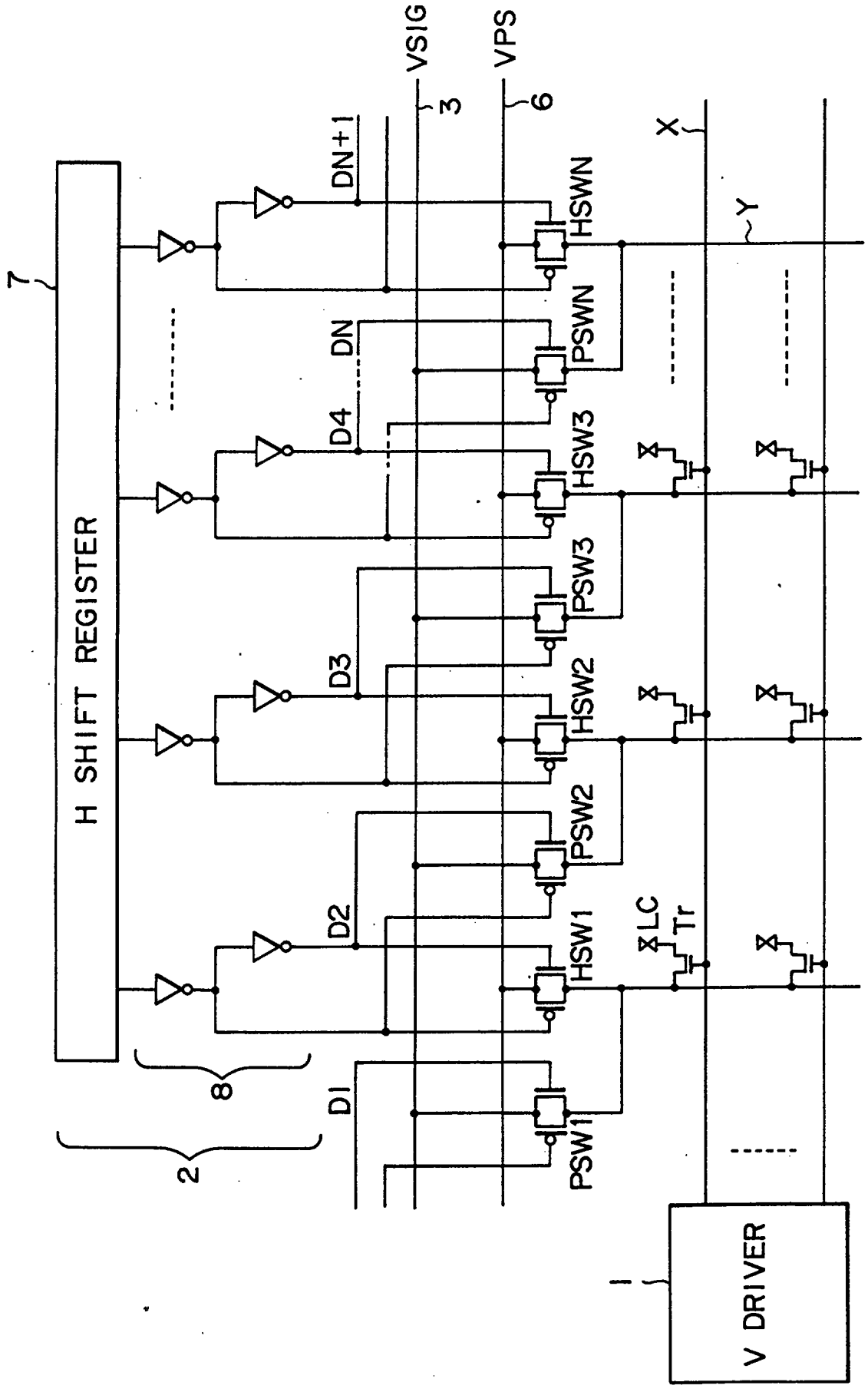
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FIG. 4



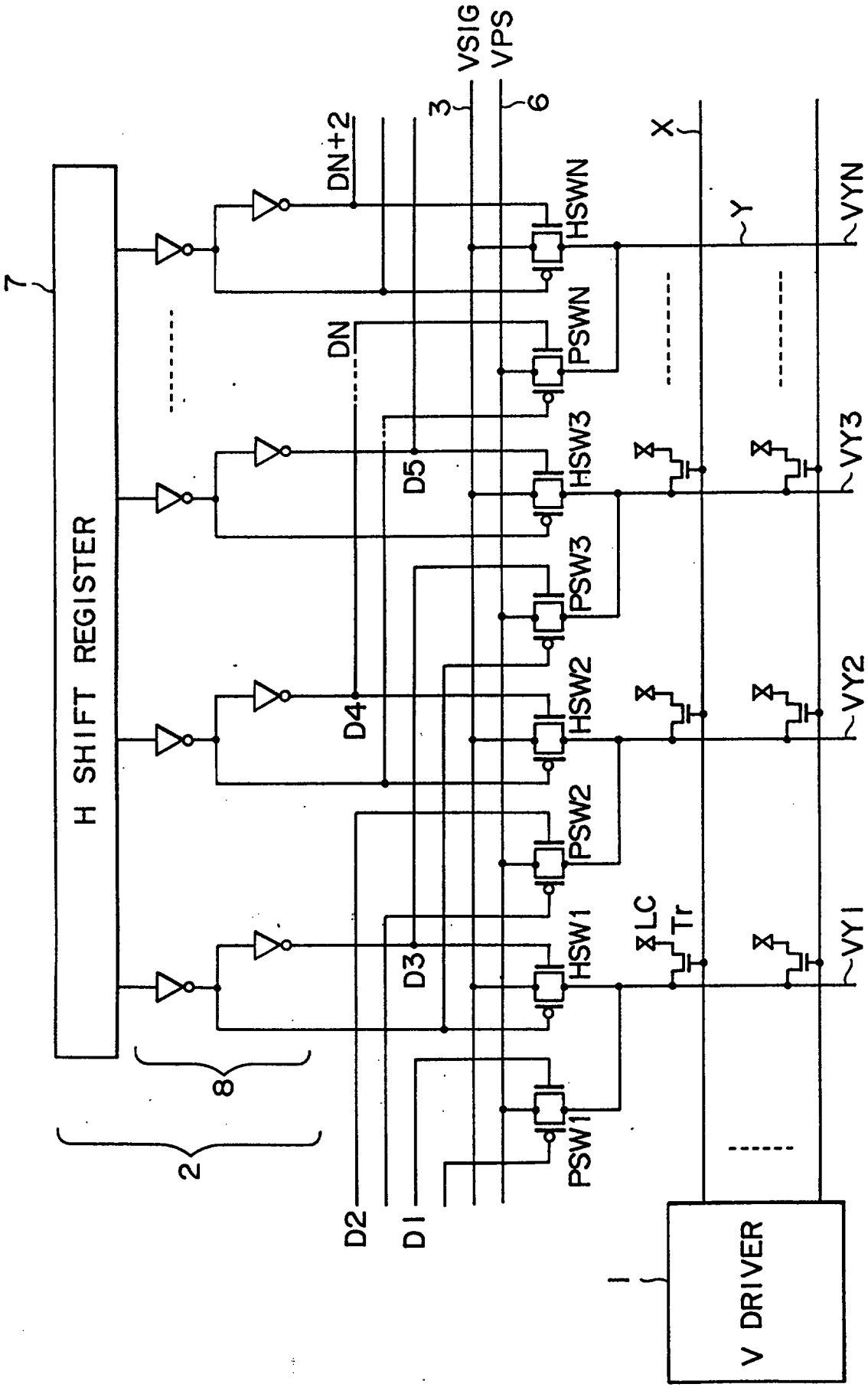
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FIG. 5



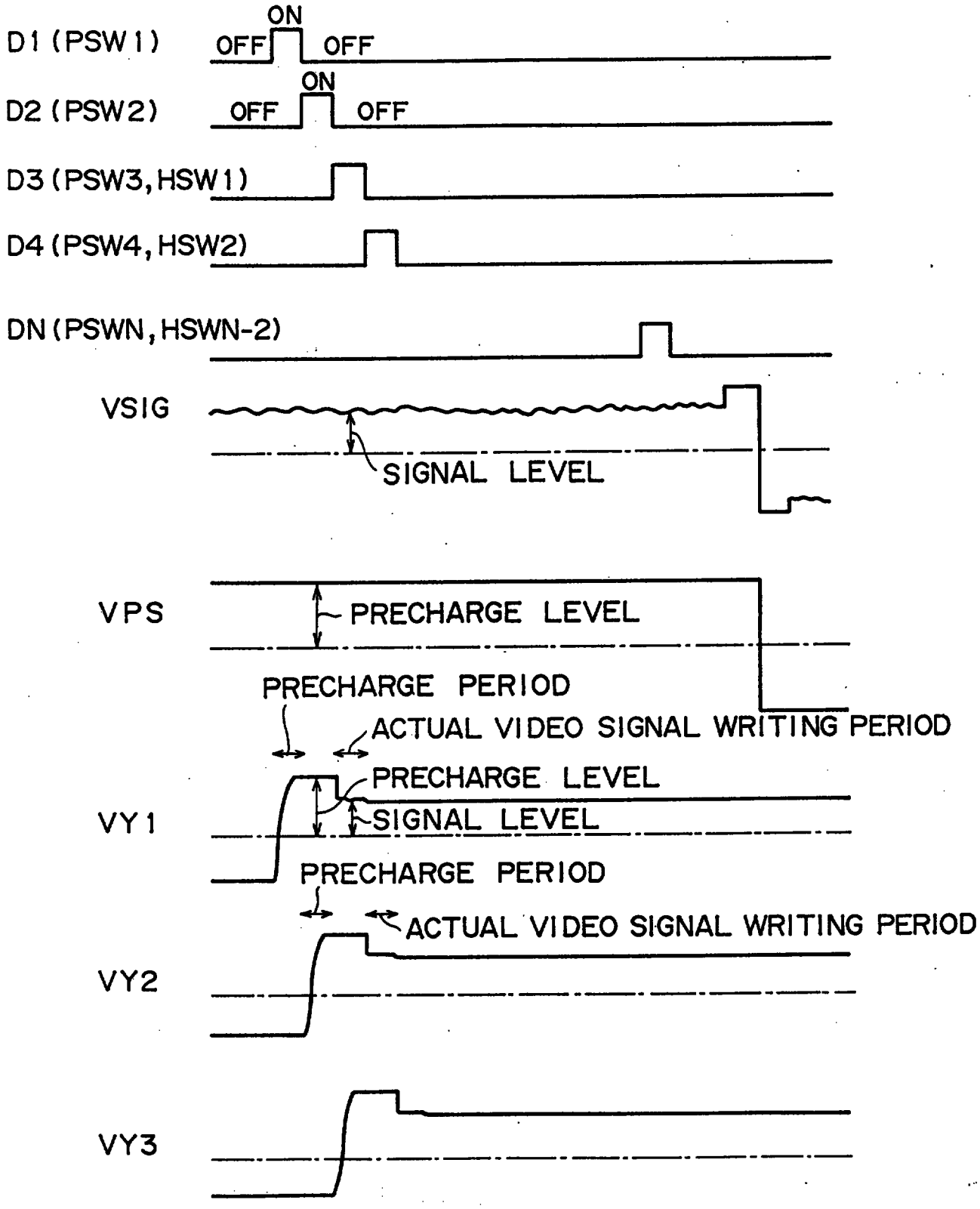
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FIG. 6



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FIG. 7



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FIG. 8

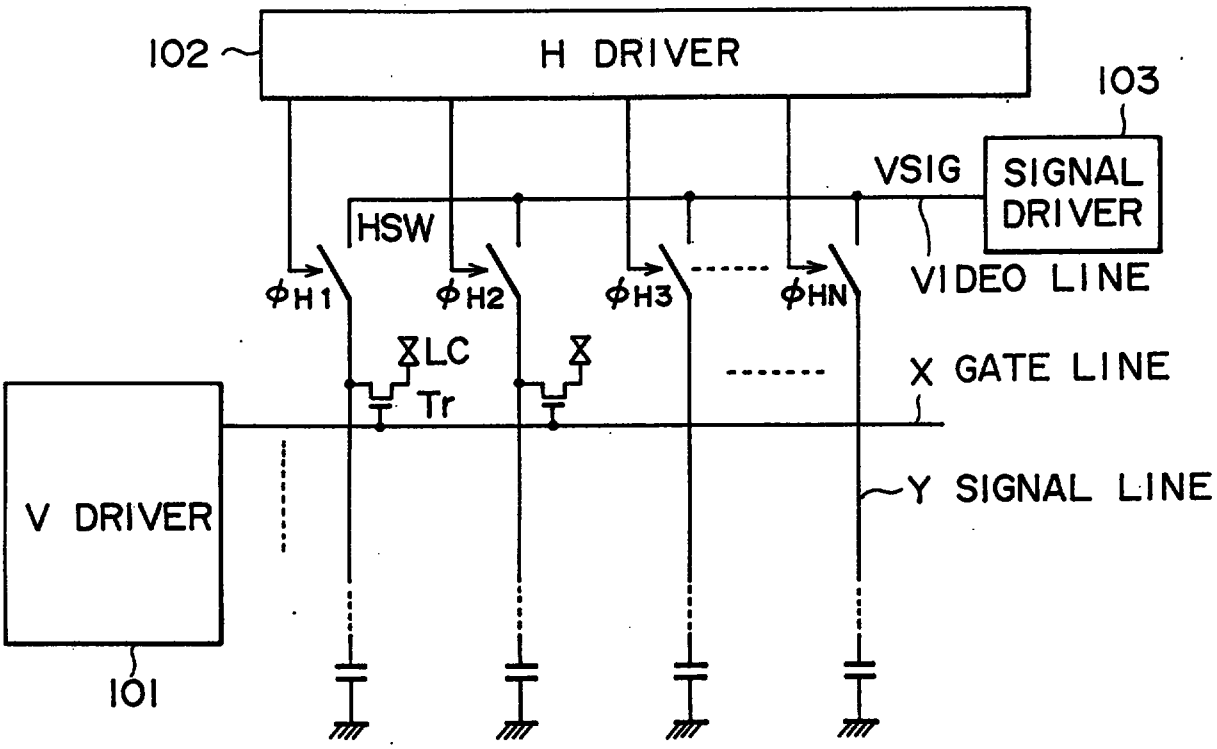
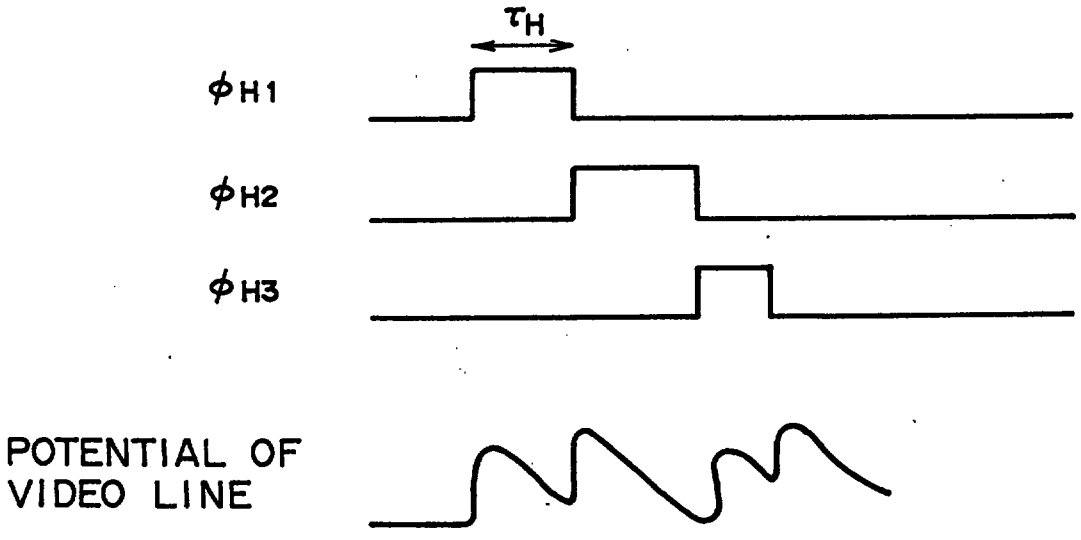


FIG. 9



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ACTIVE MATRIX DISPLAY DEVICE AND ITS DRIVING METHOD

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an active matrix display device and its driving method. More particularly, this invention relates to an anti-potential oscillation technology in a video line in a spot sequential driving operation.

Description of Related Art

Referring now to Fig. 8, a configuration of the prior art active matrix display device will be described in brief. The active matrix display device is comprised of gate lines X of row, signal lines Y of column and liquid crystal pixels LC in matrix arranged at each of crossing points of both lines. Each of the liquid crystal pixels LC is driven by a thin film transistor Tr. V driver (a vertical scanning circuit) 101 performs a line sequential scanning of each of the gate lines X and selects the liquid crystal pixel LC on one line for every one horizontal period (1H). The H driver (a horizontal scanning circuit) 102 samples in sequence the video signals VSIG in one line within 1H in each of the signal lines Y and writes the video signals

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VSIG in the liquid crystal pixels LC in one selected line in spot sequence. More practically, each of the signals lines Y is connected to the video line through the horizontal switch HSW, receives a supplying of the video signal VSIG from the signal driver 103 and in turn the H driver 102 outputs horizontal sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3}, ... ϕ_{HN} in sequence and controls ON or OFF of each of the horizontal switches HSW.

Fig. 9 expresses waveforms of sampling pulses. As the active matrix display device is made to be highly accurate in operation, the sampling rate is made fast and the sampling pulse width τ_H becomes disturbed. As the sampling pulse is outputted, its corresponding horizontal switch HSW is turned on or off and the video signal VSIG from the video line is sampling held in the corresponding signal line Y. Each of the signal lines Y has a capacitor component and its charging or discharging is produced by the sampling of the video signal VSIG. As a result, the potential in the video line is varied. As described above, as the sampling rate is made fast, the sampling pulse width τ_H is disturbed, so that a charging or discharging in respect to each of the signal lines Y is not made constant and the potential at the video line is oscillated. There

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occurs a problem that this state appears as a vertical fixed pattern and remarkably damages quality of the displayed video image. In the case of displaying in accordance with the normal NTSC Standards, the sampling rate is relatively low and shows a timing in which a next sampling pulse is raised after ending of the potential oscillation in the video line, so that a vertical fixed pattern does not appear due to no bad influence against the previous signal line. However, in the case of HDTV or a double-speed NTSC, the sampling rate is rapidly increased and an effective restriction of a potential oscillation in the video line is difficult to perform. The sampling pulse is in general generated by the H driver comprised of shift registers or the like constituted by TFTs. Since TFT has a lower mobility as compared with that of a monolithic silicon transistor and also has a higher disturbance in each of the physical constants, it is difficult to perform an accurate control over the sampling pulses generated by this circuit. In addition, a certain disturbance may occur in ON resistance of the horizontal switch HSW in addition to the disturbance of the sampling pulse width. With such an arrangement as above, there occurs a variation in charging or discharging characteristic in

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the signal line Y and the video line potential is oscillated, so that this is overlapped on the actual video signal VSIG, appears as a vertical line to make a remarkable damage in quality of displaying the video signal.

SUMMARY OF THE INVENTION

In view of the aforesaid technical problems found in the prior art, it is an object of the present invention to perform an effective restriction of a potential oscillation in the video line generated as the sampling rate is increased. In order to accomplish the aforesaid object, the present invention has provided the following means. That is, the active matrix display device of the present invention is provided with gate lines in row, signal lines in column and matrix pixels arranged at each of the crossing points of both lines as its basic configuration. In addition, there is also provided a vertical scanning circuit, wherein each of the gate lines is scanned in sequence in line and pixels in one line are selected for every one horizontal period. There is also provided a horizontal scanning circuit, wherein the video signals are sampled in sequence at each of the signal lines within one

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horizontal period, and performs writing of video signals by dot sequential scanning on the selected pixels in one line. As a feature of the present invention, there is provided a precharging means and the predetermined precharging signals are supplied in sequence to each of the signal lines prior to the sequential sampling of the video signal corresponding to each of the signal lines.

More practically, the aforesaid precharging means is comprised of a plurality of switching elements connected to each of the terminal ends of the respective signal lines and a control means for controlling in sequence ON or OFF of each of the switching elements and supplying a precharging signal to each of the signal lines. This control means is comprised of an additional horizontal scanning circuit separately installed from the horizontal scanning circuit, wherein each of the switching elements is controlled in sequence in its ON or OFF state. Alternatively, the control means may be constructed such that its output is distributed and each of the switching elements is controlled in sequence for its ON or OFF state.

The precharging means supplies a precharging signal having a grey level in respect to the video signal varying between the white level and the black

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level. Alternatively, the precharging means may be constructed to supply the precharging signal having the same polarity and the same waveform as those of the video signal.

The present invention includes a method for driving the active matrix display device. That is, the driving method in accordance with the present invention is characterized in that it performs a vertical scanning for scanning linearly in sequence of each of the gate lines and selecting pixels in one line for every one horizontal period, a horizontal scanning for sampling in sequence the video signals in one horizontal period to each of the signal lines and writing the video signals by dot sequential scanning to the pixels in one selected line, and a precharging for supplying in sequence a predetermined precharging signal to each of the signal lines prior to the sequential sampling of the video signals in respect to each of the signal lines.

According to the present invention, the charging or discharging of each of the signal lines is almost completed with the precharging signal, and the charging or discharging in case of performing the sampling of the video signals is carried out such that it may occur only at a difference between the

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precharging level and the signal level. Accordingly, the potential oscillation in the video line for supplying the video signals is restricted more as compared with that of the prior art and then the vertical fixed pattern becoming a problem in keeping video quality can be eliminated. In particular, in the present invention, the precharged signals are sampled by so-called dot sequential scanning to each of the signal lines. As compared with the case that the precharged signals are all sample held in all signal lines, the potential oscillation at the gate lines or power source line can be reduced. In addition, a less driving capability of the precharging means is also satisfactory.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram for showing the first preferred embodiment of the active matrix display device.

Fig. 2 is a timing chart applied for illustrating an operation in the first preferred embodiment.

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Fig. 3 is a circuit diagram for showing the second preferred embodiment of the active matrix display device of the present invention.

Fig. 4 is a timing chart applied for illustrating an operation of the second preferred embodiment.

Fig. 5 is a circuit diagram for showing an example of practical configuration of the second preferred embodiment.

Fig. 6 is a circuit diagram for showing another practical example of configuration of the second preferred embodiment.

Fig. 7 is a timing chart applied for illustrating an operation of the configuration shown in Fig. 6.

Fig. 8 is a circuit diagram for showing the configuration of the prior art active matrix display device.

Fig. 9 is a waveform view applied for illustrating the problem.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings, the preferred embodiments of the present invention will be described

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in detail. Fig. 1 is a circuit diagram for showing the first preferred embodiment of the active matrix display device of the present invention. The active matrix display device is comprised of gate lines X in row, signal lines Y in column and liquid crystal pixels LC in matrix arranged at each of the crossing points in both lines. In this preferred embodiment, there are provided pixels LC utilizing liquid crystal as electro-photo substance. However, the present invention is not limited to this embodiment, but other electro-optical substances may be utilized. There are provided thin film transistors Tr for use in driving each of the liquid crystal pixels LC. The source electrode of the thin film transistor Tr is connected to the corresponding signal line Y, the gate electrode is connected to the corresponding gate line X and the drain electrode is connected to the corresponding liquid crystal pixel LC.

There is provided a V driver 1 so as to constitute the vertical scanning circuit, and each of the gate lines X is scanned in line at a time and a liquid crystal pixel LC in one line is selected for every one horizontal period. More practically, the V driver 1 transfers the vertical start signal VST in

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sequence in synchronous with the vertical clock signal VCK and outputs the selection pulses ϕ_{V1}, ϕ_{V2}, ... ϕ_{VM} to each of the gate lines X. With such an arrangement as above, the thin film transistor Tr is controlled in its ON or OFF state.

In addition, there is provided a H driver 2 so as to constitute the horizontal scanning circuit in which the video signals VSIG are sampled in sequence to each of the signal lines in one horizontal period and the video signals VSIG are written by dot sequential scanning to the liquid crystals LC of selected one line. More practically, one end of each of the signal lines Y is provided with horizontal switching elements HSW1, HSW3, HSW4, ... HSWN, connected to each of the video lines 3 so as to receive the video signals VSIG. In turn, the H driver 2 transfers in sequence the horizontal start signal HST in synchronous with the predetermined horizontal clock signal HCK and outputs the sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3}, ϕ_{H4} ... ϕ_{HN}. These sampling pulses control ON or OFF of the corresponding horizontal switching elements and sample holds the video signals VSIG to each of the signal lines Y.

As a feature of the present invention, there is provided a precharging means 4, a predetermined

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precharging signal VPS is supplied in sequence to each of the signal lines Y prior to the sequential sampling of the video signal VSIG in respect to each of the signal lines Y and then a charging or a discharging of each of the signal lines Y through sampling is restricted. With such an arrangement as above, a less potential oscillation of the video line 3 occurs. More practically, the precharging means 4 has additional switching elements PSW1, PSW2, PSW3, PSW4, ... connected to the terminal end of each of the signal lines Y. In addition, there is provided a P driver 5 so as to constitute a control means for controlling in sequence ON or OFF of the additional switching elements PSW and supplying the precharging signal VPS to each of the signal lines Y. More practically, the P driver 5 has a similar configuration to that of the H driver 2, wherein the horizontal start signal PST is transferred in sequence in synchronous with the horizontal clock signal PCK, and then precharging sampling pulses ϕ_{P1}, ϕ_{P2}, ϕ_{P3}, ϕ_{P4}, ... ϕ_{PN} are outputted. The additional horizontal switching elements PSW are controlled in sequence for their ON or OFF state in response to these precharging sampling pulses. In the preferred embodiment, the control means is comprised of the horizontal scanning

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circuit having the additional P driver 5 separate from the H driver 2, wherein each of the switching elements PSW is controlled in its ON or OFF state in sequence. In addition, the horizontal scanning circuit such as the H driver 2 or the P driver 5 has as its basic configuration shift registers, wherein either the thin film transistors or monolithic silicon transistors are integrated. The switching element HSW for the video signal sampling or the switching element PSW for the precharging signal sampling can be constructed by NMOS, PMOS and CMOS. In the preferred embodiment, although the H driver 2 and the P driver 5 are separately arranged at both ends of the signal line Y, the H driver 2 and the P driver 5 may be integrated at the same side. In this case, the horizontal switches HSW and PSW are also arranged at one end of the signal line Y.

Then, referring to Fig. 2, operation of the active matrix display device shown in Fig. 1 will be described in detail. As described above, the P driver 5 transfers in sequence the start signal PST in synchronous with the horizontal clock signal PCK and outputs the precharging sampling pulses ϕ_{P1}, ϕ_{P2}, ϕ_{P3}, and ϕ_{P4}. Similarly, the H driver 2 also transfers the horizontal start signals HST in synchronous with the

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horizontal clock signal HCK and outputs the sampling pulses ϕ_{H1}, ϕ_{H2}, and ϕ_{H3}. In the preferred embodiment, as the signals HCK and PCK, the same horizontal clock signals are used. In turn, the horizontal start signal is operated such that its PST operates first and then its HST operates. With such an arrangement as above, the sampling pulse for the precharging signal is always preceded in advance only by 1 sampling timing as compared with the sampling for the video signal.

The video signal VSIG is supplied to the H driver 2 and a precharging signal VPS is supplied to the P driver 5. As shown in the timing chart of Fig. 2, the video signal VSIG has a waveform varying between a white level and a black level. In turn, the precharging signal VPS has a specified potential of a grey level. In light of this state, the precharging signal VPS having the same polarity and the same waveform as those of the video signal VSIG may be used. Applying the same waveform in VSIG and VPS reduces remarkably a charging or discharging amount at the signal line and the potential oscillation at the video line 3 can be effectively restricted. Provided in the case that the same waveform is used in VSIG and VPS, the signal is not branched from the common video driver, but it is

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necessary to prepare a respective separate signal source. In turn, in the case that the specified voltage waveform of grey level is used as the precharging signal, a slight charging or discharging is produced at the sampling time of the video signal, although the charging or discharging amount of the signal line can be remarkably reduced as compared with that of the case in which the video signal having an opposite polarity such as in the case of 1H reversing driving operation.

At the lowest stage of the timing chart shown in Fig. 2 are expressed variations of potentials VY1, VY2 and VY3 of each of the signal lines Y. Taking account of the initial signal line Y1 shows that ϕ_{P1} is outputted before ϕ_{H1} is outputted, so that the precharging level is sampled at first at the signal line Y1 and then the video signal level is sampled. This operation is performed in sequence to the second and subsequent signal lines to enable a high quality displaying having no vertical stripe to be attained. In the present invention, the charging or discharging to Y1, Y2, Y3....are almost finished with the precharging signal VPS and the charging or discharging with VSIG is produced only with a difference between the precharging level and the video signal level. At this time, the

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precharging signal VPS is sampled by so-called dot sequential scanning to each of the signal lines Y. Merits of this system consist in the fact that the precharging signal VPS is sample held at all signal lines, resulting in that the gate line X and the power source line are not oscillated. Since the load capacity as viewed from the line of the precharging signal VPS is reduced, so that a resistance in the precharging signal line, a size of the added switching element PSW and a driving capability of the P driver and the like can be reduced.

In the preferred embodiment, although the vertical scanning circuit is constructed to output selection pulses to gate lines in such a manner that each of the gate lines is scanned in sequence in a linear way and some pixels in one line are selected for every horizontal period, it may also be applicable that the pixels in more than two lines are concurrently selected.

Fig. 3 is a circuit diagram for showing the second preferred embodiment of the active matrix display device of the present invention. Basically,the second preferred embodiment has the similar configuration to that of the first preferred embodiment shown in Fig. 1,

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wherein the corresponding reference numerals are added to the corresponding portions and their understanding is facilitated. In the preferred embodiment, one end of each of the signal lines Y is provided with the sampling switching element HSW for the video signal VSIG and the sampling switching element PSW for the precharging signal VPS. These switching elements HSW and PSW are commonly controlled by the H driver 2 for their ON or OFF state. That is, the preferred embodiment is different from the previous preferred embodiment, wherein the P driver used in the sampling hold of the precharging signal VPS is eliminated and its configuration is made more simple. A sampling pulse D outputted from each of the stages of the H driver 2 is applied for use in controlling ON or OFF of HSW corresponding to each of the stages and concurrently it performs a control over ON or OFF of the PSW belonging to the next stage. In other words, the control means is assembled in the horizontal scanning circuit, its sampling pulse output is properly distributed to control in sequence ON or OFF of each of the switching elements HSW, PSW.

Referring now to the timing chart shown in Fig. 4, operation of the second preferred embodiment

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shown in Fig. 3 will be described in detail. At first, as the H driver 2 outputs the first sampling pulse D1, PSW1 is controlled for its ON or OFF state. Subsequently, as the second sampling pulse D2 is outputted, HSW1 and PSW2 are concurrently controlled for their ON or OFF state. As apparent from these facts, taking account into the first signal line Y1 causes PSW1 to be driven for its ON or OFF state, thereafter HSW1 is driven for its ON or OFF state. In addition, as the third sampling pulse D3 is outputted, HSW2 and PSW3 are concurrently driven for their ON or OFF state. Lastly, as DN is outputted, HSWN-1 and PSWN are concurrently driven for their ON or OFF state. The video signal VSIG supplied from the video line 3 and the precharging signal VPS supplied from the precharging line 6 are sampling held at each of the signal lines Y in response to the driving for ON or OFF state of these switching elements HSW and PSW. For example, taking into account the potential VY1 appeared at the first signal line causes VPS to be sampling held during a precharging period of making PSW1 to be ON and subsequently VSIG is sampled for a video writing period in which HSW1 becomes ON. In addition, taking into account the potential VY2 appearing the second signal line causes the precharging

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level to be written at a timing of making PSW2 ON and then the video signal level is written at a timing in which HSW2 subsequently becomes ON.

As described above, in the preferred embodiment, the charging or discharging for the signal line Y is almost completed through the precharging line 6, the charging or discharging through the video line 3 merely corresponds to a difference between the precharging level (VPS) and the video signal level (VSIG), resulting in that the potential oscillation of the video line 3 can be reduced and the vertical fixed pattern can be improved. In the preferred embodiment above, although the sampling pulse for driving PSW is taken out from the stage before the H driver 2, the present invention is not limited to its operation. As long as the time band is of one in which a polarity of the video signal is not changed, it is satisfactory that the sampling pulse can be taken from any stages before the H driver 2. In the preferred embodiment as above, since the precharging is carried out by dot sequential scanning for each of the signal lines, no sub-action for the video quality caused by writing of the precharging signal VPS at once is found. For example, as the precharging signals are all sampling held for all signal

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lines at once, a potential at the gate signal is oscillated due to a capacitance coupling, resulting in that a leak of the video signals written into the liquid crystal pixels may occur to cause a shading or a lateral stripe to be generated. In the worst case, a lack of bright point may occur in the case of normal white mode due to a leakage of electrical load written into it. Not only potential oscillation at the gate lines can be restricted, but also no oscillation occurs at the power source line or the earth line and an operating margin is expanded. In addition, since the capacity as viewed from the precharging line 6 is less in its value, a design margin can be expanded. With such an arrangement as above, a high quality video can be obtained and a driving margin can be expanded.

Fig. 5 is a circuit diagram for illustrating a practical example of the second preferred embodiment shown in Fig. 3. As shown in this figure, HSW and PSW are constructed as transmission gates in the preferred embodiment. In addition, the H driver 2 is comprised of the H shift register 7 and the output gate 8 connected to each of the stages. The output gate 8 forms the sampling pulse and its reversing pulse in response to the output of the H shift register 7 so as to drive for

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ON or OFF of each of HSW and PSW. As described above, the sampling pulse applied to PSW is supplied from one stage before the H shift register 7, so that the point sequential sampling hold of the precharging signal VPS is carried out prior to the point sequential sampling of the video signal VSG.

Fig. 6 shows a modified form of the preferred embodiment shown in Fig. 5, wherein some corresponding reference numerals are applied to the corresponding portions so as to facilitate its understanding. The basic configuration is similar to that of the preferred embodiment shown in Fig. 5. The different points are that the sampling pulse to be applied to PSW is not one before the stage, but supplied from the H shift register 7 of two stages before. In general, if there is a time in which polarities of VSIG and VPS are not reversed, the sampling pulse applied to PSW may be taken before any stages of the H shift register.

Lastly, referring now to Fig. 7, operation of the preferred embodiment shown in Fig. 6 will be described in detail. As described above, the sampling pulses D1, D2, D3, D4, ... DN are outputted in sequence from the H register 7 through the output gate 8. When D1 is outputted, PSW1 is turned ON. Then, when D2 is

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outputted, PSW2 is turned ON. Subsequently, when D3 is outputted, PSW3 and HSW1 are turned ON. In addition, when D4 is outputted, PSW4 and HSW2 are turned ON. Lastly, when DN is outputted, PSWN and HSWN-2 are turned ON. In turn, VSIG has a waveform in which the signal level is changed in response to a video signal. In the preferred embodiment above, since 1H reversing driving is carried out, so that its polarity is reversed for every 1H. In compliance with this operation, VPS having a predetermined precharging level is also reversed for every 1H.

Taking into account the potential VY1 appearing at the first signal line shows that a precharging level is written for a precharging period in which D1 is outputted and PSW1 is turned ON. Subsequently, after elapsing 1 sampling timing, the signal level is sampling held during a period of writing actual video signal in which HSW1 is turned ON in response to the output of D3. In this case, a charging or a discharging amount of the first signal line becomes a difference between the precharging level and the signal level and it can be restricted low. In particular, the aforesaid difference is almost eliminated in the case that the same waveform as that of

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the video signal VSIG is used as the precharging signal PS. Then, taking into account the potential VY2 appearing at the second signal line shows that the precharging level is written during a precharging period in which PSW2 is turned ON in response to D2, and the signal level is sampling held during an actual video signal writing period in which HSW2 is turned ON in response to D4 in 1 sampling timing. The potential VY3 appearing at the third signal line is also similarly processed.

As described above, according to the present invention, predetermined precharging signals are supplied in sequence prior to the sequential sampling of the video signals for each of the signal lines so as to restrict the charging or discharging of each of the signal lines through the sampling. With such an arrangement as above, since the potential oscillation in the video line (noise) is substantially reduced, it has an effect that the vertical fixed pattern can be removed from the displayed image. Since the precharging is carried out by dot sequential scanning, the shooting or lateral stripe pattern can be restricted and similarly the image quality can be improved. Due to similar reasons, it has effects that an operating margin can be

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expanded and potential oscillation at the power source line or the earth line is not found. Since the vertical fixed pattern can be removed by the pre-charging, it has some effects that it is not necessary to consider the problem of minute disturbance of the sampling pulse width and that a design margin of the horizontal scanning circuit is expanded. Due to the similar reason, it has another effect that the power source voltage can be reduced and the consumption power can be saved.

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* C L M S *

What Is Claimed Is:

1. An active matrix display device comprising:

a plurality of gate lines arranged in row;

a plurality of signal lines arranged in column;

pixels arranged at each of crossing points of said gate lines and signal lines;

a vertical scanning circuit for scanning each of the gate lines in sequence and selecting pixels of at least one line;

a horizontal scanning circuit for sampling video signals in sequence and writing the video signals in sequence in the pixels in selected line; and

a precharging circuit for supplying precharging signals in sequence to each of the signal lines prior to a sequential sampling of video signals to each of the signal lines.

2. An active matrix display device according to claim 1 in which said precharging circuit is comprised of switching elements connected to an end part of each of the signal lines, and a control circuit for controlling the switching elements and supplying a precharging signal to each of the signal lines.

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3. An active matrix display device according to claim 2 in which said control circuit is an additional horizontal scanning circuit arranged independently from said horizontal scanning circuit.

4. An active matrix display device according to claim 2 in which said control circuit is assembled in said horizontal scanning circuit, distributes its output and controls each of the switching elements in sequence for its ON or OFF state.

5. An active matrix display device according to claim 1 in which said precharging circuit supplies a precharging signal having a grey level in respect to a video signal varying between a white level and a black level.

6. An active matrix display device according to claim 1 in which said precharging circuit supplies a precharging signal having the same polarity as that of the video signal.

7. An active matrix display device according to claim 1 in which said precharging circuit is arranged in opposition to said horizontal scanning circuit.

8. An active matrix display device according to claim 1 in which said precharging circuit is arranged

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* C L M S *

at the same side as that of said horizontal scanning circuit.

9. A method for driving an active matrix device comprising gate lines arranged in row, a plurality of signal lines arranged in column, and pixels arranged at the crossing parts between said gate lines and signal lines, comprising the following steps of:

line scanning in sequence of each of the gate lines and selecting pixels for at least one row;

sampling in sequence the video signals and writing the video signals by dot sequential scanning to the pixels in one selected row; and

providing a precharging signal to each of the signal lines prior to a sequential sampling of the video signal for each of the signal lines.

10. A method for driving an active matrix device according to claim 7 in which said precharging signal is a signal having the same polarity as that of the video signal and having a grey level.

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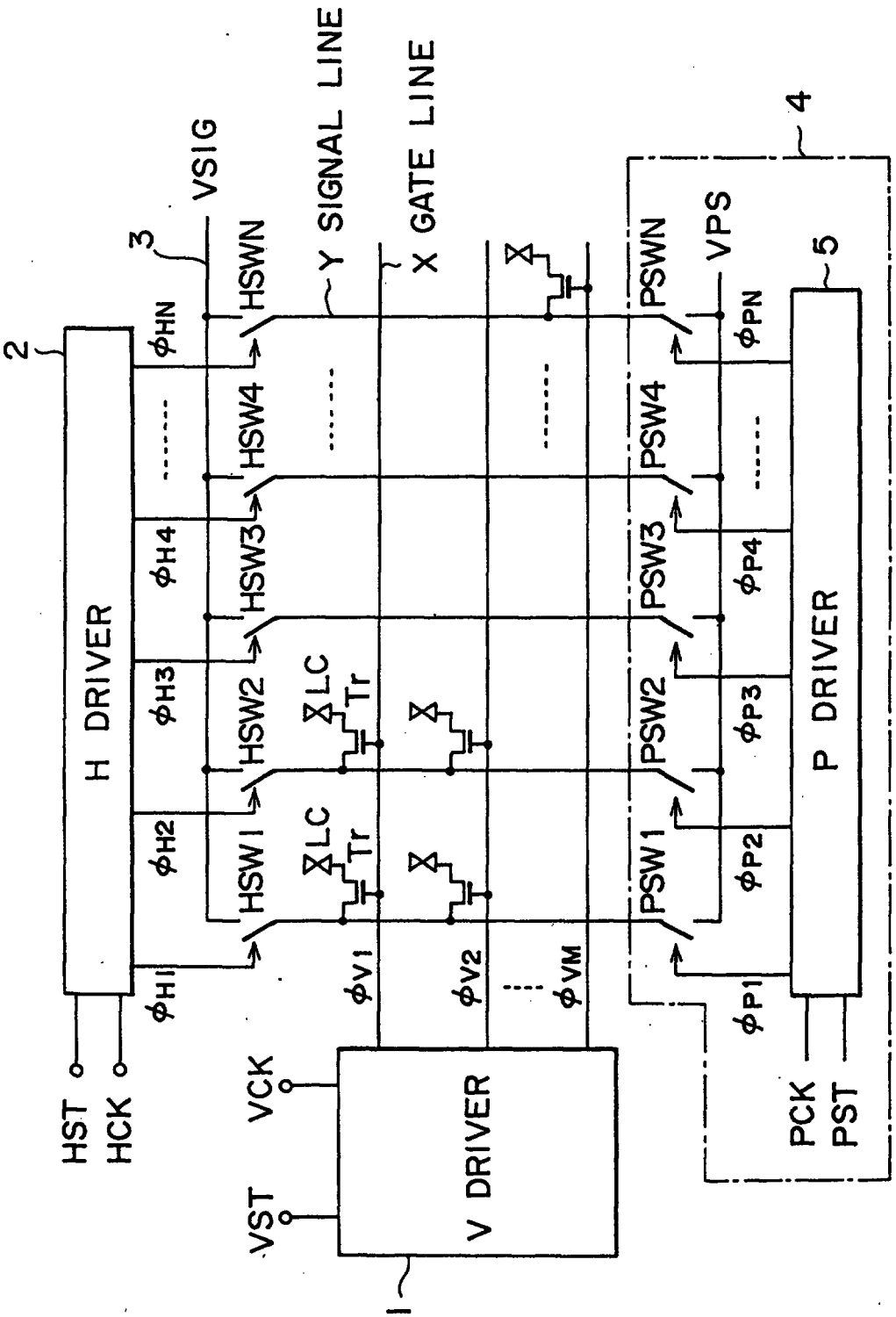
ACTIVE MATRIX DISPLAY DEVICE AND ITS DRIVING METHOD

Abstract of the Disclosure

To restrict a potential oscillation in a video line caused by a high speed sampling rate, precharging means supplies in sequence the predetermined precharging signal VPS prior to the sequential sampling of the video signal VSIG for each of the signal lines Y. This precharging means is comprised of a plurality of switching elements PSW connected to an end part of each of the signal lines Y, and of the P driver for supplying the precharge signal VPS to each of the signal lines Y through sequential controlling of ON or OFF of each of the switching elements PSW.

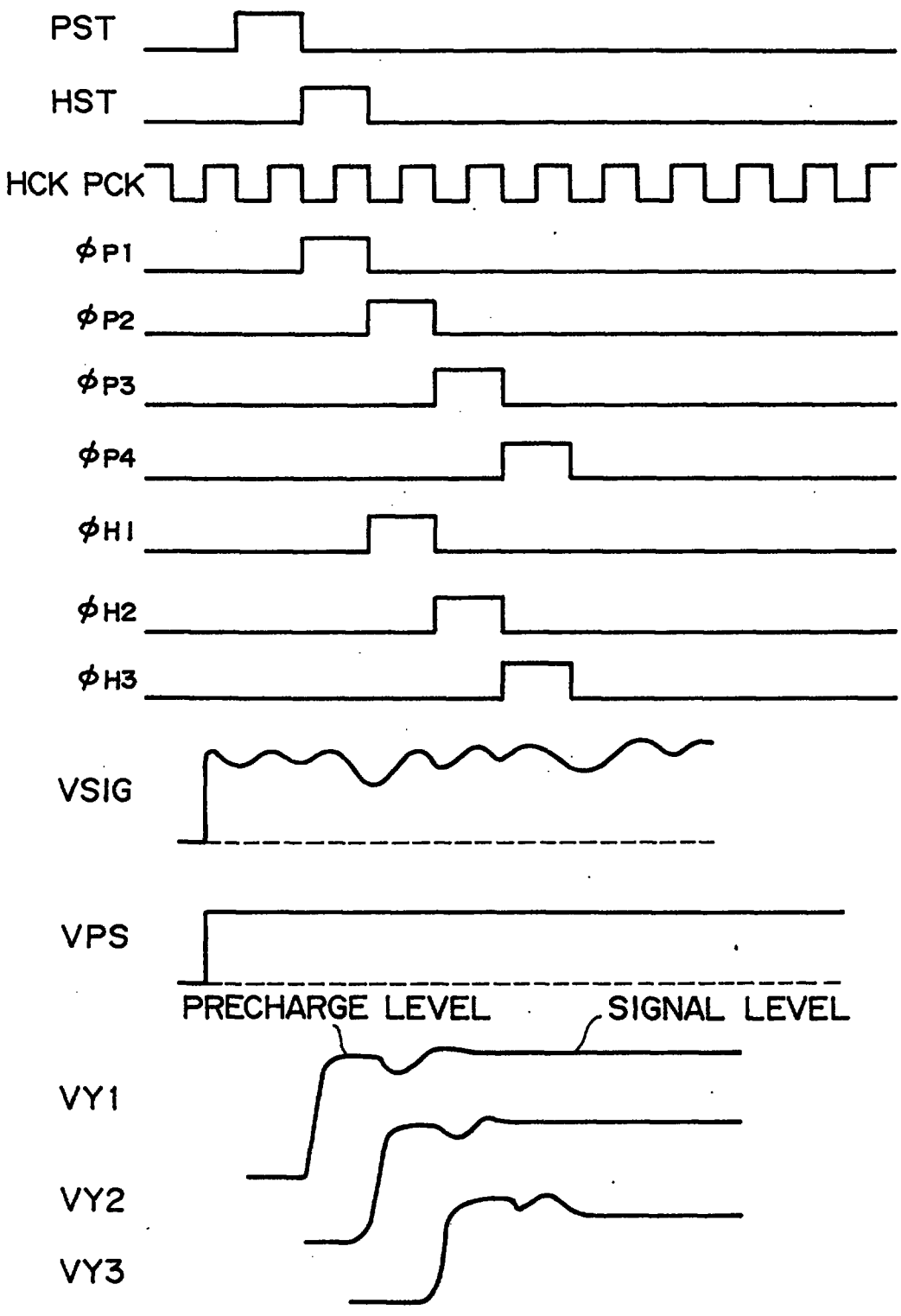
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FIG. 1



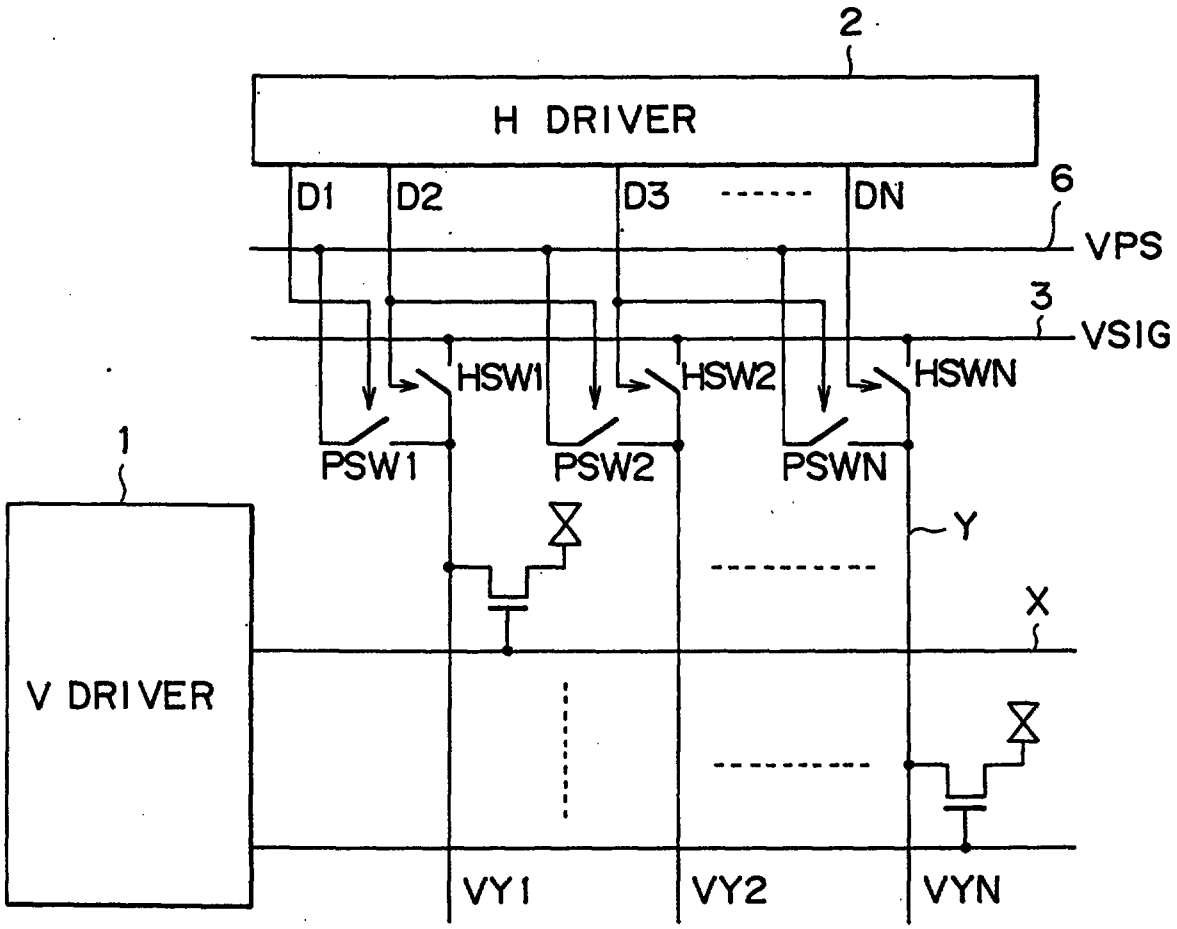
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FIG. 2



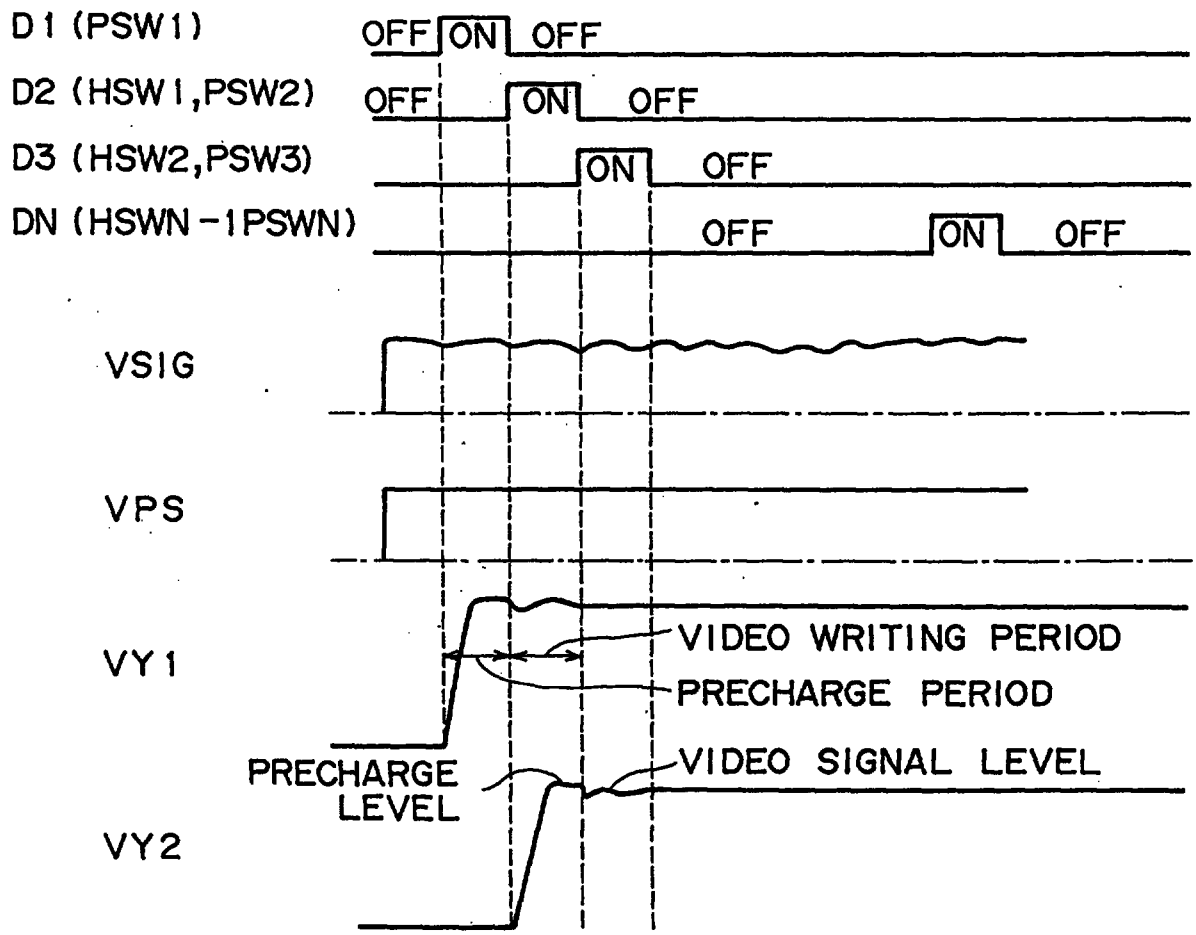
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FIG. 3



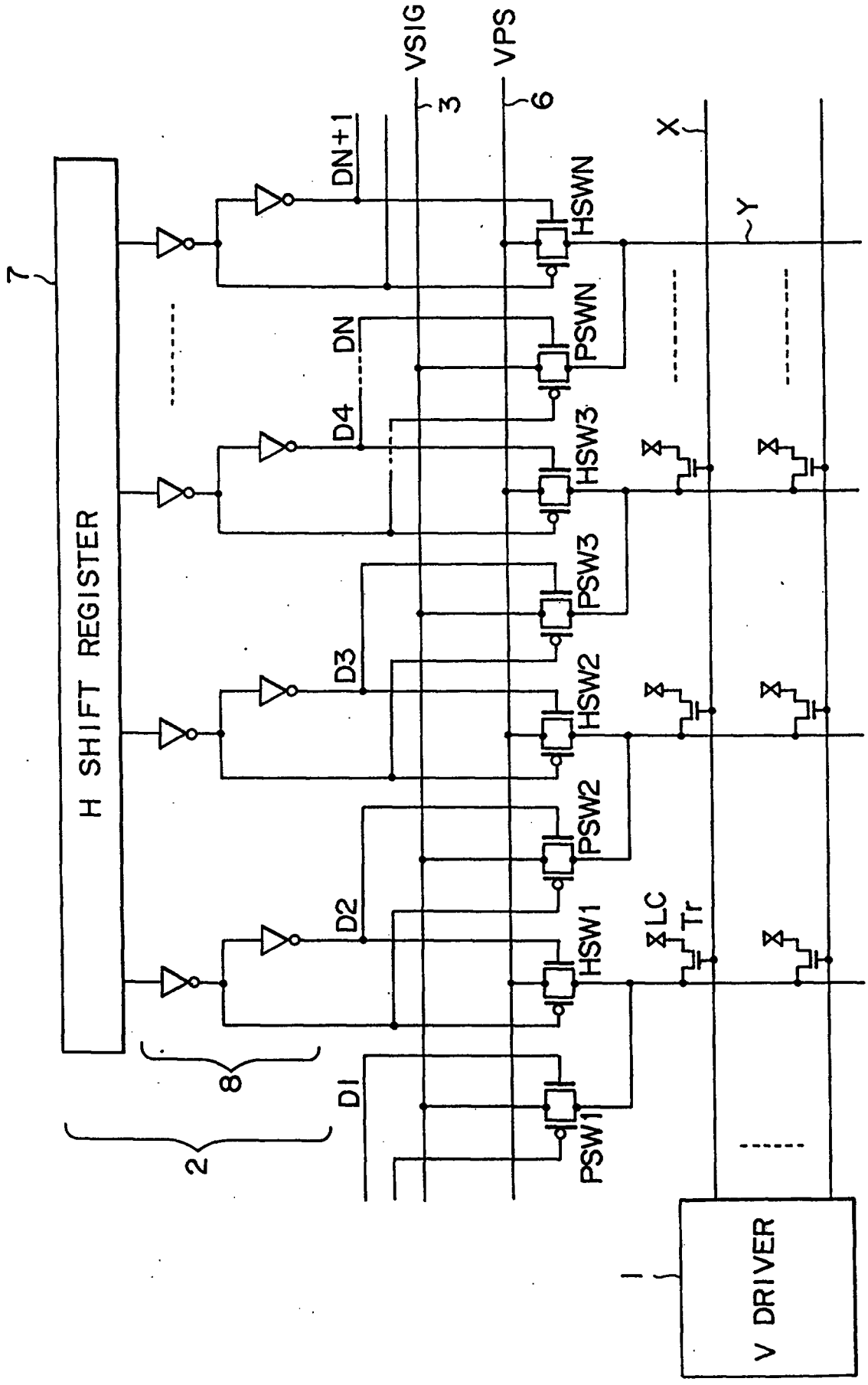
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FIG. 4



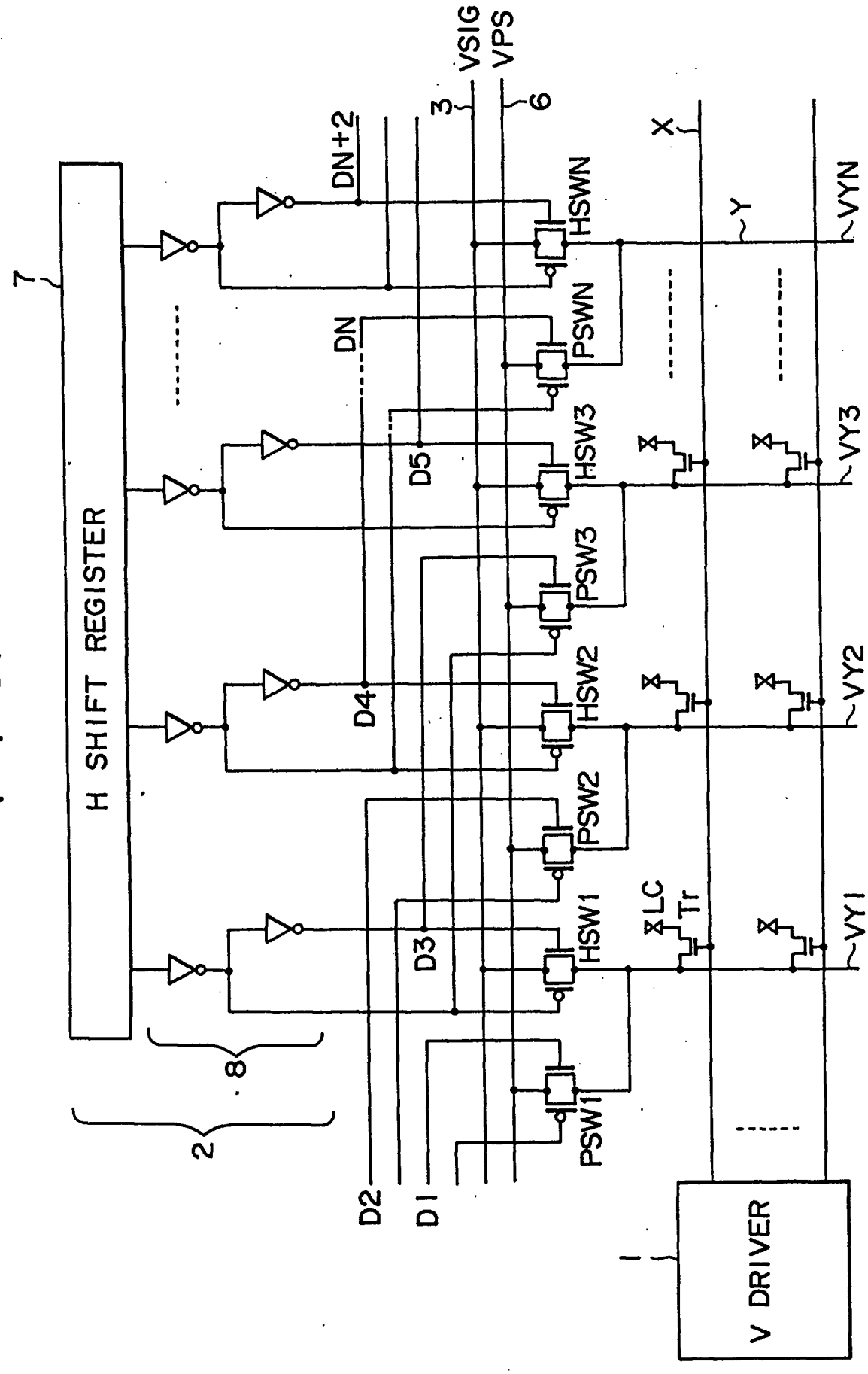
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FIG. 5



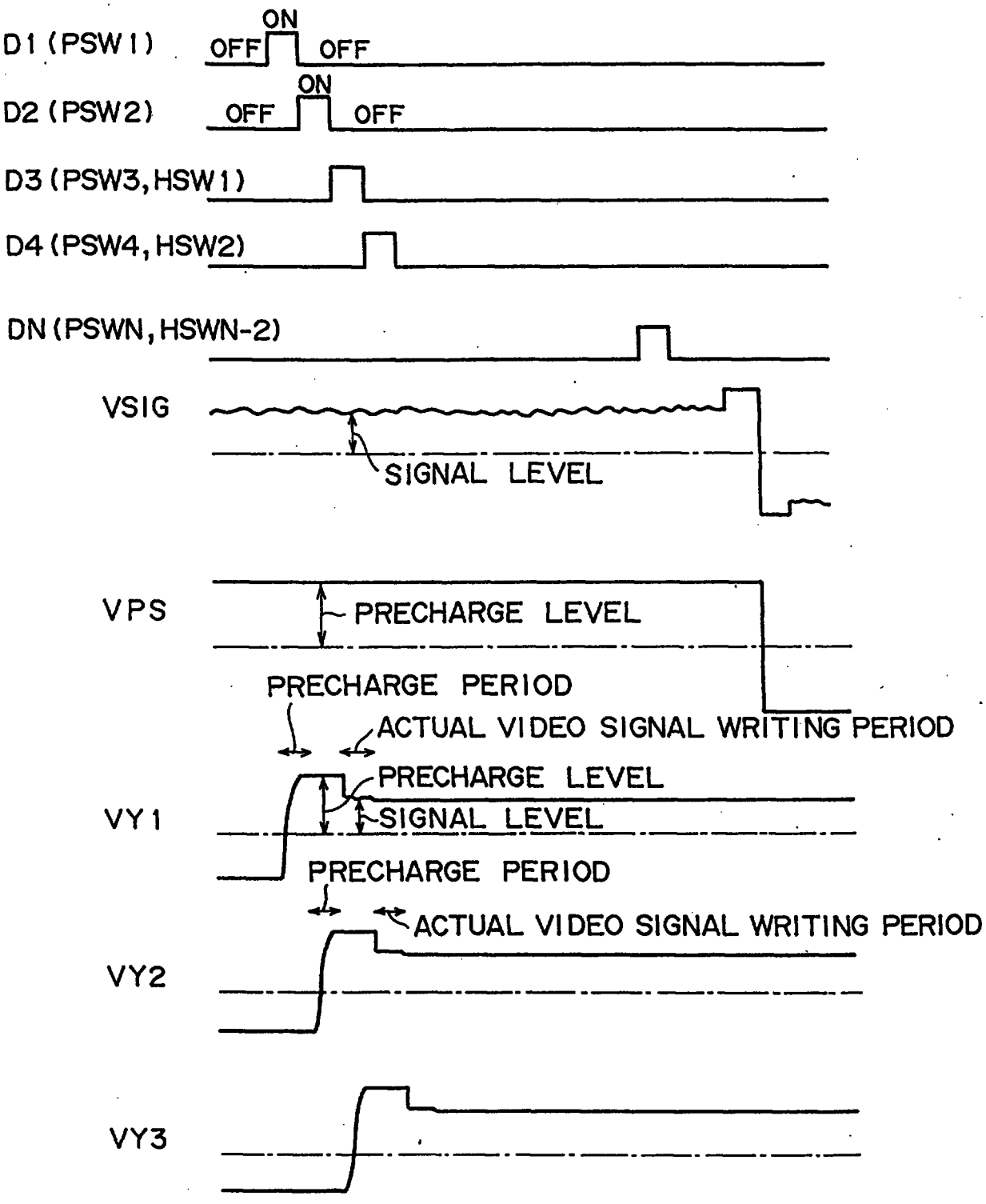
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Date : 8 NOV 1995

FIG. 6



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Date : 8 NOV 1995

FIG. 7



REPLACEMENT SHEET
8 NOV 1995
Date :.....

FIG. 8

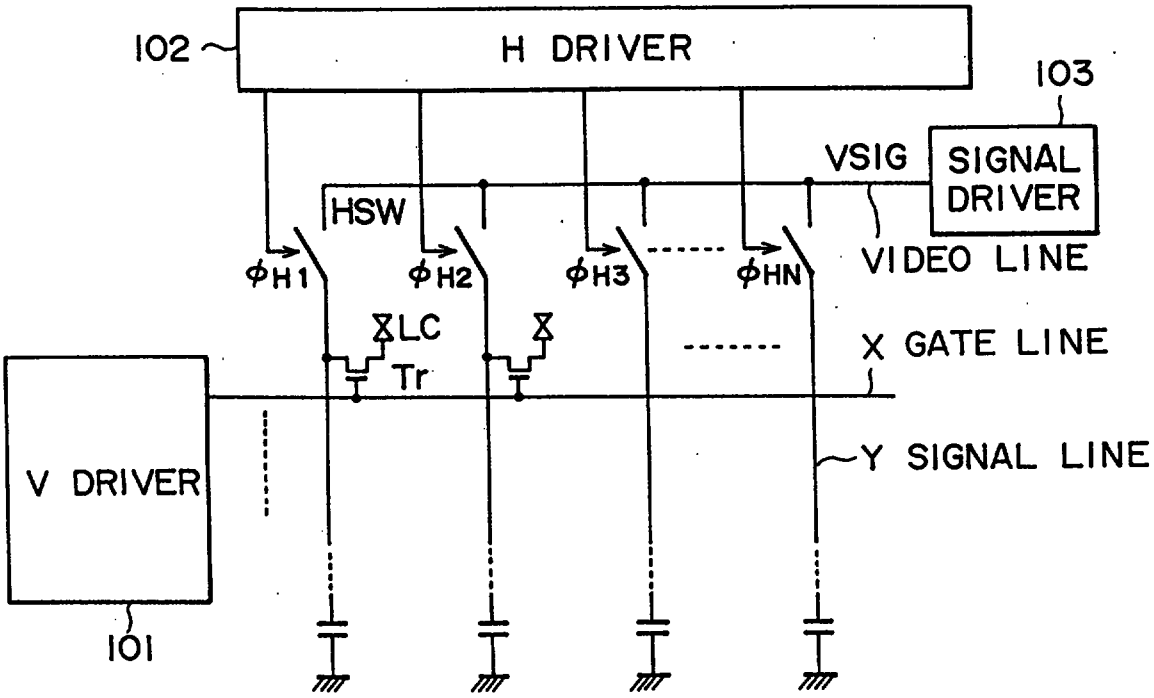


FIG. 9

