What is claimed is:

1. A method of operating a ferroelectric memory cell, the method comprising:

applying one of a positive bias voltage or a negative bias voltage to a ferroelectric memory cell comprising a ferroelectric capacitor; and

applying another of the positive bias voltage or the negative bias voltage to the ferroelectric memory cell to switch a polarization of the ferroelectric memory cell, the negative bias voltage having a different magnitude than the positive bias voltage.

2. The method of claim **1**, wherein applying one of a positive bias voltage or a negative bias voltage comprises applying one of the positive bias voltage or the negative bias voltage having an absolute value between about twenty-five percent and about ninety-nine percent of an absolute value of the other of the positive bias voltage or the negative bias voltage.

3. The method of claim **1**, wherein applying one of a positive bias voltage or a negative bias voltage comprises applying one of the positive bias voltage or the negative bias voltage having an absolute value between about sixty percent and about seventy-five percent of an absolute value of the other of the positive bias voltage or the negative bias voltage.

4. The method of claim **1**, wherein applying one of a positive bias voltage or a negative bias voltage to a ferroelectric memory cell comprises applying the one of the positive voltage or the negative voltage to the ferroelectric capacitor, the ferroelectric capacitor comprising an interfacial material between one of a first electrode or a second electrode and directly on and contacting one of the first electrode or the second electrode.

5. The method of claim **1**, wherein applying one of a positive bias voltage or a negative bias voltage to a ferroelectric memory cell comprises applying one of the positive bias voltage or the negative bias voltage to the ferroelectric capacitor, the ferroelectric capacitor comprising an interfacial material comprising titanium oxide or aluminum nitride.

6. The method of claim **1**, wherein applying one of a positive bias voltage or a negative bias voltage to a ferroelectric memory cell comprises applying one of the positive bias voltage or the negative bias voltage to the ferroelectric capacitor, the ferroelectric capacitor comprising a top electrode having a different thickness than a bottom electrode thereof.

7. The method of claim **1**, wherein applying one of a positive bias voltage or a negative bias voltage to a ferroelectric memory cell comprises applying one of the positive bias voltage or the negative bias voltage to the ferroelectric capacitor, the ferroelectric capacitor comprising at least one electrode comprising titanium aluminum nitride.

8. The method of claim **1**, wherein applying one of a positive bias voltage or a negative bias voltage to a ferroelectric memory cell comprises applying one of the positive bias voltage or the negative bias voltage to the ferroelectric capacitor, the ferroelectric capacitor comprising at least one of hafnium oxide or zirconium oxide between a top electrode and a bottom electrode.

9. The method of claim **1**, wherein applying one of a positive bias voltage or a negative bias voltage to a ferroelectric memory cell comprises applying one of the positive bias voltage or the negative bias voltage to the ferroelectric capacitor, the ferroelectric capacitor having a positive remnant polarization that is different from a negative remnant polarization.

10. The method of claim **1**, further comprising altering at least one of the positive bias voltage or the negative bias voltage after a predetermined number of cycles.

11. A ferroelectric memory cell, comprising:

a capacitor, the capacitor comprising:

a first electrode comprising titanium aluminum nitride;

a second electrode comprising titanium nitride, titanium aluminum nitride, or tantalum nitride; and

a ferroelectric material comprising hafnium oxide, zirconium oxide, or a combination thereof between the first electrode and the second electrode.

12. The ferroelectric memory cell of claim **11**, further comprising an interfacial material between the first electrode and the second electrode.

13. The ferroelectric memory cell of claim **12**, wherein the interfacial material comprises titanium oxide or aluminum nitride.

14. The ferroelectric memory cell of claim **11**, wherein the ferroelectric material further comprises a dopant comprising silicon, aluminum, zirconium, magnesium, strontium, gadolinium, yttrium, or combinations thereof.

15. The ferroelectric memory cell of claim **11**, wherein the second electrode comprises titanium nitride.

16. A capacitor comprising:

a first electrode comprising titanium nitride;

a ferroelectric material comprising hafnium oxide, zirconium oxide, or a combination thereof;

a second electrode over the ferroelectric material; and

an interfacial material comprising aluminum nitride or titanium oxide between the first electrode and the second electrode.

17. The capacitor of claim **16**, wherein the second electrode comprises titanium nitride.

18. The capacitor of claim **16**, wherein the second electrode comprises titanium aluminum nitride.

19. The capacitor of claim **16**, wherein the ferroelectric material comprises hafnium oxide and directly overlies and contacts the interfacial material.

20. The capacitor of claim **16**, wherein the interfacial material directly overlies and contacts the first electrode.