What is claimed is:

1. A method of forming a memory cell, comprising:

forming a resistance variable memory cell material on a first electrode and a wall of a via;

forming a first dielectric material on the resistance variable memory cell material;

removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed; and

forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material.

2. The method of claim 1, wherein the method includes forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material.

3. The method of claim 2, wherein the method includes removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the resistance variable memory cell material formed on the first electrode to form a first and a second resistance variable memory cell structure.

4. The method of claim 3, wherein forming the first and the second resistance variable memory cell structures includes forming a first arcuate resistance variable region corresponding to the first resistance variable memory cell structure and a second arcuate resistance variable region corresponding to the second resistance variable memory cell structure.

5. The method of any one of claims 1-4, including forming the resistance variable memory cell material such that it has a thickness of no greater than 5 nanometers.

6. The method of any one of claims 1-4, wherein forming the resistance variable memory cell material includes depositing the resistance variable memory cell material using atomic layer deposition.

7. The method of any one of claims 1-4, wherein forming the resistance variable memory cell material includes depositing the resistance variable memory cell material using chemical vapor deposition.

8. The method of any one of claims 1-4, including forming the first electrode of a material that is different than at least one of the second and the third electrode.

9. The method of any one of claims 1-4, including forming the via through a second dielectric material to the first electrode prior to forming the resistance variable memory cell material on the first electrode and the wall of the via.

10. The method of claim 9, wherein removing the portion of the first dielectric material includes planarizing an upper surface of the semiconductor structure down to the second dielectric material.

11. The method of any one of claims 1-4, including forming the second electrode and the third electrode such that a portion of each overlaps the first dielectric material formed in the via.

12. A method of forming a memory cell, comprising:

forming a memory cell structure having a via formed over a first electrode;

forming a phase change material on the first electrode and on the walls of the via such that a gap remains between the walls of the via;

forming a first dielectric material on the phase change material;

removing a portion of the first dielectric material such that a portion of the phase change material is exposed and such that the first dielectric material remains only in the gap;

forming a second electrode on a first exposed portion of the phase change material and third electrode on a second exposed portion of the phase change material;

forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material located in the gap; and

removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the phase change material formed on the first electrode such that a first and a second phase change memory cell structure is formed.

13. The method of claim 12, wherein removing the at least a portion of the spacer material between the second and third electrodes, the at least a portion of the first dielectric material within the via, and the at least a portion of the phase change material forms an arcuate phase change region corresponding to the first phase change memory cell structure and an arcuate phase change region corresponding to the second phase change memory cell structure, with the first electrode being common to the first and the second phase change memory cell structures.

14. The method of claim 12, wherein forming the first dielectric material includes depositing a low temperature oxide material.

15. The method of any one of claims 12-14, including forming the second and third electrodes such that they overlap the dielectric material located in the gap.

16. The method of any one of claims 12-14, including performing a dry etch to remove the at least a portion of the spacer material between the second and third electrodes, the at least a portion of the first dielectric material within the via, and the at least a portion of the phase change material formed on the first electrode.

17. A resistance variable memory cell structure, comprising:

a first electrode common to a first and a second resistance variable memory cell;

a first vertically oriented resistance variable material having an arcuate top surface in contact with a second electrode and a non-arcuate bottom surface in contact with the first electrode; and

a second vertically oriented resistance variable material having an arcuate top surface in contact with a third electrode and a non-arcuate bottom surface in contact with the first electrode.

18. The resistance variable memory cell structure of claim 17, wherein an arcuate portion of the first and the second vertically oriented resistance variable material is located between a first dielectric material and a second dielectric material.

19. The resistance variable memory cell structure of claim 18, wherein the arcuate portion of the first vertically oriented resistance variable material is located a distance of not more than 20 nanometers from the arcuate portion of the second vertically oriented resistance variable material.

20. The resistance variable memory cell structure of claim 18, wherein the second electrode overlaps a portion of the first and the second dielectric material.

21. The resistance variable memory cell structure of claim 18, wherein a spacer material is formed on the first dielectric material and on an edge of the second electrode and an edge of the third electrode.

22. The resistance variable memory cell structure of any one of claims 17-21, wherein the first electrode is made of a material different than at least one of the second and the third electrodes.

23. The resistance variable memory cell structure of any one of claims 17-21, wherein the resistance variable material has a thickness of not greater than 5 nanometers.

24. The resistance variable memory cell structure of claim 17, wherein the second electrode is the top electrode of a first phase change memory cell, the third electrode is the top electrode of a second phase change memory cell, and the first electrode is a bottom electrode common to the first and second phase change memory cells.

25. The resistance variable memory cell structure of any one of claims 17-21, wherein the arcuate top surface of the first and the second vertically oriented resistance variable material is a planarized surface.

26. The resistance variable memory cell structure of any one of claims 17-21, wherein the first electrode is formed on a conductive contact.

27. An array of resistance variable memory cells having at least a first and a second resistance variable memory cell structure formed according to a method, comprising:

forming a memory cell structure having a via formed over a first electrode;

forming a resistance variable memory cell material on the first electrode and a wall of the via;

forming a first dielectric material on the resistance variable memory cell material;

removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed;

forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material;

forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material; and

forming the first and the second resistance variable memory cell structure by removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the resistance variable memory cell material formed on the first electrode.

What is claimed is:

1. A method of forming a memory cell, comprising:

forming a resistance variable memory cell material on a first electrode and a wall of a via;

forming a first dielectric material on the resistance variable memory cell material;

removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed;

forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material; and

forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material.

2. The method of claim 1, wherein the method includes removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the resistance variable memory cell material formed on the first electrode to form a first and a second resistance variable memory cell structure.

3. The method of claim 3, wherein forming the first and the second resistance variable memory cell structures includes forming a first arcuate resistance variable region corresponding to the first resistance variable memory cell structure and a second arcuate resistance variable region corresponding to the second resistance variable memory cell structure.

4. The method of claim 1, including forming the resistance variable memory cell material such that it has a thickness of no greater than 5 nanometers.

5. The method of claim 1, wherein forming the resistance variable memory cell material includes depositing the resistance variable memory cell material using atomic layer deposition.

6. The method of claim 1, wherein forming the resistance variable memory cell material includes depositing the resistance variable memory cell material using chemical vapor deposition.

7. The method of claim 1, including forming the first electrode of a material that is different than at least one of the second and the third electrode.

8. The method of claim 1, including forming the via through a second dielectric material to the first electrode prior to forming the resistance variable memory cell material on the first electrode and the wall of the via.

9. The method of claim 8, wherein removing the portion of the first dielectric material includes planarizing an upper surface of the semiconductor structure down to the second dielectric material.

10. The method of claim 1, including forming the second electrode and the third electrode such that a portion of each overlaps the first dielectric material formed in the via.

11. A method of forming a memory cell, comprising:

forming a memory cell structure having a via formed over a first electrode;

forming a phase change material on the first electrode and on the walls of the via such that a gap remains between the walls of the via;

forming a first dielectric material on the phase change material;

removing a portion of the first dielectric material such that a portion of the phase change material is exposed and such that the first dielectric material remains only in the gap;

forming a second electrode on a first exposed portion of the phase change material and third electrode on a second exposed portion of the phase change material;

forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material located in the gap; and

removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the phase change material formed on the first electrode such that a first and a second phase change memory cell structure is formed.

12. The method of claim 11, wherein removing the at least a portion of the spacer material between the second and third electrodes, the at least a portion of the first dielectric material within the via, and the at least a portion of the phase change material forms an arcuate phase change region corresponding to the first phase change memory cell structure and an arcuate phase change region corresponding to the second phase change memory cell structure, with the first electrode being common to the first and the second phase change memory cell structures.

13. The method of claim 11, wherein forming the first dielectric material includes depositing a low temperature oxide material.

14. The method of claim 11, including forming the second and third electrodes such that they overlap the dielectric material located in the gap.

15. The method of claim 11, including performing a dry etch to remove the at least a portion of the spacer material between the second and third electrodes, the at least a portion of the first dielectric material within the via, and the at least a portion of the phase change material formed on the first electrode.

16. A resistance variable memory cell structure, comprising:

a first electrode common to a first and a second resistance variable memory cell;

a first vertically oriented resistance variable material having an arcuate top surface in contact with a second electrode and a non-arcuate bottom surface in contact with the first electrode; and

a second vertically oriented resistance variable material having an arcuate top surface in contact with a third electrode and a non-arcuate bottom surface in contact with the first electrode;

wherein the first electrode is made of a material different than at least one of the second and the third electrodes.

17. The resistance variable memory cell structure of claim 16, wherein an arcuate portion of the first and the second vertically oriented resistance variable material is located between a first dielectric material and a second dielectric material.

18. The resistance variable memory cell structure of claim 17, wherein the arcuate portion of the first vertically oriented resistance variable material is located a distance of not more than 20 nanometers from the arcuate portion of the second vertically oriented resistance variable material.

19. The resistance variable memory cell structure of claim 17, wherein the second electrode overlaps a portion of the first and the second dielectric material.

20. The resistance variable memory cell structure of claim 17, wherein a spacer material is formed on the first dielectric material and on an edge of the second electrode and an edge of the third electrode.

21. The resistance variable memory cell structure of claim 16, wherein the resistance variable material has a thickness of not greater than 5 nanometers.

22. The resistance variable memory cell structure of claim 16, wherein the second electrode is the top electrode of a first phase change memory cell, the third electrode is the top electrode of a second phase change memory cell, and the first electrode is a bottom electrode common to the first and second phase change memory cells.

23. The resistance variable memory cell structure of claim 16, wherein the arcuate top surface of the first and the second vertically oriented resistance variable material is a planarized surface.

24. The resistance variable memory cell structure of claim 16, wherein the first electrode is formed on a conductive contact.

25. An array of resistance variable memory cells having at least a first and a second resistance variable memory cell structure formed according to a method, comprising:

forming a memory cell structure having a via formed over a first electrode;

forming a resistance variable memory cell material on the first electrode and a wall of the via;

forming a first dielectric material on the resistance variable memory cell material;

removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed;

forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material;

forming a spacer material on at least a portion of the second electrode, the third electrode, and the first dielectric material; and

forming the first and the second resistance variable memory cell structure by removing at least a portion of the spacer material between the second and third electrodes, at least a portion of the first dielectric material within the via, and at least a portion of the resistance variable memory cell material formed on the first electrode.

26. A method of forming a memory cell, comprising:

forming a resistance variable memory cell material on a first electrode and a wall of a via such that the resistance variable memory cell material has a thickness of no greater than 5 nanometers;

forming a first dielectric material on the resistance variable memory cell material;

removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed; and

forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material.

27. A method of forming a memory cell, comprising:

forming a resistance variable memory cell material on a first electrode and a wall of a via;

forming a first dielectric material on the resistance variable memory cell material;

removing a portion of the first dielectric material such that a portion of the resistance variable memory cell material is exposed; and

forming a second electrode on a first exposed portion of the resistance variable memory cell material and third electrode on a second exposed portion of the resistance variable memory cell material;

wherein the first electrode is formed of a material that is different than at least one of the second and the third electrode.

28. A resistance variable memory cell structure, comprising:

a first electrode common to a first and a second resistance variable memory cell;

a first vertically oriented resistance variable material having an arcuate top surface in contact with a second electrode and a non-arcuate bottom surface in contact with the first electrode; and

a second vertically oriented resistance variable material having an arcuate top surface in contact with a third electrode and a non-arcuate bottom surface in contact with the first electrode;

wherein an arcuate portion of the first and the second vertically oriented resistance variable material is located between a first dielectric material and a second dielectric material; and

wherein the arcuate portion of the first vertically oriented resistance variable material is located a distance of not more than 20 nanometers from the arcuate portion of the second vertically oriented resistance variable material.

29. A resistance variable memory cell structure, comprising:

a first electrode common to a first and a second resistance variable memory cell;

a first vertically oriented resistance variable material having an arcuate top surface in contact with a second electrode and a non-arcuate bottom surface in contact with the first electrode; and

a second vertically oriented resistance variable material having an arcuate top surface in contact with a third electrode and a non-arcuate bottom surface in contact with the first electrode;

wherein an arcuate portion of the first and the second vertically oriented resistance variable material is located between a first dielectric material and a second dielectric material; and

wherein a spacer material is formed on the first dielectric material and on an edge of the second electrode and an edge of the third electrode.

30. A resistance variable memory cell structure, comprising:

a first electrode common to a first and a second resistance variable memory cell;

a first vertically oriented resistance variable material having an arcuate top surface in contact with a second electrode and a non-arcuate bottom surface in contact with the first electrode; and

a second vertically oriented resistance variable material having an arcuate top surface in contact with a third electrode and a non-arcuate bottom surface in contact with the first electrode;

wherein the first vertically oriented resistance variable material and the second vertically oriented resistance variable material have a thickness of not greater than 5 nanometers.