C L A I M S

[Claim 1] A memory device controlling method, characterized by:

receiving, by a first semiconductor memory, a read command transmitted from a controller;

receiving, by a second semiconductor memory, a write command transmitted from the controller;

reading, from the first semiconductor memory, data based on the read command, and transmitting, by the first semiconductor memory, to the second memory the data and a control signal indicating that the data is output; and

receiving, by the second semiconductor memory, the data and the control signal transmitted from the first semiconductor memory without intermediation of the controller, and writing the received data into the second semiconductor memory.

[Claim 2] The memory device controlling method according to claim 1, characterized in that

transmitting the data at the first semiconductor memory and receiving the data at the second semiconductor memory are performed based on a SDR (Single Data Rate).

[Claim 3] The memory device controlling method according to claim 1, characterized in that

transmitting the data at the first semiconductor memory and receiving the data at the second semiconductor memory are performed based on a DDR (Double Data Rate),

the first semiconductor memory includes a phase conversion circuit, and

when transmitting by the first semiconductor memory the data and the control signal indicating that the data is output, the control signal whose phase is converted relative to a phase of the data by the phase conversion circuit is transmitted.

[Claim 4] The memory device controlling method according to claim 1, characterized in that

transmitting the data at the first semiconductor memory and receiving the data at the second semiconductor memory are performed based on a DDR (Double Data Rate),

the second semiconductor memory includes a phase conversion circuit,

when transmitting by the first semiconductor memory the data and the control signal indicating that the data is output, a phase of the data and a phase of the control signal are aligned for transmission, and

when receiving by the second semiconductor memory the data at the timing based on the control signal, phases of edges of the received data and the control signal are converted by the phase conversion circuit.

[Claim 5] The memory device controlling method according to claim 1, further comprising:

step of receiving, by the controller including an ECC circuit, the data outputted from the first semiconductor memory;

when detecting an error in the received data, step of correcting the error using the ECC circuit; and

step of transmitting by the controller data in which the error is corrected, from the controller to the second semiconductor memory.

[Claim 6] The memory device controlling method according to claim 1, characterized in that

the first and second semiconductor memories receive a first command for directly transferring the data from the first semiconductor memory to the second semiconductor memory from the controller before receiving the read command and the write command.

[Claim 7] The memory device controlling method according to claim 1, characterized in that

the first semiconductor memory receives a second command that includes a chip address of a memory from which the data is to be read before receiving the read command and a read address subsequently to the read command, and the first semiconductor memory is selected based on the second command, and

the second semiconductor memory receives a third command that includes a chip address of a memory into which the data is to be written before receiving the write command and a write address subsequently to the write command, and the second semiconductor memory is selected based on the third command.

[Claim 8] A memory device, comprising:

a first semiconductor memory controlled by a controller; and

a second semiconductor memory controlled by the controller;

wherein the first semiconductor memory receives a read command that is transmitted from the controller,

the second semiconductor memory receives a write command transmitted from the controller,

the first semiconductor memory reads data from the first semiconductor memory based on the read command, and transmits to the second semiconductor memory the data and a control signal indicating that the data is output, and

the second semiconductor memory receives, based on the write command, the data and the control signal transmitted from the first semiconductor memory without intermediation of the controller, and writes the received data into the second semiconductor memory.

[Claim 9] The memory device according to claim 8, characterized in that

transmitting the data at the first semiconductor memory and receiving the data at the second semiconductor memory are performed based on an SDR (Single Data Rate).

[Claim 10] The memory device according to claim 8, characterized in that

transmitting the data at the first semiconductor memory and receiving the data at the second semiconductor memory are performed based on a DDR (Double Data Rate),

the first semiconductor memory includes a phase conversion circuit,

when transmitting the data, the first semiconductor memory transmits the control signal whose phase is converted relative to a phase of the data by the phase conversion circuit.

[Claim 11] The memory device according to claim 8, characterized in that

transmitting the data from the first semiconductor memory and receiving the data at the second semiconductor memory are performed based on a Double Data Rate (DDR),

the second semiconductor memory includes a phase conversion circuit,

the first semiconductor memory aligns a phase of the data with a phase of the control signal for transmission, and

the second semiconductor memory converts phases of edges of the received data and the control signal by the phase conversion circuit.

[Claim 12] The memory device according to claim 8, characterized in that

the controller including an ECC circuit receives the data transmitted from the first semiconductor memory,

when an error is detected in the received data at the controller, the ECC circuit corrects the error; and

the second semiconductor memory receives a data in which the error is corrected from the controller.

[Claim 13] The memory device according to claim 8, characterized in that

the first and second semiconductor memories receive a first command for directly transferring the data from the first semiconductor memory to the second semiconductor memory from the controller before receiving the read command and the write.

[Claim 14] The memory device according to claim 8, characterized in that

the first semiconductor memory receives a second command that includes a chip address of a memory from which the data is to be read before receiving the read command and a read address subsequently to the read command, and the first semiconductor memory is selected based on the second command, and

the second semiconductor memory receives a third command that includes a chip address of a memory to which the data is to be written before receiving the write command and a write address subsequently to the write command, and the second semiconductor memory is selected based on the third command.