ABSTRACT OF THE DISCLOSURE

A capacitor consisting of a storage electrode (19), a capacitor dielectric film (20) and a plate electrode (21) is formed in a trench formed through dielectric films (6, 8, 10 and 12) stacked on a semiconductor substrate (1) and buried wiring layers (9 and 11) are formed under the capacitor. As the capacitor is formed not in the semiconductor substrate but over it, there is room in area in which the capacitor can be formed and the difficulty of forming wiring is reduced by using the wiring layers (9 and 11) for a global word line and a selector line.

As the upper face of an dielectric film (32) which is in contact with the lower face of wiring (34) in a peripheral circuit area is extended into a memory cell area and is in contact with the side of the capacitor (33), step height between the peripheral circuit area and the memory cell area is remarkably reduced.

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