CLAIMS

1. A method performed in an apparatus which comprises a memory to store a plurality of data values corresponding to an SIMD (Single Instruction, Multiple Data) instruction, and a processor having a plurality of SIMD lanes, wherein each of the plurality of the SIMD lanes is to process one of the plurality of data stored in the memory in accordance with the SIMD instruction, the method comprising:

scaling a plurality of arguments representing floating point numbers to generate a plurality of corresponding scaled arguments;

multiplying the plurality of scaled arguments to generate a first value;

inverting the first value to generate a second value; and

reconstructing a plurality of results, wherein reconstructing each of the plurality of results is based on a multiplication of the second value with ~~one or more~~all of the plurality of scaled arguments except a corresponding one of the plurality of scaled arguments for which the each of the plurality of results is being reconstructed,

wherein the plurality of results correspond to inverted versions of the plurality of arguments.

2. The method of claim 1, wherein inverting the first value is performed by changing a sign of an exponent portion of the first value.

3. The method of claim 1, further comprising converting the~~a~~ floating point ~~version~~ numbers of the plurality of arguments to respective ~~an~~ integer values.

4. The method of claim 1, wherein scaling the plurality of arguments comprises scaling the plurality of arguments by 1.0.

5. The method of claim 1, further comprising storing generated values in a memory.

6. An apparatus comprising:

a memory to store a plurality of data values corresponding to an SIMD (Single Instruction, Multiple Data) instruction; and

a processor having a plurality of SIMD lanes, wherein each of the plurality of the SIMD lanes is to process one of the plurality of data stored in the memory in accordance with the SIMD instruction, wherein the processor is to:

scale ~~an exponent portion and~~ a fraction portion of a first value of the plurality of data values represented by floating point numbers to ~~respectively~~ generate a second value ~~and a third value~~;

negate an exponent portion of the first value to generate a third value;

invert the second value ~~and the third value~~ to ~~respectively~~ generate a fourth value ~~and a fifth value~~; and

multiply the fourth value and the ~~fifth~~ third value to generate an inverse version of the first value, wherein the ~~second value~~exponent portion is to be ~~inverted~~ negated by changing a sign of the exponent portion of the first value.

7. The apparatus of claim 6, wherein the processor is to determine the exponent portion and fraction portion of the first value.

8. The apparatus of claim 6, wherein the processor is to scale the ~~exponent and~~ fraction portions of the first value by 1.0 to generate the second ~~and third~~ values.

9. The apparatus of claim 6, wherein the processor is to convert ~~a~~ the floating point ~~version~~ numbers of the plurality of data values to respective ~~an~~ integer values.

10. The apparatus of claim 6, wherein the memory comprises a cache.

11. The apparatus of claim 6, wherein the processor comprises one or more processor cores.

12. The apparatus of claim 6, wherein the processor is to cause storage of generated values in the memory.

13. The apparatus of claim 6, further comprising a display device to display the inverse version of the first value.

14. A computer-readable medium comprising one or more instructions that when executed on a processor configure the processor to perform one or more operations to:

scale a plurality of arguments representing floating point numbers to generate a plurality of corresponding scaled arguments;

multiply the plurality of scaled arguments to generate a first value;

invert the first value to generate a second value; and

reconstruct a plurality of results, wherein reconstructing each of the plurality of results is based on a multiplication of the second value with ~~one or more~~all of the plurality of scaled arguments except a corresponding one of the plurality of scaled arguments for which the each of the plurality of results is being reconstructed, wherein the plurality of results correspond to inverted versions of the plurality of arguments.

~~15. The computer-readable medium of claim 14, wherein the plurality of results correspond to inverted versions of the plurality of arguments.~~

165. The computer-readable medium of claim 14, further comprising one or more instructions that when executed on a processor configure the processor to invert the first value by changing a sign of an exponent portion of the first value.

176. The computer-readable medium of claim 14, further comprising one or more instructions that when executed on a processor configure the processor to convert ~~a~~ the floating point numbers~~version~~ of the plurality of arguments to ~~an~~respective integer values.

187. The computer-readable medium of claim 14, further comprising one or more instructions that when executed on a processor configure the processor to scale the plurality of arguments by 1.0.

198. The computer-readable medium of claim 14, further comprising one or more instructions that when executed on a processor configure the processor to store generated values in a memory.

~~20~~19. The computer-readable medium of claim 14, further comprising one or more instructions that when executed on a processor configure the processor to multiply an inverted exponent portion and an inverted fraction portion of the plurality of arguments.

20. A method performed in an apparatus which comprises a memory to store a plurality of data values corresponding to an SIMD (Single Instruction, Multiple Data) instruction, and a processor having a plurality of SIMD lanes, wherein each of the plurality of the SIMD lanes is to process one of the plurality of data stored in the memory in accordance with the SIMD instruction, the method comprising:

scaling a fraction portion of a first value of the plurality of data values represented by floating point numbers to generate a second value;

negating an exponent portion of the first value to generate a third value;

inverting the second value to generate a fourth value; and

multiplying the fourth value and the third value to generate an inverse version of the first value, wherein the exponent portion is to be negated by changing a sign of the exponent portion of the first value.

21. A computer-readable medium comprising one or more instructions that when executed on a processor configure the processor to perform one or more operations to:

scale a fraction portion of a first value of the plurality of data values represented by floating point numbers to generate a second value;

negate an exponent portion of the first value to generate a third value;

invert the second value to generate a fourth value; and

multiply the fourth value and the third value to generate an inverse version of the first value, wherein the exponent portion is to be negated by changing a sign of the exponent portion of the first value.