WHAT IS CLAIMED IS:

1. A memory device, comprising:

a first power rail for transmitting a high power voltage;

a second power rail for transmitting a low power voltage;

a third power rail configured to selectively receive the high power voltage from the first power rail through a first dynamic voltage and frequency scaling (DVFS) switch, and to selectively receive the low power voltage from the second power rail through a second DVFS switch;

a fourth power rail connected through a first power gating (PG) switch to selectively receive the high power voltage or the low power voltage from the third power rail; and

a first circuit block connected to the fourth power rail to selectively receive a power voltage to which the DVFS and the power gating are applied,

wherein the first circuit block selectively receives the high power voltage or the low power voltage as the power voltage as the first PG switch is turned on, and wherein supply of the high power voltage and the low power voltage to the first circuit block is blocked as the first PG switch is turned off.

2. The memory device of claim 1, further comprising a second circuit block connected to the third power rail to regularly receive the high power voltage or the low power voltage.

3. The memory device of claim 2, further comprising a third circuit block connected to the third power rail and the fourth power rail,

wherein some circuits in the third circuit block are connected to the third power rail,

and

wherein some other circuits in the third circuit block are connected to the fourth power rail.

4. The memory device of claim 1,

wherein the high power voltage is a VDD2H voltage defined in a low power double data rate 5 (LPDDR 5) specification, and

wherein the low power voltage is a VDD2L voltage defined in the LPDDR5 specification.

5. The memory device of claim 1, further comprising:

a second PG switch connected between the first power rail and the fourth power rail; and

a third PG switch connected between the second power rail and the fourth power rail.

6. The memory device of claim 5,

wherein the first DVFS switch is turned on in a first period in which the high power voltage is provided to the third power rail and the second DVFS switch is turned on in a second period in which the low power voltage is provided to the third power rail, and

wherein the first PG switch is turned on in at least a partial period in each of the first period and the second period.

7. The memory device of claim 6,

wherein the second PG switch is turned on together with the first PG switch in the first period, and

wherein the third PG switch is turned on together with the first PG switch in the second period.

8. The memory device of claim 1, further comprising:

a fifth power rail for regularly transmitting the high power voltage;

a second PG switch connected between the first power rail and the fourth power rail; and

a third PG switch connected between the first power rail and the fifth power rail,

wherein the high power voltage is selectively provided to the fourth power rail and the fifth power rail through a single switching operation.

9. The memory device of claim 8, further comprising:

a first voltage region including one or more data processing blocks for transmitting data to be stored in a memory cell array or read from the memory cell array; and

a second voltage region including one or more control blocks for controlling the data processing blocks,

wherein the first voltage region is connected to the third power rail or the fourth power rail to receive the power voltage to which DVFS is applied, and wherein the second voltage region is connected to the fifth power rail to regularly receive the high power voltage.

10. A memory device, comprising:

a power rail/control switch block having a plurality of power rails, including first and second power rails to transmit power voltages used for the memory device, and a plurality of switches connected to the plurality of power rails to control transmission of the power voltages;

a first voltage region connected to the first power rail for selectively transmitting a high power voltage or a low power voltage as dynamic voltage and frequency scaling (DVFS) is applied; and

a second voltage region connected to the second power rail configured to selectively transmit the high power voltage or the low power voltage or block transmission of the high power voltage and the low power voltage as the DFVS and a power gating (PG) are applied,

wherein the second power rail selectively receives the high power voltage from a third power rail for selectively transmitting the high power voltage to the second power rail by a single switching operation.

11. The memory device of claim 10, wherein the power rail/control switch block comprises:

a first DVFS switch connected between the third power rail and the first power rail;

a second DVFS switch connected between the first power rail and a fourth power rail for selectively transmitting the low power voltage from the first power rail to the fourth power rail;

a first power gating (PG) switch connected between the first power rail and the second power rail; and

a second PG switch connected between the third power rail and the second power rail,

wherein, as the second PG switch is turned on, the high power voltage is transmitted from the third power rail to the second power rail by the single switching operation.

12. The memory device of claim 11, wherein, as the first PG switch and the second PG switch are turned on, the high power voltage is transmitted to the second power rail through the first PG switch and the second PG switch.

13. The memory device of claim 11, wherein the power rail/control switch block further comprises a third PG switch connected between the fourth power rail and the second power rail.

14. The memory device of claim 13,

wherein the first DVFS switch and the second DVFS switch are alternately turned on, and

wherein the first PG switch is turned on at timing irrelevant to timing of switching operations for the first and second DVFS switches.

15. The memory device of claim 14,

wherein the second PG switch is turned on together with the first PG switch in a first period in which the first DVFS switch is turned on, and

wherein the third PG switch is turned on together with the first PG switch in a second period in which the second DVFS switch is turned on.

16. The memory device of claim 10,

wherein the high power voltage is a VDD2H voltage defined in a LPDDR 5 specification, and

wherein the low power voltage is a VDD2L voltage defined in the LPDDR5 specification.

17. A memory device that operates in accordance with a low power double data rate (LPDDR) specification, the memory device comprising:

a first power rail for transmitting a first power voltage (VDD1);

a second power rail for transmitting a second high power voltage (VDD2H);

a third power rail for transmitting a second low power voltage (VDD2L);

a fourth power rail configured to selectively transmit the second high power voltage or the second low power voltage based on an operation mode of the memory device as dynamic voltage and frequency scaling (DVFS) is applied;

a fifth power rail for selectively transmitting the second high power voltage or the second low power voltage or blocking transmission of the second high power voltage and second low power voltage as the DVFS and PG are applied; and

a control switch block including a plurality of switches for controlling transmission of one or more of the power voltages between the first to fifth power rails,

wherein, based on control of the control switch block, the fifth power rail is selectively connected to the fourth power rail and is further selectively connected to at least one of the second power rail and the third power rail.

18. The memory device of claim 17,

wherein the memory device receives the first power voltage, the second high power voltage, and the second low power voltage from an external power management integrated circuit, and

wherein the first power voltage has a higher voltage level than the second high power voltage and the second high power voltage has a higher voltage level than the second low power voltage.

19. The memory device of claim 17, wherein the control switch block comprises:

a first DVFS switch connected between the second power rail and the fourth power

rail;

a second DVFS switch connected between the third power rail and the fourth power rail;

a first PG switch connected between the fourth power rail and the fifth power rail; and

a second PG switch connected between the second power rail and the fifth power rail.

20. The memory device of claim 19, further comprising a third PG switch connected between the third power rail and the fifth power rail.