



FIG. 1

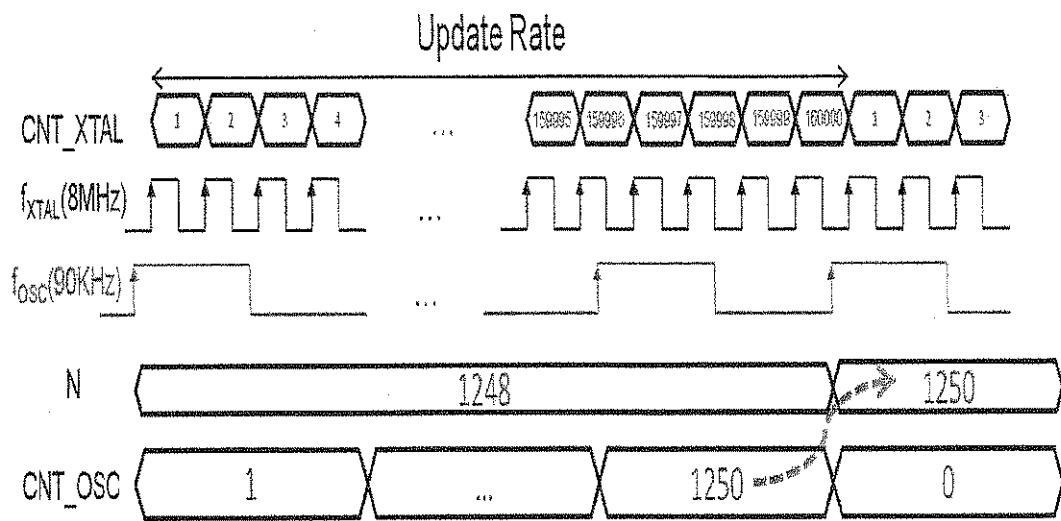


FIG. 2A

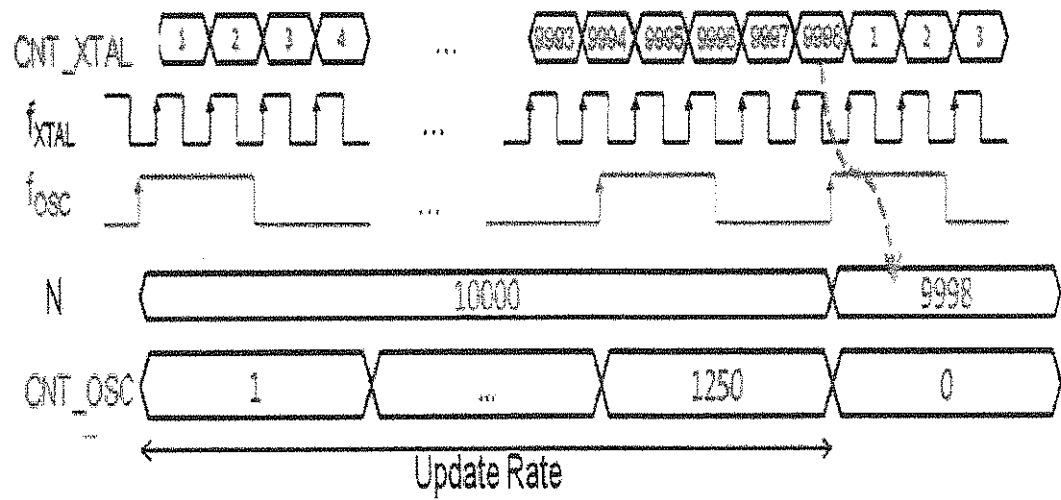


FIG. 2B

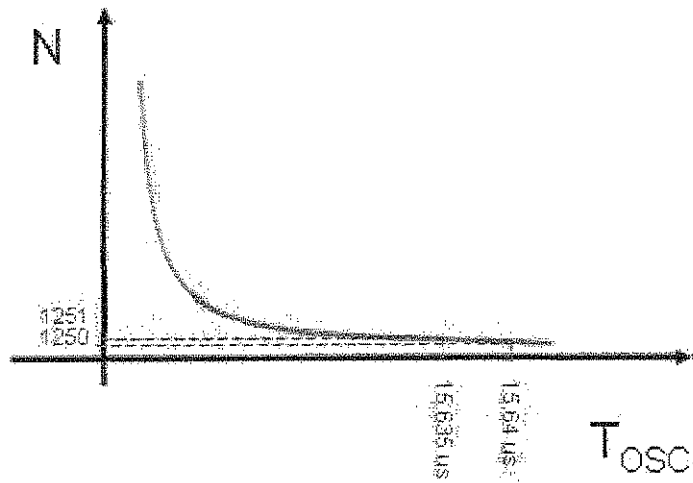


FIG. 3A

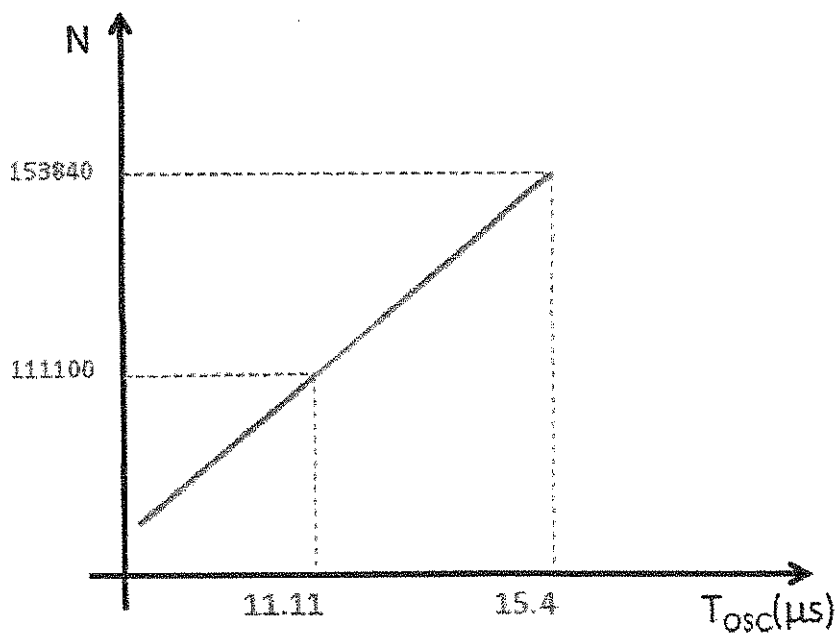


FIG. 3B

Timing diagram for a CMOS inverter with a load capacitor. The output voltage starts at V_{DD} , then discharges through the load capacitor with a slope $S1 = I_{REF}/C$. It then enters a second phase where it discharges more rapidly with a slope $S2 = I_{MAX} + I_{REF}/C$. The total delay is the sum of $T1$ and $T2$. The voltage levels V_{DD} , V_{TH} , and $V_{REF,COMP}$ are marked on the y-axis.

FIG. 5

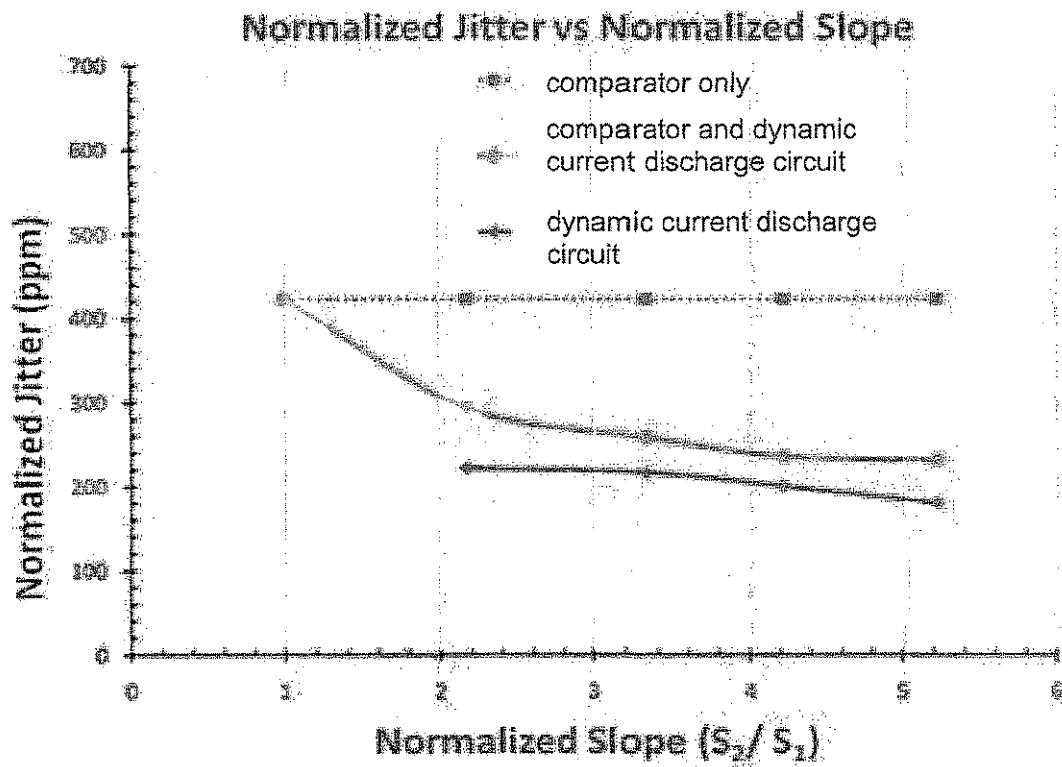


FIG. 6

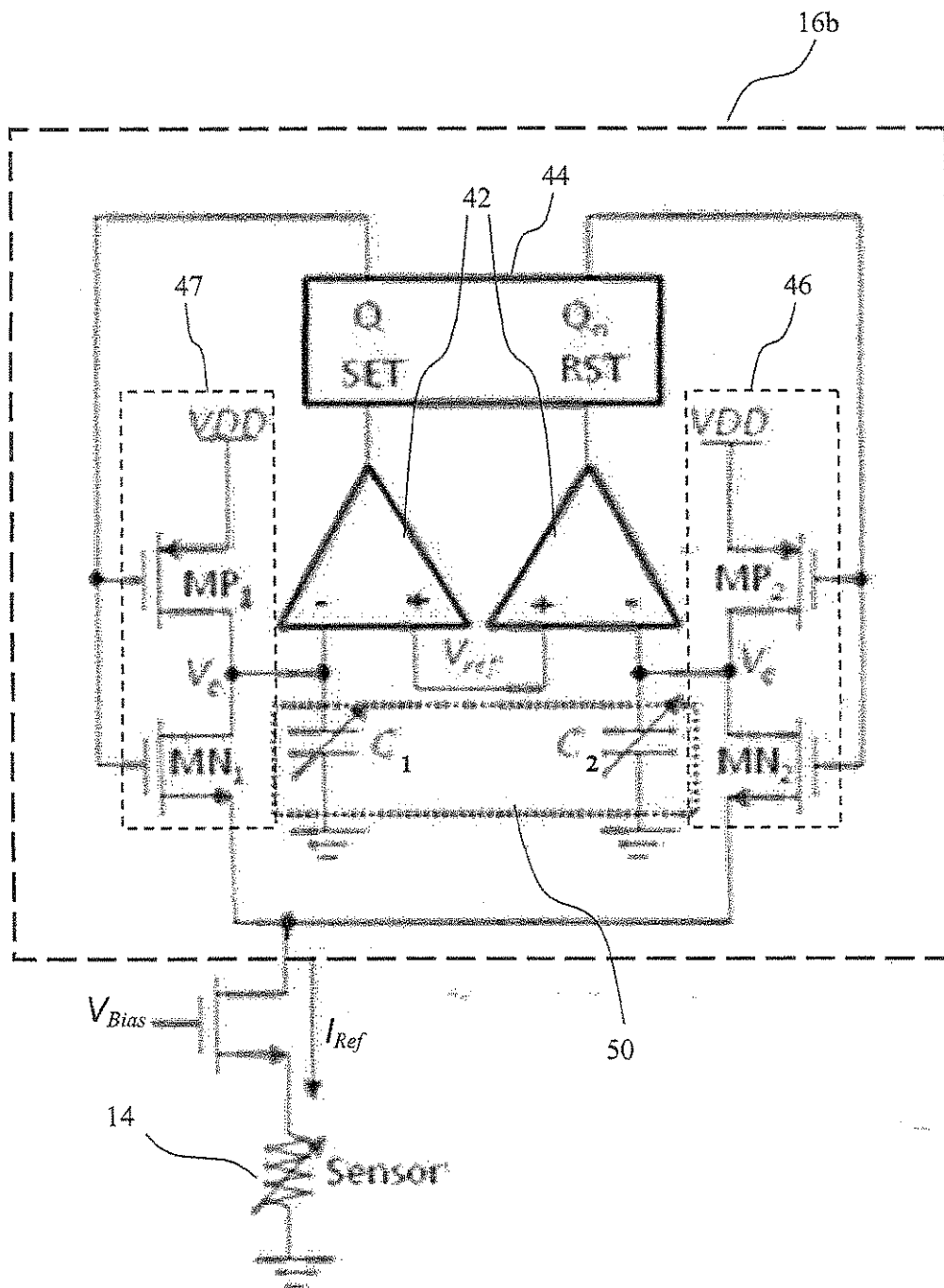


FIG. 7

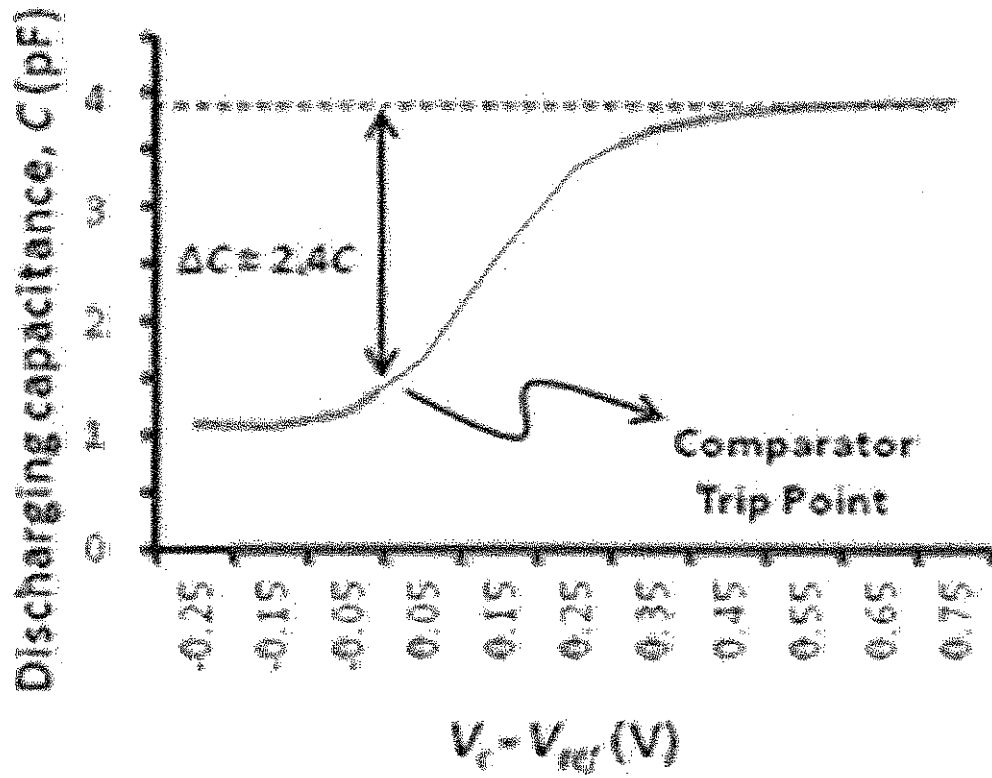


FIG. 8

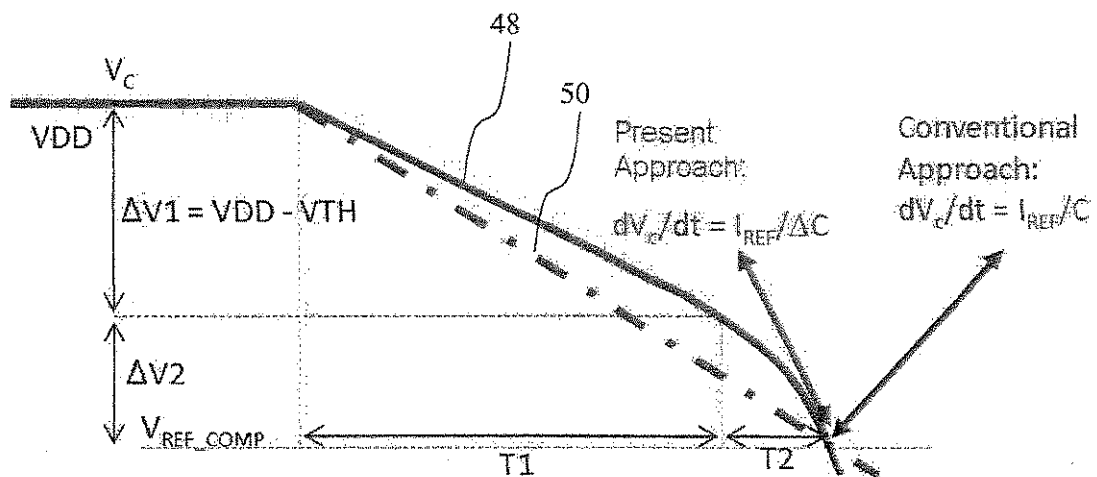


FIG. 9

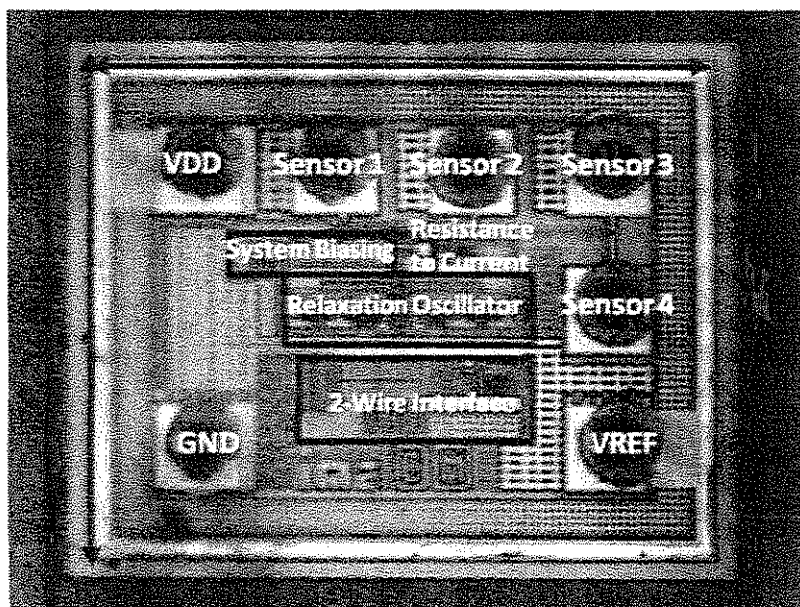


FIG. 10

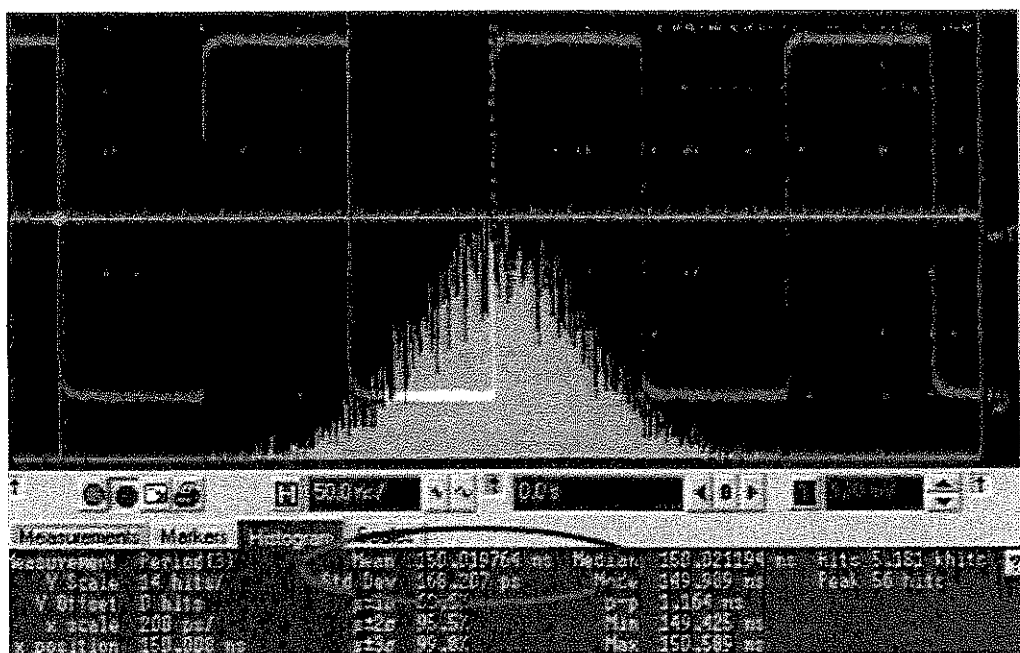


FIG. 11A

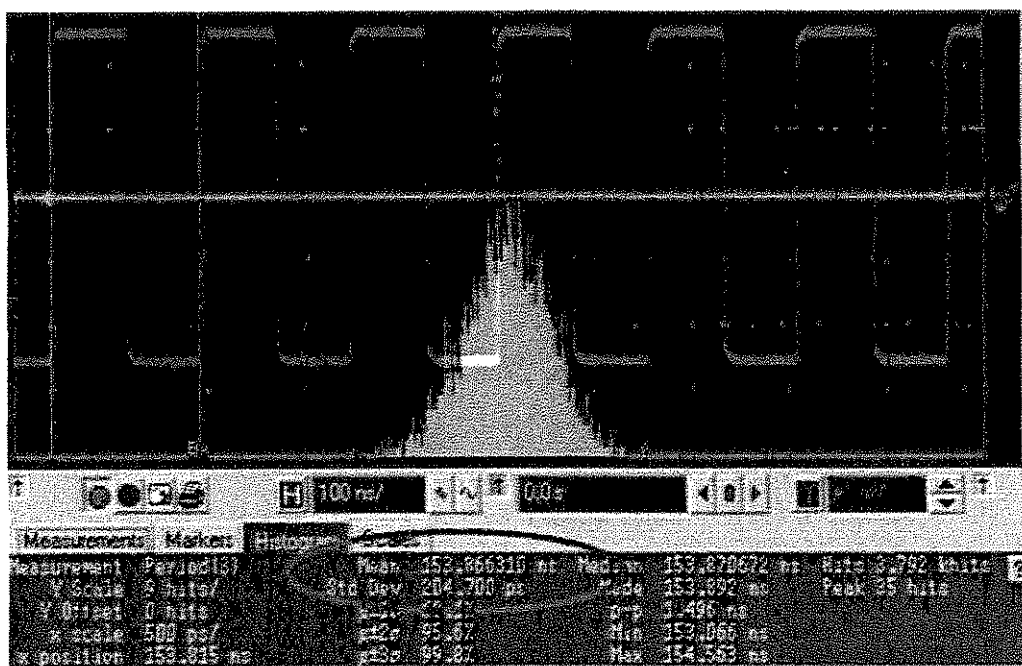


FIG. 11B

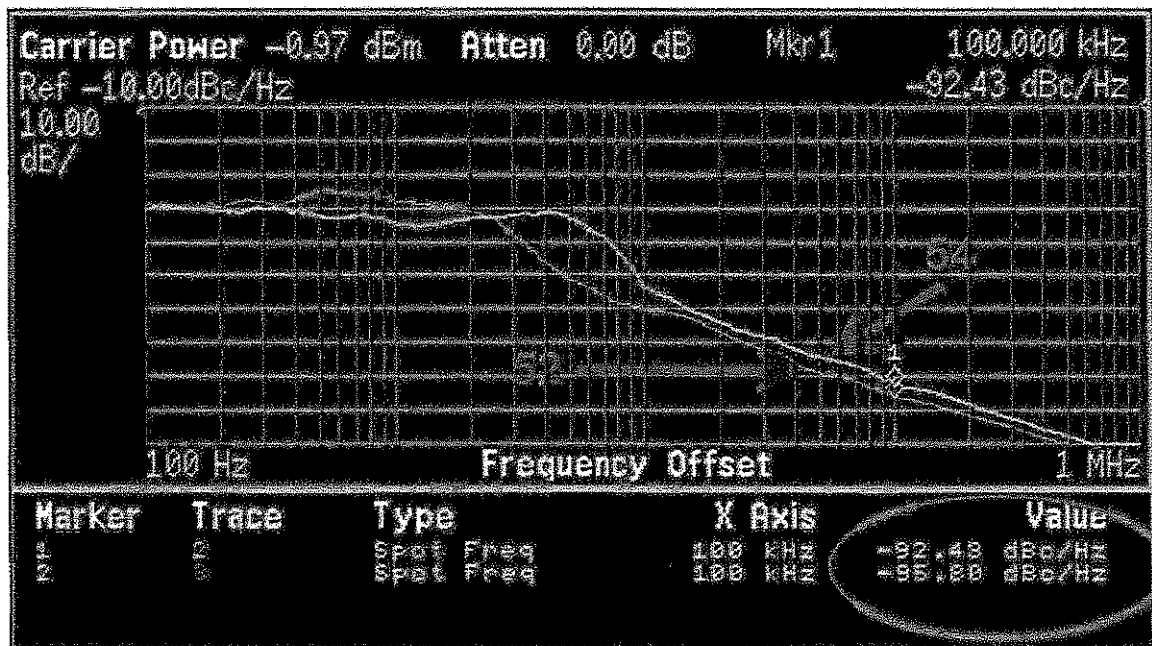


FIG. 12

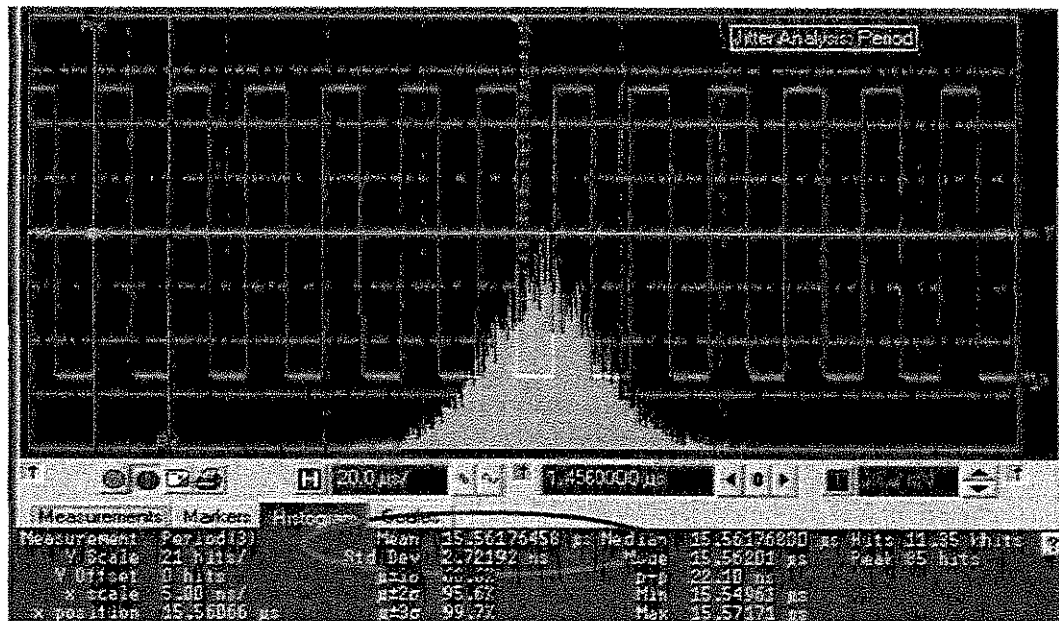


FIG. 13A

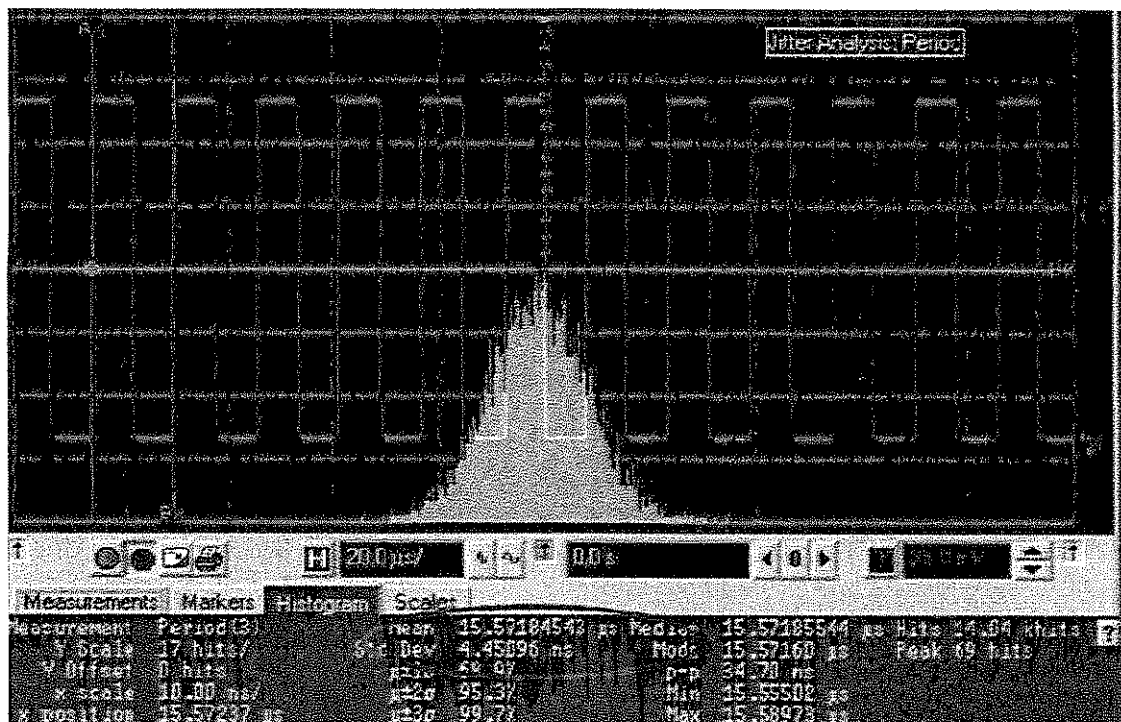


FIG. 13B

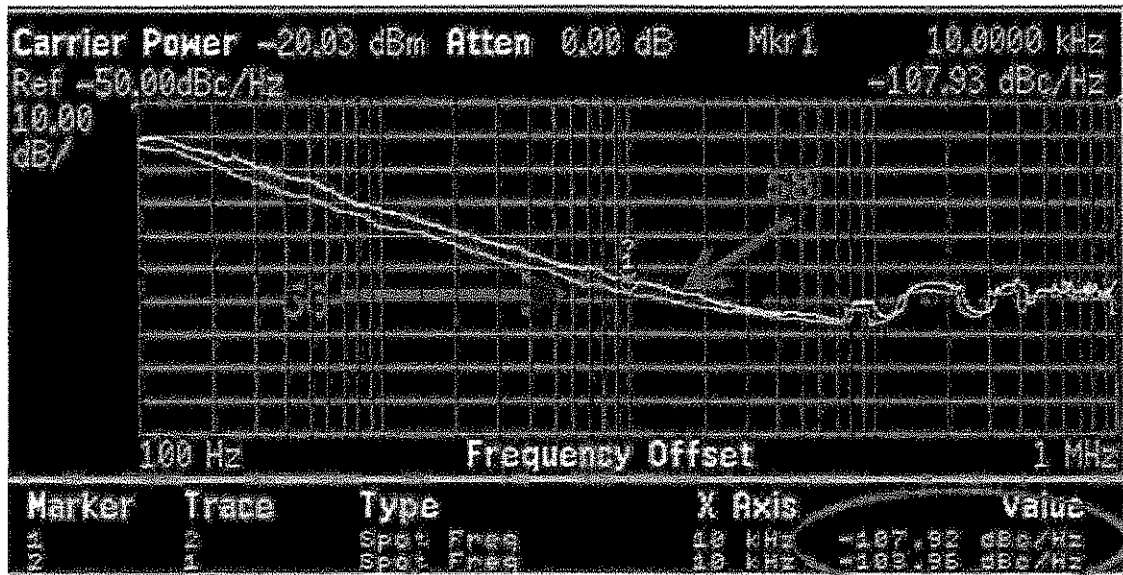


FIG. 14

Number of Edges v.s. Sensing Resistance

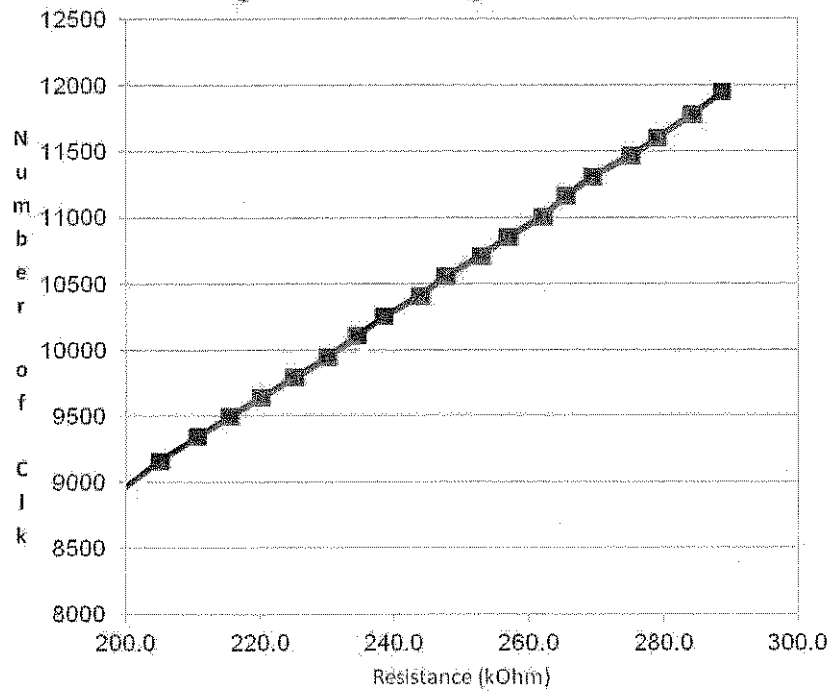


FIG. 15A

Number of Edges v.s. Sensing Resistance

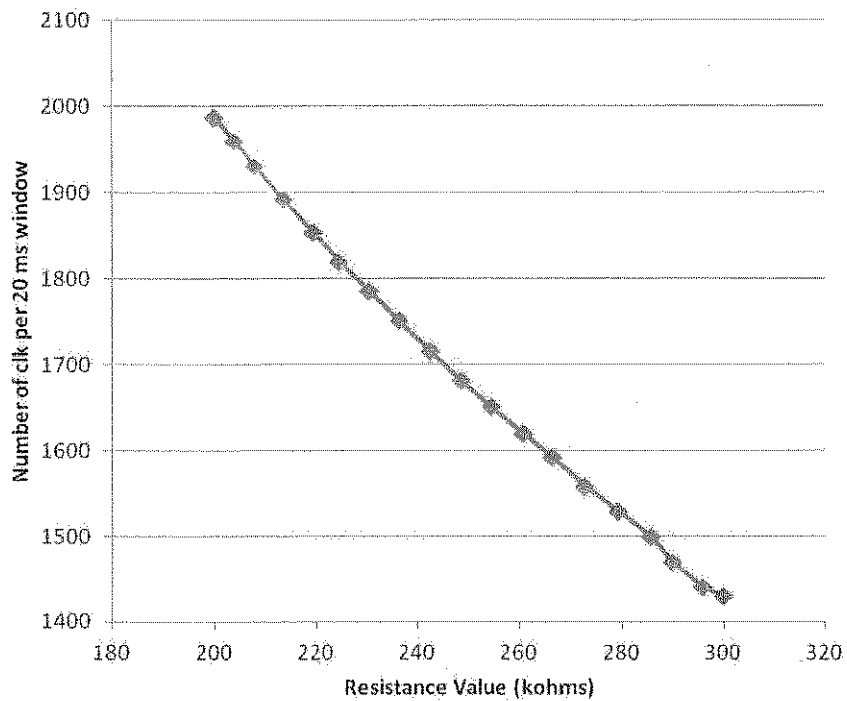


FIG. 15B