CLAIMS

1. A grid array capacitor located between an integrated circuit (IC) package and a printed circuit board (PCB), the grid array capacitor configured to be physically and electrically coupled to the IC package and to the PCB, the grid array capacitor comprising:

an inner conductor configured to be electrically connected to the IC package and to the PCB, wherein the inner conductor is a helical coil;

an inner dielectric in a coaxial orientation to and at least partially surrounding the inner conductor; and

a secondary conductor in a coaxial orientation to and at least partially surrounding the inner dielectric, the secondary conductor configured to be electrically connected to the IC package and to the PCB.

2. The grid array capacitor of claim 1 further comprising:

an outer dielectric in a coaxial orientation to and at least partially surrounding the secondary conductor; and

an outer conductor in a coaxial orientation to and at least partially surrounding the outer dielectric, the outer conductor configured to be electrically connected to the IC package and to the PCB.

3. The grid array capacitor of claim 2, wherein the outer dielectric is selected from the group consisting of: polyimide and barium titanate.

4. The grid array capacitor of claim 1, wherein the inner conductor is a wire.

5. The grid array capacitor of claim 1, wherein the secondary conductor includes materials selected from the group consisting of: copper, tin, nickel, niobium and titanium.

6. The grid array capacitor of claim 1, wherein a capacitance of the grid array capacitor is in a range between 1 nF and 8 nF.

7. The grid array capacitor of claim 1, wherein the secondary conductor is a helical coil.

8. The grid array capacitor of claim 1, wherein the secondary conductor is a hollow cylindrical sleeve.

9. An electronic system comprising:

a printed circuit board (PCB);

an integrated circuit (IC) package;

a grid array capacitor located between the IC package and the PCB, the grid array capacitor physically and electrically coupled to the IC package and to the PCB, the grid array capacitor comprising:

an inner conductor physically and electrically connected to the IC package and to the PCB, wherein the inner conductor is a helical coil;

an inner dielectric in a coaxial orientation to and at least partially surrounding the inner conductor; and

a secondary conductor in a coaxial orientation to and at least partially surrounding the inner dielectric, the secondary conductor physically and electrically connected to the IC package and to the PCB.

10. The electronic system of claim 9, wherein the secondary conductor is a helical coil.

11. The electronic system of claim 9, wherein the secondary conductor is a hollow cylindrical sleeve.

12. The electronic system of claim 9, wherein the inner dielectric is selected from the group consisting of: polyimide and barium titanate.

13. A grid array capacitor located between an integrated circuit (IC) package and a printed circuit board (PCB), the grid array capacitor configured to be physically and electrically coupled to the IC package and to the PCB, the grid array capacitor comprising:

an inner conductor configured to be electrically connected to the IC package and to the PCB;

an inner dielectric in a coaxial orientation to and at least partially surrounding the inner conductor; and

a secondary conductor in a coaxial orientation to and at least partially surrounding the inner dielectric, the secondary conductor configured to be electrically connected to the IC package and to the PCB;

wherein the secondary conductor includes a first section adjacent to a first end and a second section adjacent to a second end, wherein the first section and the second section are spaced and electrically insulated from each other in a longitudinal direction of the coaxial orientation.