

## ABSTRACT OF THE DISCLOSURE

Provided are memory devices and memory systems. The memory device includes a memory cell array in a first semiconductor layer and including word lines stacked in a first direction, and channel structures passing through the word lines in the first direction; a control logic circuit in a second semiconductor layer located below the first semiconductor layer in the first direction; and a physical unclonable function (PUF) circuit including a plurality of through electrodes passing through the first semiconductor layer and the second semiconductor layer, and configured to generate PUF data according to resistance values of the plurality of through electrodes, and generate the PUF data based on a node voltage between through electrodes connected in series, among the plurality of through electrodes.

FIG. 6