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SEMICONDUCTOR INTEGRATED CIRCUIT AND DATA PROCESSING SYSTEM**ABSTRACT OF THE DISCLOSURE**

To enhance the speed of first access (read access different in word line from the previous access) to a multi-bank memory, multi-bank memory macro structures are used. Data are held in a sense amplifier for every memory bank. When access is hit to the held data, data latched by the sense amplifier are output to thereby enhance the speed of first access to the memory macro structures. Namely, each memory bank is made to function as a sense amplifier cache. To enhance the hit ratio of such a sense amplifier cache more greatly, an access controller self-prefetches the next address (an address to which a predetermined offset has been added) after access to a memory macro structure so that data in the self-prefetched address are prered by a sense amplifier in another memory bank.

Figure 1