CLAIMS

1. A control method, applied to a semiconductor memory, the semiconductor memory comprising a Data Mask Pin (DM), the DM being configured to receive an input mask signal for write data, and the method comprising:

when the semiconductor memory is in a preset test mode,

controlling an impedance of the DM to be a first impedance parameter through a first Mode Register (MR), in response to the DM being selected as a test object; or,

controlling the impedance of the DM to be a second impedance parameter through a second MR, in response to the DM not being selected as the test object;

wherein the semiconductor memory further comprises at least one Data Pin (DQ), the DQ is configured to receive or output data, the first MR is configured to indicate that an impedance of the at least one DQ in an output driver state is the first impedance parameter, and the second MR is configured to indicate that the impedance of the at least one DQ in a termination state is the second impedance parameter.

2. The control method according to claim 1, wherein when the semiconductor memory is in the preset test mode, the method further comprises:

controlling, through the first MR, the impedance of the DQ to be the first impedance parameter, in response to the DQ being selected as the test object; or,

controlling, through the second MR, the impedance of the DQ to be the second impedance parameter, in response to the DQ not being selected as the test object.

3. The control method according to claim 1, wherein the method further comprises:

determining, through a third MR, that the semiconductor memory enters the preset test mode and selects the test object; or,

determining, through the third MR, that the semiconductor memory does not enter the

preset test mode.

4. The control method according to claim 3, wherein in a case of determining that the semiconductor memory enters the preset test mode, the method further comprises:

acquiring a first Operand (OP) in the first MR, a second OP in the second MR, and a third OP in the third MR;

decoding the third OP to obtain a first test flag signal; wherein the first test flag signal indicates whether the DM is the test object; and

selecting one of the first OP and the second OP to control the impedance of the DM according to the first test flag signal.

5. The control method according to claim 4, wherein the method further comprises:

determining a first non-test state control signal and a second impedance control signal;

when the semiconductor memory is in the preset test mode, determining, based on one of the first OP and the second OP, a first impedance control signal according to the first test flag signal; or, when the semiconductor memory is not in the preset test mode, determining, based on the first non-test state control signal, the first impedance control signal; and

selecting, according to a working state of the semiconductor memory, one of the first impedance control signal and the second impedance control signal to control the impedance of the DM;

wherein the first non-test state control signal is configured to indicate the impedance of the DM in a mode other than the preset test mode, and the second impedance control signal is configured to indicate the impedance of the DQ in the output driver state; or the first non-test state control signal is configured to indicate the impedance of the DQ in the output driver state, and the second impedance control signal is configured to indicate the impedance of the DM in the mode other than the preset test mode.

6. The control method according to claim 4, wherein in the case of determining that the semiconductor memory enters the preset test mode, the method further comprises:

decoding the third OP to obtain at least one second test flag signal, wherein one of the at least one second test flag signal indicates whether one of the at least one DQ is the test object; and

selecting, according to the second test flag signal, one of the first OP and the second OP to control the impedance of a respective one of the at least one DQ.

7. The control method according to claim 6, wherein the method further comprises:

determining a third non-test state control signal, a fourth impedance control signal and a fifth impedance control signal;

when the semiconductor memory is in the preset test mode, determining, based on one of the first OP and the second OP, a third impedance control signal according to the second test flag signal; or, when the semiconductor memory is not in the preset test mode, determining, based on the third non-test state control signal, the third impedance control signal; and

selecting, according to the working state of the semiconductor memory, the third impedance control signal and the fifth impedance control signal to control the impedance of the DQ, or selecting, according to the working state of the semiconductor memory, the fourth impedance control signal and the fifth impedance control signal to control the impedance of the DQ;

wherein the third non-test state control signal is configured to indicate the impedance of a corresponding DQ in the termination state, and the fourth impedance control signal and the fifth impedance control signal are jointly configured to indicate the impedance of the corresponding DQ in the output driver state; or the third non-test state control signal and the fifth impedance control signal are jointly configured to indicate the impedance of the corresponding DQ in the output driver state, and the fourth impedance control signal is

configured to indicate the impedance of the corresponding DQ in the termination state.

8. The control method according to claim 4, wherein the preset test mode is a Package Output Driver Test Mode (PODTM), and the PODTM is configured to test the impedance of the DM or the at least one DQ after packaging;

the first MR has a standard serial number of 5, and the first OP refers to an OP from a second bit to a first bit stored in the first MR;

the second MR has a standard serial number of 34, and the second OP refers to an OP from a second bit to a 0^{th} bit stored in the second MR; and

the third MR has a standard serial number of 61, and the third OP refers to an OP from a 4^{th} bit to a 0^{th} bit stored in the third MR.

9. A semiconductor memory, comprising a first Mode Register (MR), a second MR, a Data Mask Pin (DM), and a first driver circuit connected to the first MR, the second MR and the DM respectively; wherein

the DM is configured to receive an input mask signal for write data;

the first driver circuit is configured to, when the semiconductor memory is in a preset test mode, control an impedance of the DM to be a first impedance parameter according to the first MR in response to the DM being selected as a test object, or control the impedance of the DM to be a second impedance parameter according to the second MR in response to the DM not being selected as the test object;

wherein the semiconductor memory further comprises at least one Data Pin (DQ), the DQ is configured to receive or output data, the first MR is configured to indicate that an impedance of the at least one DQ in an output driver state is the first impedance parameter, and the second MR is configured to indicate that an impedance of the at least one DQ in a termination state is the second impedance parameter.

10. The semiconductor memory according to claim 9, wherein the semiconductor memory further comprises at least one second driver circuit, and each of the at least one second driver circuit is connected with the first MR, the second MR and one of the at least one DQ; wherein

the second driver circuit is configured to, when the semiconductor memory is in the preset test mode, control the impedance of the DQ to be the first impedance parameter through the first MR in response to the DQ being selected as the test object, or control the impedance of the DQ to be the second impedance parameter through the second MR in response to the DQ not being selected as the test object.

11. The semiconductor memory according to claim 10, wherein the semiconductor memory further comprises a third MR and a first decoding module; wherein

the first MR is configured to store and output a first Operand (OP) ;

the second MR is configured to store and output a second OP;

the third MR is configured to store and output a third OP; wherein the third OP is configured to indicate whether the semiconductor memory enters the preset test mode;

the first decoding module is configured to receive the third OP, decode the third OP and output a first test flag signal; wherein the first test flag signal is configured to indicate whether the DM is the test object; and

the first driver circuit is further configured to receive the first test flag signal, the first OP and the second OP; and select one of the first OP and the second OP to control the impedance of the DM according to the first test flag signal in a case that the semiconductor memory enters the preset test mode.

12. The semiconductor memory according to claim 11, wherein the semiconductor memory is further configured to determine a first non-test state control signal, a second impedance control signal and a first calibration signal; wherein the first calibration signal is configured to calibrate a pull-up resistance value;

the first driver circuit comprises:

a first signal processing module, configured to receive the first test flag signal, the first OP, the second OP and the first non-test state control signal; and output, based on one of the first OP and the second OP, a first impedance control signal according to the first test flag signal when the semiconductor memory is in the preset test mode; or, output, based on the first non-test state control signal, the first impedance control signal when the semiconductor memory is not in the preset test mode;

a first logic module, configured to receive the first impedance control signal, the second impedance control signal and the first calibration signal; and select and logically combine the first impedance control signal, the second impedance control signal and the first calibration signal to output a first target signal; and

a first driver module, comprising a plurality of first impedance units and configured to receive the first target signal, and control the plurality of first impedance units by using the first target signal, so as to control an impedance of the DM;

wherein the first non-test state control signal is configured to indicate the impedance of the DM in a mode other than the preset test mode, and the second impedance control signal is configured to indicate the impedance of the DQ in the output driver state; or, the first non-test state control signal is configured to indicate the impedance of the DQ in the output driver state, and the second impedance control signal is configured to indicate the impedance of the DM in the mode other than the preset test mode.

13. The semiconductor memory according to claim 12, wherein the first signal processing module comprises:

a second decoding module, configured to receive the first OP, decode the first OP and output a first decoded signal;

a third decoding module, configured to receive the second OP, decode the second OP and output a second decoded signal;

a first selection module, configured to receive the first test flag signal, the first

decoded signal and the second decoded signal; and select one of the first decoded signal and the second decoded signal to output a first test state control signal according to the first test flag signal; and

a second selection module, configured to receive a test enable signal, the first test state control signal and the first non-test state control signal; and select one of the first test state control signal and the first non-test state control signal to output the first impedance control signal according to the test enable signal; wherein the test enable signal is configured to indicate whether the semiconductor memory is in the preset test mode.

14. The semiconductor memory according to claim 13, wherein each of the first decoded signal, the second decoded signal, the first test state control signal, the first non-test state control signal and the first impedance control signal comprises (M+l) bits of sub-signals, the first selection module comprises (M+l) first data selectors, and the second selection module comprises (M+1) second data selectors; wherein

an input of one of the first data selectors is configured to receive a 1-bit sub-signal of the first decoded signal and a 1-bit sub-signal of the second decoded signal, an output of one of the first data selectors is configured to output a 1-bit sub-signal of the first test state control signal, and control ends of all the first data selectors are configured to receive the first test flag signal;

an input of one of the second data selectors is configured to receive a 1-bit sub-signal of the first test state control signal and a 1-bit sub-signal of the first non-test state control signal, an output of one of the second data selectors is configured to output a 1-bit sub-signal of the first impedance control signal, and the control ends of all the second data selectors are configured to receive the test enable signal;

wherein M is a positive integer.

15. The semiconductor memory according to claim 14, wherein the second impedance control signal comprises (M+1) bits of sub-signals, the first calibration signal comprises N bits of sub-signals, the first target signal comprises I groups of sub-signals, and each group of the

sub-signals comprises N bits of sub-signals;

the first driver module comprises I first impedance units, and each of the first impedance units is configured to receive a group of sub-signals in the first target signal; wherein

the first logic module is specifically configured to determine whether a level pull-up function of at least one of the first impedance units is enabled according to the first impedance control signal and the second impedance control signal; and determine, in a case that a level pull-up function of an i^{th} first impedance unit is enabled, a level state of an i^{th} group of sub-signals in the first target signal according to the first calibration signal, so as to control a resistance value of the i^{th} first impedance unit to be a standard resistance value; or determine, in a case that the level pull-up function of the i^{th} first impedance unit is disabled, that the i^{th} group of sub-signals in the first target signal are in a first level state;

wherein each of the first impedance units comprises N first switch transistors, N second switch transistors and 2N first resistors, a control end of an n^{th} first switch transistor in the i^{th} first impedance unit is connected with an n^{th} sub-signal in the i^{th} group of sub-signals in the first target signal, a first end of one of the first switch transistors is connected with a first end of one of the first resistors, and a second end of one of the first switch transistors is connected with a power signal; a control end of one of the second switch transistors is connected with a ground signal, a first end of one of the second switch transistors is connected with the ground signal, a second end of one of the second switch transistors is connected with the first end of one of the first resistors, and second ends of the 2N first resistors are all connected with the DM;

wherein n, i, N, and I are all integers, n is less than or equal to N, i is less than or equal to A, and (M+1) is less than or equal to I.

16. The semiconductor memory according to claim 11, wherein

the first decoding module is further configured to decode the third OP and output at least one second test flag signal; wherein one of the at least one second test flag signal is configured to indicate whether one of the at least one DQ is the test object; and

the second driver circuit is further configured to receive a corresponding second test flag signal, the first OP and the second OP; and select, in a case that the semiconductor memory enters the preset test mode, one of the first OP and the second OP to control the impedance of the DQ according to the second test flag signal.

17. The semiconductor memory according to claim 16, wherein the semiconductor memory is further configured to determine a third non-test state control signal, a fourth impedance control signal, a fifth impedance control signal, a second calibration signal and a third calibration signal; wherein the second calibration signal is configured to calibrate a pull-up resistance value, and the third calibration signal is configured to calibrate a pull-down resistance value;

the second driver circuit comprises:

a second signal processing module, configured to receive the second test flag signal, the first OP, the second OP and the third non-test state control signal; and output a third impedance control signal based on one of the first OP and the second OP according to the second test flag signal when the semiconductor memory is in the preset test mode; or output the third impedance control signal based on the third non-test state control signal when the semiconductor memory is not in the preset test mode;

a second logic module, configured to receive the third impedance control signal, the fourth impedance control signal and the second calibration signal; and select and logically combine the fourth impedance control signal and the second calibration signal to output a second target signal;

a third logic module, configured to receive the fifth impedance control signal and the third calibration signal, and logically combine the fifth impedance control signal and the third calibration signal to output a third target signal; and

a second driver module, comprising a plurality of second impedance units and configured to receive the second target signal and the third target signal, and control the plurality of second impedance units by using the second target signal and the third target signal, so as to control the impedance of the corresponding DM;

wherein the third non-test state control signal is configured to indicate the impedance of the corresponding DQ in the termination state, and the fourth impedance control signal and the fifth impedance control signal are jointly configured to indicate the impedance of the corresponding DQ in the output driver state; or the third non-test state control signal and the fifth impedance control signal are jointly configured to indicate the impedance of the corresponding DQ in the output driver state, and the fourth impedance control signal is configured to indicate the impedance of the corresponding DQ in the termination state.

18. The semiconductor memory according to claim 17, wherein the second signal processing module comprises:

a fourth decoding module, configured to receive the first OP, decode the first OP and output a third decoded signal;

a fifth decoding module, configured to receive the second OP, decode the second OP and output a fourth decoded signal;

a third selection module, configured to receive the second test flag signal, the third decoded signal and the fourth decoded signal; and select, according to the second test flag signal, one of the third decoded signal and the fourth decoded signal to output a third test state control signal; and

a fourth selection module, configured to receive the test enable signal, the third test state control signal and the third non-test state control signal, and select, according to the test enable signal, one of the third test state control signal and the third non-test state control signal to output the third impedance control signal; wherein the test enable signal is configured to indicate whether the semiconductor memory is in the preset test mode.

19. The semiconductor memory according to claim 18, wherein each of the third decoded signal, the fourth decoded signal, the third test state control signal, the third non-test state control signal and the third impedance control signal comprises (M+l) bits of sub-signals, the third selection module comprises (M+l) third data selectors, and the fourth selection module comprises (M+1) fourth data selectors; wherein

an input of one of the third data selectors is configured to receive a 1-bit sub-signal of the third decoded signal and a 1-bit sub-signal of the fourth decoded signal, an output of one of the third data selectors is configured to output a 1-bit sub-signal of the third test state control signal, and control ends of all the third data selectors are configured to receive the second test flag signal;

an input of one of the fourth data selectors is configured to receive the 1-bit sub-signal of the third test state control signal and a 1-bit sub-signal of the third non-test state control signal, an output of one of the fourth data selectors is configured to output a 1-bit sub-signal of the third impedance control signal, and control ends of all the fourth data selectors are configured to receive the test enable signal.

20. The semiconductor memory according to claim 19, wherein the fourth impedance control signal comprises (M+1) bits of sub-signals, each of the second calibration signal and the third calibration signal comprises N bits of sub-signals, each of the second target signal and the third target signal comprises I groups of sub-signals, and each group of the sub-signals comprises N bits of sub-signals;

the second driver module comprises I second impedance units, and each of the second impedance units is configured to receive a group of sub-signals in the second target signal and a group of sub-signals in the third target signal; wherein

the second logic module is specifically configured to determine whether a level pull-up function of the at least one of the second impedance units is enabled according to the third impedance control signal and the fourth impedance control signal; and determine, in a case that a level pull-up function of an i^{th} second impedance unit is enabled, a level state of the i^{th} group of sub-signals in the second target signal according to the second calibration signal, so as to control a resistance value of the second impedance unit to be a standard resistance value; or, determine, in a case that the level pull-up function of the i^{th} second impedance unit is disabled, that the i^{th} group of sub-signals in the second target signal are in the first level state;

the third logic module is specifically configured to determine whether the level pull-up function of the at least one of the second impedance units is enabled according to the fifth impedance control signal; and determine, in the case that the level pull-down function of the

i^{th} second impedance unit is enabled, the level state of the i^{th} group of sub-signals in the third target signal according to the third calibration signal, so as to control the resistance value of the second impedance unit to be the standard resistance value; or, determine, in the case that the level pull-down function of the i^{th} second impedance unit is disabled, that the i^{th} group of sub-signals in the third target signal are in the second level state;

wherein each of the second impedance units comprises N third switch transistors, N fourth switch transistors and 2N second resistors, a control end of an n^{th} second switch transistor in the i^{th} third impedance unit is connected with an n^{th} sub-signal in the i^{th} group of sub-signals in the second target signal, a first end of one of the third switch transistors is connected with a first end of one of the second resistors, and a second end of one of the third switch transistors is connected with a power signal; a control end of an n^{th} fourth switch transistor in the i^{th} second impedance unit is connected with an n^{th} sub-signal in the i^{h} group of sub-signals in the third target signal, a first end of one of the fourth switch transistors is connected with a ground signal, a second end of one of the fourth switch transistors is connected with the first end of one of the second resistors, and second ends of the 2N second resistors are all connected with the DM.

21. The semiconductor memory according to any one of claims 15-20, wherein

the first level state is a high level state, and the second level state is a low level state;

both the first switch transistor and the third switch transistor are P-channel field effect transistors, and both the second switch transistor and the fourth switch transistor are N-channel field effect transistors;

a control end of each of the P-channel field effect transistors is a gate electrode, a second end of each of the P-channel field effect transistors is a source electrode, a first end of each of the P-channel field effect transistors is a drain electrode, a control end of each of the N-channel field effect transistors is the gate electrode, a second end of each of the N-channel field effect transistors is the drain electrode, and a first end of each of the N-channel field effect transistors is the source electrode; and

the standard resistance value is 240 ohms.

22. An electronic device, comprising the semiconductor memory according to any one of claims 9-21.