

ABSTRACT

INTEGRATED CIRCUIT HAVING ULTRALOW-K DIELECTRIC LAYER

A device layer is configured to reduce change in stress characteristics due to subsequent processing to reduce cracking of a subsequently formed layer. The change in stress characteristics can be reduced by providing a shield layer over the device layer to protect the device layer from exposure to subsequently processing, such as curing medium used to form voids in an ultralow-k dielectric layer.

Fig. 2