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Method for fabricating microstructures and arrangement of microstructures

The invention lies in the field of semiconductor technology and relates to a method for fabricating microstructures.

Advancing scaling of integrated circuits and the associated miniaturization and increasing complexity of the structures contained in the integrated circuits entail a multiplicity of problems.

Thus, by way of example, the interconnect resistances of the individual interconnects within the wiring planes increase. The capacitive coupling between the interconnects increases at the same time. Associated with this is an unfavorable rise in the RC time constants, which lead to rising signal propagation times, decreasing limiting frequencies, high power loss densities and crosstalk effects. The technical literature also groups these problems under the term "wiring crisis". In this respect, see, in particular, the technical articles by M.T. Bohr, "Interconnect Scaling - The Real Limiter to High Performance ULSI", IEDM 95, 241 - 244;
S. Oh and K. Chang, "2001 Needs for Multi-Level Interconnect Technology", Circuits & Devices, 1995, 16 - 20;
T.H. Ning, "0.1 µm Technology and BEOL", Mat. Res. Soc. Symp. Proc. Vol. 427, 1996, 17 - 21; and
K. Yamashita & S. Odanaka, "Interconnect Scaling Scenario using a Chip Level Interconnect Model", Symp. On VLSI Technology Digest of Technical Papers, 1997, 53 - 54.

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A further problem associated with miniaturization can be examined in the proximity effects of lithography (e.g. US 5,821,014) and etching technology. In the fabrication of integrated circuits, these effects lead to structural results which deviate from the desired structures prescribed on the lithography mask. In order to reduce or eliminate the proximity effects, it is necessary to resort to corrections (for example layout changes, US 6,083,275) of ever increasing complexity. The effects discussed are based on the fact that individual process steps of the overall patterning process (exposure, development, plasma etchings, chemical mechanical polishing, etc.) depend on the local structural characteristic features (packing density, distances from adjacent structures, center and edge positions). The required layout changes have to be determined for each new layout, with a high outlay, and taken into account by means of suitable measures on the corresponding masks.

In order to reduce the RC time constants, use is often made of interconnects having high conductivity (e.g. copper) and dielectrics having low dielectric constants ε_r (often also designated by k). Diverse organic dielectrics having dielectric constants of approximately 2.5 are used as "low-k dielectrics" (e.g. so-called aerogels or xerogels, US 6,277,728), but they are usually associated with diverse disadvantages (low thermal and chemical stability, hygroscopy, low blocking effect against the diffusion of e.g. copper, need to develop new deposition and patterning processes, new process installations). Porous inorganic dielectrics having even lower dielectric

constants (e.g. porous SiON) are not yet ready for production at the present time.

The best material with extremely low ε_r is vacuum or air ($\varepsilon_r = 1$). Therefore, a series of documents deal with techniques enabling the production of cavities between interconnects.

Thus, in accordance with US 6,252,290 B1, by way of example, after the completion of the interconnects, cavities are produced between the interconnects by subsequent removal of insulation material.

US 5,936,295, by contrast, exploits the porosity of a dielectric layer. After the completion of interconnect sections between which an auxiliary material is situated, said dielectric layer is applied to the interconnect sections and the auxiliary material. On account of the porosity of the dielectric layer, an etching substance can penetrate as far as the auxiliary material and remove the latter. As a result, cavities remain between the interconnect sections.

A similar approach is pursued by US 6,297,125 B1, but here a dielectric covering layer with subsequently introduced slots is used, through which the etching substance can penetrate as far as the auxiliary material.

In contrast thereto, in accordance with US 5,869,880, in each patterning plane (metalization and contact hole plane), the initially solid dielectric between the metal structures is finally patterned, thereby forming

comparatively small openings in the dielectric in comparison with the metal structures, which openings contribute to a reduction of the dielectric constants taking effect.

A further method for forming cavities between metal structures is disclosed in DE 199 57 302 A1, wherein the cavities can be produced in a self-aligned manner with respect to the metal structures.

The abovementioned methods have the disadvantage of a relatively high process complexity. Despite the cavities, capacitive couplings occur between the interconnects of different metalization planes on account of the dielectric layers (e.g. silicon oxide or silicon nitride) situated there. One possibility of reducing these capacitive couplings is afforded by the production of macroscopic cavity arrangements in these dielectric layers, i.e. in the contact hole plane, as is described for example in the German patent application - not a prior publication - DE 101 09 778.6 of 01.03.2001 from the same applicant and in US 6,869,880 already cited.

However, the fundamental problems going back to the proximity effects of lithography and etching technology are not avoided with the abovementioned methods.

Therefore, it is an object of the present invention to specify a method in which the effects of proximity effects are considerably reduced.

This object is achieved by means of a method in accordance with claim 1.

In this case, the method according to the invention for fabricating microstructures comprises the following steps:

a) formation of a regular arrangement of closed cavities in a patterning layer arranged on a substrate, the cavities being separated from one another by partitions;

b) opening of such cavities in which microstructures are intended to be produced;

c) removal of at least a portion of the partitions situated between adjacent opened cavities in order to form trenches extending over at least two cavities; and

d) introduction of a material into the trenches in order to fabricate the microstructures.

Accordingly, in accordance with the invention, firstly a regular arrangement of closed cavities is formed in a patterning layer. Regular structures can be fabricated with particularly high precision and accuracy in conjunction with a comparatively small extent. On account of the regularity, no local differences occur during the exposure and the etching. Therefore, local proximity effects are avoided particularly during a global regular patterning of the patterning layer. On the other hand, the regularity of the cavities also allows the imaging of cavities which are so small that they can no longer be imaged satisfactorily in the case of separate imaging. The individual cavities are separated from one another by

partitions comprising the material of the patterning layer.

In order to reliably ensure the regularity, the closed cavities are formed by microelectronic processes known per se (e.g. CVD, lithography, etching, CMP). It is preferably the case, therefore, that in order to form the cavities, depressions are produced in the patterning layer and are closed with a covering layer, thereby producing the cavities. In this case, the dimensions of the depressions or the cavities are of the order of magnitude of the microstructures to be produced. In particular, the minimum lateral extent of the microstructures to be produced is determined by the extent of the cavities.

Preferably, the cavities or the depressions etched into the patterning layer in order to form the cavities are defined lithographically and subsequently etched into the pattering layer. In this case, a resist mask may preferably be used for the lithographic definition of the cavities or the depressions, at least two regular strip patterns rotated through a predetermined angle relative to one another being successively imaged into said resist mask. In contrast to raster-shaped patterns, strip patterns can even be imaged with higher accuracy in conjunction with the same resolution. On the other hand, they also enable the imaging of more closely adjacent lines than is possible in the case of a raster-shaped pattern. The possibilities of lithography can be maximally utilized by means of the imaging of strip patterns.

During the imaging of regular strip patterns, at least two exposures are required, the strip pattern being rotated through a predetermined angle, e.g. 90°, between the individual exposures. In principle, it is also possible to image different (e.g. with a different line spacing) strip patterns rotated with respect to one another, in order, for example, to produce cavities that are rectangular in cross section.

It is favorable if,

- in order to form the patterning layer, at least a first and a second layer are successively applied to the substrate, the materials of the first and second layers being chosen so as to enable a deposition of the material of the covering layer on the second layer selectively with respect to the first layer,
- in order to form the cavities, the depressions are formed in the first and second layers, the depressions penetrating through the second layer completely and penetrating through the first layer at least partially, and, afterward, the material of the covering layer is deposited in such a way that it grows essentially only on the second layer,

since this enables the covering layer to be applied in a particularly simple and purposeful manner. Moreover, inadvertent filling of the depressions is reliably avoided. Accordingly, the materials for the first and second layers are selected so as to ensure a selective deposition of the covering layer on the second layer. The depressions are formed completely in the second layer and at least partly in the first layer. Preferably, the first

layer is likewise etched through completely. The residual material between the depressions forms the partitions. A third layer may be applied in addition to the first and second layers, the material of which third layer differs from the second layer, so that the material of the covering layer essentially likewise grows only on the second layer. Accordingly, no material of the covering layer grows on the first and third layers, even if, during the progressive growth of the material of the covering layer on the second layer, the third layer is possibly covered by said material. In the case of a three-layered construction of the patterning layer, the third layer preferably serves as a polishing stop during the subsequent polishing-back of the protruding material of the covering layer. In the case of a two-layered construction, by contrast, the second layer preferably performs this function.

The first, second and third layers are preferably dielectric layers, since, for dielectric layers, it is possible to have recourse to a multiplicity of suitable and proven patterning methods, in particular anisotropic plasma etching methods.

The use of silicon nitride for the first and third layers is particularly favorable. By contrast, a silane-based silicon oxide deposited in plasma-enhanced fashion is preferably used for the second layer. Given this choice of materials for the first, second and third layers, an oxide can be deposited selectively on the second layer by means of O_3/TEOS deposition. Therefore, an oxide of this type is preferably used for the covering layer.

In order to reliably ensure the formation of the cavities, the first layer is preferably made about 4 to 5 times thicker than the second layer.

Afterward, those cavities in which the microstructures to be fabricated are intended to be formed are opened at their top side preferably by methods of lithography and etching technology. To that end, a mask (photomask / resist mask) is applied to the covering layer, leaving uncovered the cavities that are to be opened. The material of the covering layer is expediently etched selectively with respect to the material of the first, second and third layers, and the material of the mask. As a result, even in the event of a possible misalignment of this mask with regard to the cavities, the side walls of the cavities are not etched, so that the position and extent of the cavities are preserved. The mask (for example the strip masks) used for forming the cavities (or the depressions) is, accordingly, the actual patterning mask, whereas the mask for opening the cavities performs the function of a selection mask. Therefore, less stringent requirements can be made of the mask for opening the cavities than of the mask for defining the cavities.

At least a portion of the microstructures is intended to extend over a plurality of opened cavities. This requires the removal of the webs or partitions of the patterning layer which are situated between said opened cavities. In this case, recourse is preferably had to the same mask (selection mask) which has already been used for opening the closed cavities. Through the removal of the webs or

the partitions, adjacent cavities that are initially separated from one another are combined to form individual trenches running in the patterning layer. The fabrication of the microstructures is concluded by filling the opened cavities or the trenches with the material of the microstructures to be fabricated and, if appropriate, polishing-back (for example by means of CMP).

It lies within the scope of the invention to fabricate by the method according to the invention exclusively those microstructures which extend over at least two cavities, and, in addition thereto, to fabricate those microstructures which only fill individual opened cavities. In the latter case, in addition to the trenches, individual opened cavities are also filled with the material of microstructures in order to form said microstructures.

The cavities have a lateral extent prescribed in particular by the lithography used (masks). In this case, in the context of the invention, lateral extent is understood to mean that which extends in the plane of the patterning layer. In the simplest case, the cavities have a square or approximately square cross section in a plan view of the patterning layer, deviations from the square cross section being caused in particular as a result of the imperfection during the lithographic imaging. If the microstructures to be fabricated are formed in a trench encompassing two adjacent cavities, their lateral extent at least in one direction amounts to at least twice the lateral extent of the cavities in this direction.

The method according to the invention may also be referred to as a "cellular damascene method". The basic concept is fabricating the microstructures by selecting individual cavities and, if appropriate, combining a plurality of cavities. Each cavity forms one cell in this case. In this case, the arrangement and the course of the microstructures to be fabricated depend on the raster-shaped arrangement of the cells. The latter may be made square, for example, and be arranged in rows and lines. Other arrangements are likewise possible.

The microstructures to be fabricated can ultimately be any desired microstructures, i.e. both microelectronic and micromechanical structures. The type of microstructures to be fabricated also decides the material with which the uncovered cavities or the trenches are filled. The material may be e.g. metals, insulators, semiconductors, ferroelectrics etc. The fabrication of interconnects is particularly preferred, so that the material to be introduced is, in particular, metals and/or metal alloys, and particularly preferably copper.

The method according to the invention also at the same time alleviates the problem of capacitive coupling in particular between interconnects, since, through selection of the cavities to be opened, the interconnects can be placed such that closed cavities remain between adjacent interconnects. Since the dielectric constant ε_r of said cavities amounts to 1, the dielectric constants taking effect between the adjacent interconnects is correspondingly reduced.

The advantages that can be achieved with the method according to the invention can be summarized in particular as follows:

- The regular arrangement of the cavities gives rise to microstructures which do not depend on proximity effects. The line widths and lengths are equal to the cell width or a multiple thereof if appropriate plus the web width.
- Steepness and accuracy of the microstructures are determined, independently of the material to be introduced, essentially by the cavity side walls, that is to say primarily by patterning methods used to form the depressions or cavities, in particular tried and tested anisotropic plasma etchings of dielectrics (silicon oxide, silicon nitride). The side walls can therefore be steep and smooth for all materials of the microstructures to be fabricated.
- The distance between the microstructures is determined by the web width of the cells alone or by the web width and the cavity width.
- Complex proximity corrections are obviated owing to the regular arrangement of the cells. Length and width of the resulting microstructures are an integer multiple of the cell size plus the width of the partitions originally situated between the combined cells. If the cells are rectangular, the length and the width of the microstructures in each case amount to the integer multiple of the lateral extent of the cells in the corresponding direction.
- Cavities between the interconnects make it possible to reduce the capacitive couplings between the

interconnects and thus generally capacitive couplings and signal delays.

- It is possible to have recourse to all the advantages of the damascene method, e.g. patterning of materials that cannot be etched or are difficult to etch.

The size of the microstructures is preferably in the micrometers range, i.e. 1 - 1000 µm, or less (< 1 µm). The method is preferably used in the fabrication of integrated circuits.

The invention furthermore relates to an arrangement of microstructures having a patterning layer in which a multiplicity of closed cavities and a multiplicity of microstructures are arranged, the closed cavities being seated on grid points of a predetermined raster and the microstructures running along the connecting lines that connect the grid points, and the closed cavities having a given lateral extent in at least one direction and the lateral extent of the microstructures in this direction corresponding to at least twice the lateral extent of the cavities.

In the arrangement according to the invention, the orientation and the position of the individual microstructures are prescribed by the raster of the cavities. Wherever microstructures are situated, there were originally cavities present. Combining at least two adjacent cavities, i.e. removing the partitions or webs situated between said cavities, has resulted in a continuous trench filled with the material of the microstructures. The partitions running between adjacent

cavities and between cavities and microstructures adjacent thereto preferably have the same thickness, the partitions running parallel to the connecting lines and in a manner offset uniformly with respect thereto.

The closed cavities preferably have a given lateral extent, so that the length of the microstructures corresponds to at least twice the extent of the cavities, if appropriate plus the width of the partition originally present between the adjacent cavities. The minimum extent of the microstructures preferably corresponds to the extent of the cavities.

It is furthermore preferred for the grid points to have a distance D along a first direction and the closed cavities to have a lateral extent B along said direction, where the length of the microstructures is n * D + B and n is natural number (n>0). If n = 1, by way of example, the microstructure extends over two adjacent cavities. It lies within the scope of the invention that the grid points may have a different distance D_1 and D_2 and a different lateral extent B_1 and B_2 in a different direction, e.g. perpendicularly to one another. This may be the case e.g. with cavities having a rectangular cross section in a plan view of the patterning layer. The microstructures then have an extent of n * D_1 + B_1 and m * D_2 + B_2 in the respective direction, where m and n are natural numbers and at least one of these two numbers is greater than 0. By way of example, it may be that m = 0, and n > 0. In this case, the width of the microstructures corresponds to the lateral extent B_2 and the length corresponds to a multiple of D_1 plus B_1. The microstructures can assume

practically any desired form within the raster prescribed by the cavities. Strip-shaped, areal and angular forms shall be mentioned here as examples. The cavities preferably have a square cross section in a plan view of the patterning layer, so that $D_1 = D_2 = D$ and $B_1 = B_2 = B$ hold true.

Preferably, the patterning layer comprises at least a first and a second layer made of different material, said second layer lying on said first layer, and the cavities run at least in the first layer and the microstructures run at least in both layers. A covering layer closing the cavities is preferably arranged in the plane of the second layer, so that the cavities essentially extend below the second layer, i.e. essentially within the first layer. By contrast, the microstructures preferably penetrated through both the first and the second layer, and preferably terminate with the upper edge of the second layer. If the patterning layer is even provided with at least three layers, the microstructures extend over all three layers. The cavities can be formed completely or only partly in the first layer, i.e. they did not completely penetrate through the first layer on the side remote from the second layer.

Preferably, the material of the first layer is silicon nitride and the material of the second layer is silicon oxide. The microstructures preferably constitute interconnects, in which case they comprise, in particular, a metal or a metal alloy, and particularly preferably copper.

The covering layer closing the cavities is preferably grown selectively on the material of the second layer.

The arrangement according to the invention preferably involves microstructures and in particular interconnects of an integrated circuit.

The invention is described below on the basis of exemplary embodiments and is illustrated in figures, in which:

figure 1 shows individual fabrication steps of one exemplary embodiment of the method according to the invention;

figure 2 shows individual fabrication steps of a further exemplary embodiment of the method according to the invention;

figure 3 shows an SEM photograph of the deposition of oxide on silane PE-CVD oxide; and

figure 4 shows the exposure of a resist mask with two strip patterns rotated through 90°.

Figure 1 shows an embodiment of the "cellular damascene method", in which the microstructures to be fabricated are separated from one another by cavities. The cavity pattern produced in this case extends over the entire surface of a chip to be fabricated or at least over the majority of its area.

Illustration (a) of figure 1 shows a substrate S, on which three dielectric layers S1, S2 and S3 have been successively deposited. At least the material of the second layer S2 differs from the material of the first layer S1 and of the third layer S3. By way of example, the first and third layers S1 and S3 may comprise silicon nitride and the second layer S2 may comprise silicon oxide which has been formed by means of a plasma-enhanced deposition from a silane atmosphere. In this case, the first layer S1 performs the function of a carrier layer and defines the height of the cavities that are subsequently to be formed. For this reason, this layer has a thickness that is about 4 to 5 times higher than the second layer S2, for example. The latter serves as carrier material on which the covering layer for closing the cavities subsequently grows selectively. In order to ensure the selectivity during the deposition of the material of the covering layer, the materials of the layers S1 to S3 must be chosen accordingly. The third layer S3 in turn serves as a polishing stop for a polishing step that is subsequently to be carried out. The entire thickness of this multilayer approximately corresponds to the desired height of the microstructures to be produced. The three layers S1 to S3 together form the patterning layer 2.

Lithography and etching are carried out to produce a grid pattern for forming the depressions 6 in the patterning layer 2, a resist mask that is not illustrated being used. The width of the grid webs or the partitions 4 is chosen to be as small as possible, a lower limiting factor being the required mechanical stability for the subsequent

process steps. The accuracy with which the mask for opening the cavities and removing the partitions can be aligned with respect to the cavity raster is also a limiting factor. By way of example, the overlay accuracy currently achieved in mass production is about 15 nm. It is expected that this accuracy will be improved in the future. The width of the partitions should therefore be greater than the overlay accuracy that can respectively be achieved.

All lithography methods, e.g. optical lithography, electron or ion beam projection lithography or EUV lithography, can be used for fabricating the depressions 6. For the case where one of the lithography methods would not produce depressions with sharp angles owing to inadequate resolution, two regular strip patterns rotated through 90 degrees relative to one another can be successively imaged into the resist mask. The exposure with two strip patterns rotated through 90° with respect to one another is illustrated in more detail in connection with figure 4.

The plan view of the structure thus obtained is shown in illustration (b') of figure 1, the associated illustration (b) showing a cross section along the line identified by an arrow. In all the subsequent illustrations of figure 1, the illustrations respectively identified by an apostrophe (') show the plan view, while the associated illustrations without an apostrophe show the cross section along the line indicated by the arrows.

In a further method step, the material of the covering layer S4 is deposited selectively on the second layer S2. Owing to the selectivity of this deposition, the material of the covering layer S4 grows neither on the first nor on the third layer. The time duration for this deposition is chosen such that the depressions 6 are reliably closed by lateral growth of the material of the covering layer S4, so that terminated cavities H are produced and the upper edge of the deposited covering layer S4 at least reaches the upper edge of the third layer S3. An intermediate stage of the deposition of the covering layer S4 with depressions that have already been partly closed is shown in illustrations (c1) and (c1') of figure 1, while the illustrations (c2) and (c2') represent the end stage. The cavities H thus produced form the individual cells which determine the extent and the course of the microstructures to be fabricated. The regular arrangement of the cavities H defines a grid at whose grid points the cavities are arranged. The microstrucures that are subsequently to be formed in the cavities are therefore likewise oriented to this grid and run along the connecting lines that connect the grid points.

In the case of the materials specified above for the layers S1 to S3, the material chosen for the covering layer S4 is silicon oxide, which grows only on the second layer S2 as a result of an ozone-enhanced TEOS (tetraethyl orthosilicate) deposition.

The material of the covering layer S4 which projects above the third layer S3 is removed by means of chemical mechanical polishing (CMP), it being possible to set the

CMP step in such a way that it stops reliably on the third layer S3 (illustration (d) of figure 1).

A further lithography step defines those cavities H' which are intended to be opened by means of a subsequent etching step. To that end, a resist mask PR is applied to the polished surface of the covering layer S4 and of the third layer S3, exposed and developed. This method stage is shown in illustrations (e) and (e') of figure 1. During the exposure of the resist mask PR, it should be taken into consideration that the width and length of the openings to be formed in the resist mask PR are chosen such that the latter, with the inclusion of the overlay alignment accuracy, do not project beyond the partitions 4 delimiting the individual cavities H, H'. However, they can also be chosen to be smaller as long as the conformity of the subsequent deposition process for filling the opened cavities H' is ensured.

A subsequent etching process opens the covering layer S4 above the selected cavities H' and, in the process, uncovers firstly the surface of the third layer S3 and finally the surface of the first layer S1 of the partitions 4 situated between opened cavities H'. It is also possible to carry out the etching in such a way that the second and third layers on the partitions 4 are initially not removed. As a result, even in the event of possible misalignment of the resist mask PR with respect to the side walls of the cavities H, H', it is possible to achieve opening of the cavities H' without removal of partitions. The structure thus obtained is shown in illustrations (f) and (f') of figure 1, in illustration

(f') the partitions 4 between uncovered cavities H' already having been removed down to the first layer S1.

By means of an anisotropic plasma etching step, the residual partitions, only comprising the material of the first layer S1, between uncovered cavities H' are removed using the resist mask PR. Combining a plurality of opened cavities H' produces trenches 8 in the patterning layer 2 (illustrations (g) and (g') of figure 1).

The trenches 6 and/or holes defined by the resist mask PR are then filled with the material M of the microstructures to be formed and protruding material is removed by means of a CMP step. To that end, sputtering, vapor deposition, CVD, electrochemical deposition methods or combinations thereof are used depending on the material M. The material M may be, by way of example, copper for forming interconnects. The method steps specifically required for the deposition and planarization of copper are described for example in DE 199 57 302 A1 already cited, the disclosure content of which is hereby incorporated in its entirety. The state after the concluding CMP step with the completed microstructures M (here interconnects) is shown in illustrations (h) and (h') of figure 1.

If, instead of the triple layer comprising first, second and third layers S1 to S3, only a double layer (S1 and S2) has been used or the third layer S3 has been removed again during the concluding CMP step, the result is the end state shown in illustrations (i) and (i') of figure 1.

In the case of the exemplary embodiment described above, the microstructures produced (here interconnects) were fabricated in such a way that they are separated from one another by cavities. The low dielectric constant $\varepsilon_r = 1$ of air or vacuum correspondingly reduces the dielectric constant taking effect, so that the RC time constants are reduced.

If the geometrical midpoints of the cavities (cells) are regarded as grid points and the distance between adjacent cells is designated by D and the extent of an (essentially square) cavity is designated by B, then the microstructures M have a length of n * D + B, where n is a natural number (n > 0), i.e. the microstructures extend at least over two cavities. In the simplest case, the width of the microstructures corresponds to the lateral extent of a cavity. It goes without saying that the width of the microstructures may likewise extend over a plurality of cavities, so that m * D + B, where n is a natural number, holds true for the width in the case of essentially square cavities.

With reference to figure 2, the basic process sequence for the "cellular damascene method" is outlined for the case where the microstructures produced are not generally separated from one another by cavities.

Proceeding from the layer construction shown in illustrations (a) and (a') of figure 1, lithography and etching are carried out analogously to the description relating to the above illustrations (b) and (b') of figure 1 to produce a grid pattern (illustrations (a) and (a') of

figure 2). In this case, however, the width of the partitions has been set equal to the width of the etched depressions 6.

In the same way as in figure 1, figure 2 illustrates mutually assigned plan views and cross sections along the lines indicated by arrows in the plan views.
Using processes identical to those described in connection with figure 1, the depressions 6 are closed with the covering layer S4 and planarized, in this case the CMP step stopping on the second layer S2. The structure thus obtained is shown in illustrations (b) and (b').

After further process steps, likewise described in connection with figure 1, those cavities H' in which the microstructures (here interconnects and/or contact holes) are intended to be produced are defined lithographically and opened by etching. Afterward, the uncovered partitions or webs 4 between the opened cavities (cells) H' are removed and the resulting trenches are filled with the material M of the microstructures to be fabricated. The protruding material M is removed by means of a CMP step. During the lithography for the selection of the cavities H' to be opened, account was taken of the fact that adjacent microstructures are generally closely adjacent and are separated from one another only by partitions and not additionally by cavities. Cavities between adjacent interconnects can be dispensed with particularly when the material of the first layer S1 is a "low-k dielectric". Requirements similar to those mentioned above in connection with illustrations (e) and (e') of figure 1 apply to the lithography step. However, they are more

relaxed owing to the wider webs or partitions in comparison with figure 1. The structure obtained after the concluding planarizing step (CMP) for removing excess material M, with the completed microstructures M (here interconnects), is shown in illustrations (c) and (c') of figure 2.

It goes without saying that the exemplary embodiments described above can readily be combined with one another.

Figure 3 shows a cross section through an SEM photograph (scanning electron microscope) through a cavity produced by selective ozone-enhanced TEOS deposition of the fourth layer S4 (ozone-TEOS oxide) on PE-CVD (plasma-enhanced CVD) silane oxide of the second layer S2. By contrast, no material of the fourth layer has been deposited on the first layer S1 comprising silicon nitride (Si_3N_4). The covering of the upper edge of the first layer S1 is caused by the ozone-TEOS oxide growing on all sides on the second layer S2.

Figure 4 shows two identical strip patterns 10 and 12 rotated through 90°, which are successively imaged into the resist mask 14 used for defining the depressions or cavities.

List of reference symbols

S	Substrate
S1	First layer
S2	Second layer
S3	Third layer
S4	Covering layer
H, H'	Cavities
PR	Resist mask
M	Microstructures / material of the microstructures
2	Patterning layer
4	Partitions / webs
6	Depressions
8	Trenches
10, 12	Strip patterns
14	Resist mask

Patent Claims

1. A method for fabricating microstructures having the following steps:

a) formation of a regular arrangement of closed cavities (H) in a patterning layer (2, S1, S2, S3) arranged on a substrate (S), the cavities (H) being separated from one another by partitions (4);

b) opening of such cavities (H') in which microstructures (M) are intended to be produced;

c) removal of at least a portion of the partitions (4) situated between adjacent opened cavities (H') in order to form trenches (8) extending over at least two cavities (H'); and

d) introduction of a material (M) into the trenches (8) in order to fabricate the microstructures (M).

2. The method as claimed in claim 1, wherein,
in order to form the cavities (H), depressions (6) are produced in the patterning layer (2, S1, S2, S3) and are closed with a covering layer (S4), thereby producing the cavities (H).

3. The method as claimed in claim 2, wherein,

- in order to form the patterning layer (2, S1, S2, S3), at least a first and a second layer (S1, S2) are successively applied to the substrate (S), the materials (M) of the first and second layers (S1, S2) being chosen so as to enable a deposition of the material

of the covering layer (S4) on the second layer (S2) selectively with respect to the first layer (S1),

- in order to form the cavities (H, H'), the depressions (6) are formed in the first and second layers (S1, S2), the depressions (6) penetrating through the second layer (S2) completely and penetrating through the first layer (S1) at least partially, and
- afterward, the material of the covering layer (S4) is deposited in such a way that it grows essentially only on the second layer (S2).

4. The method as claimed in one of claims 1 to 3, wherein
the cavities (H, H') or the depressions (6) are defined lithographically and subsequently etched into the pattering layer (2, S1, S2, S3).

5. The method as claimed in claim 4, wherein
a resist mask (14) is used for the lithographic definition of the cavities (H, H') or the depressions (6), at least two regular strip patterns (10, 12) rotated through a predetermined angle relative to one another being successively imaged into said resist mask.

6. The method as claimed in claim 5, wherein
the predetermined angle is 90°.

7. The method as claimed in one of claims 3 to 6, wherein,

in order to form the patterning layer (2, S1, S2, S3), a third layer (S3) is applied in addition to the first and second layers (S1, S2), the material of which third layer differs from the second layer (S2), so that the material of the covering layer (S4) essentially grows only on the second layer (S2).

8. The method as claimed in one of claims 3 to 7, wherein
the material of the covering layer (S4) is polished back as far as the third or as far as the second layer, the third or the second layer respectively acting as a polishing stop.

9. The method as claimed in one of claims 3 to 8, wherein
the first, second and third layers (S1, S2, S3) are dielectric layers.

10. The method as claimed in one of claims 3 to 9, wherein
the material of the first and third layers (S1, S3) is silicon nitride, the material of the second layer (S2) is silane-based silicon oxide deposited in plasma-enhanced fashion, and the material of the covering layer (S4) is an oxide fabricated by means of O_3/TEOS deposition.

11. The method as claimed in one of claims 3 to 10, wherein
the first layer (S1) is about 4 to 5 times thicker than the second (S2) layer.

12. The method as claimed in one of the preceding claims, wherein,
in addition to the trenches (8), individual opened cavities (H') are also filled with the material of microstructures in order to form said microstructures.

13. The method as claimed in one of the preceding claims, wherein,
in order to open the cavities (H') and in order to remove the partitions (4), a mask (PR) is applied to the covering layer (S4).

14. The method as claimed in one of the preceding claims, wherein
the material of the microstructures (M) to be formed is introduced into the opened cavities (H') and protruding material is polished back.

15. The method as claimed in one of the preceding claims, wherein
the material of the microstructures (M) to be formed is metal and/or metal alloys and, in particular, copper.

16. The method as claimed in one of the preceding claims, wherein
the microstructures (M) to be fabricated are interconnects.

17. An arrangement of microstructures
having a patterning layer (2, S1, S2, S3), in which a multiplicity of closed cavities (H) and a multiplicity of microstructures (M) are arranged, the closed cavities (H)

being seated on grid points of a predetermined raster and the microstructures (M) running along the connecting lines that connect the grid points, and the closed cavities (H) having a given lateral extent in at least one direction and the lateral extent of the microstructures (M) in this direction corresponding to at least twice the lateral extent of the cavities (H).

18. The arrangement as claimed in claim 17, wherein
partitions (4) of identical thickness are arranged between adjacent cavities (H) and between cavities (H) and microstructures (M) adjacent thereto.

19. The arrangement as claimed in claim 17 or 18, wherein
the grid points have a distance D, the lateral extent of the closed cavities (H) is B, and the lateral extent of the microstructures is n*D + B, where n is a natural number.

20. The arrangement as claimed in one of claims 17 to 19, wherein
the patterning layer (2, S1, S2, S3) comprises at least a first and a second layer (S1, S2) made of different material, said second layer lying on said first layer, and the cavities (H) run at least in the first layer (S1) and the microstructures (M) run at least in both layers (S1, S2).

21. The arrangement as claimed in claim 20, wherein

the material of the first layer (S1) is silicon nitride and the material of the second layer (S2) is silicon oxide.

22. The arrangement as claimed in one of claims 17 to 21, wherein
the microstructures (M) are interconnects.

23. The arrangement as claimed in one of claims 17 to 22, wherein
the microstructures (M) comprise a metal or a metal alloy and, in particular, copper.

24. The arrangement as claimed in one of claims 17 to 23, wherein
the cavities (H) are closed with a covering layer (S4) grown selectively on the material of the second layer (S2).