WHAT IS CLAIMED IS:

1. A compound semiconductor substrate comprising:

a Si substrate with O concentration of $3*10^{17}/cm^3$ or more and $3*10^{18}/cm^3$ or less,

a SiC layer formed on the Si substrate,

a first nitride semiconductor layer made of $Al_xGa_{1-x}N$ ($0.1 \leqq x \leqq 1$), formed on the SiC layer and including an insulating or semi-insulating layer,

a second nitride semiconductor layer formed on the first nitride semiconductor layer and including a main layer comprising of insulating or semi-insulating $Al_yGa_{1-y}N$ ($0 \leqq y < 0.1$),

an electronic traveling layer formed on the second nitride semiconductor layer and made of $Al_zGa_{1-z}N$ ($0 \leqq z < 0.1$), and

a barrier layer formed on the electronic traveling layer and having a wider band gap than a band gap of the electronic traveling layer, wherein

a sum total thickness of the first and second nitride semiconductor layers and the electronic traveling layer is 6 micrometers or more and 10 micrometers or less,

the first nitride semiconductor layer includes at least one of a first region made of $Al_xGa_{1-x}N$ ($0.4 < x \leqq 1$) and a second region made of $Al_xGa_{1-x}N$ ($0.1 \leqq x \leqq 0.4$) having a thickness of 0.5 micrometer or more,

the first region has Si concentration of 0 atoms/cm^3 or more and $5*10^{17}$ atoms/cm^3 or less, O concentration of 0 atoms/cm^3 or more and $5*10^{17}$ atoms/cm^3 or less, and Mg concentration of 0 atoms/cm^3 or more and $5*10^{17}$ atoms/cm^3 or less,

the second region has Si concentration of 0 atoms/cm^3 or more and $2*10^{16}$ atoms/cm^3 or less, O concentration of 0 atoms/cm^3 or more and $2*10^{16}$ atoms/cm^3 or less, and Mg concentration of 0 atoms/cm^3 or more and $2*10^{16}$ atoms/cm^3 or less,

at least one of C concentration and Fe concentration in the second region is higher than any of Si concentration, O concentration, and Mg concentration in the second region, and $5*10^{19}$ atoms/cm^3 or less,

the main layer has Si concentration of 0 atoms/cm^3 or more and $2*10^{16}$ atoms/cm^3 or less, O concentration of 0 atoms/cm^3 or more and $2*10^{16}$ atoms/cm^3 or less, and Mg concentration of 0 atoms/cm^3 or more and $2*10^{16}$ atoms/cm^3 or less,

at least one of C concentration and the Fe concentration in the second nitride semiconductor layer is higher than any of Si concentration, O concentration, and Mg concentration in the second nitride semiconductor layer and is $5*10^{19}$ atoms/cm^3 or less,

the main layer includes a region where concentration of activated donor ions is 0 atoms/cm^3 or more and $2*10^{14}$ atoms/cm^3 or less, and

the electronic traveling layer has Si concentration of 0 atoms/cm^3 or more and $1*10^{16}$ atoms/cm^3 or less, O concentration of 0 atoms/cm^3 or more and $1*10^{16}$ atoms/cm^3 or less, and Mg concentration of 0 atoms/cm^3 or more and $1*10^{16}$ atoms/cm^3 or less, C concentration of 0 atoms/cm^3 or more and $1*10^{17}$ atoms/cm^3 or less, and Fe concentration of 0 atoms/cm^3 or more and $1*10^{17}$ atoms/cm^3 or less.

2. The compound semiconductor substrate according to claim 1, wherein

the second nitride semiconductor layer further includes one or more intermediate layer formed at least one of inside of the main layer and on the main layer, the intermediate layer comprising of $Al_yGa_{1-y}N$ ($0.5 \leqq y \leqq 1$), and

the main layer has at least one of C concentration higher than that of the electronic traveling layer and Fe concentration higher than that of the electronic traveling layer.

3. The compound semiconductor substrate according to claim 2, wherein

the intermediate layer is two or more layers, and each of the two or more intermediate layers has a thickness of 10 nanometers or more and 30 nanometers or less, and is formed at intervals of 0.5 micrometers or more and 10 micrometers or less.

4. The compound semiconductor substrate according to claim 1, wherein

the Si substrate contains B, and has p type conductivity and a resistivity of 0.1 mΩcm or more and 100 mΩcm or less.

5. The compound semiconductor substrate according to claim 1, wherein

the SiC layer has a thickness of 0.5 micrometers or more and 2 micrometers or less.

6. The compound semiconductor substrate according to claim 1, wherein

the first nitride semiconductor layer includes both the first region and the second region, and

a distance between the first region and the SiC layer is less than a distance between the second region and the SiC layer.

7. The compound semiconductor substrate according to claim 1, wherein

the first nitride semiconductor layer has a thickness less than or equal to a thickness of the second nitride semiconductor layer.

8. The compound semiconductor substrate according to claim 1, wherein

the electronic traveling layer has a thickness of 0.3micrometers or more.

9. The compound semiconductor substrate according to claim 1, wherein

stipulating a least squares plane of a top surface of the compound semiconductor substrate, when a sum total value of distance from the least squares plane to a highest point of the top surface of the compound semiconductor substrate and distance from the least squares plane to a lowest point of the top surface of the compound semiconductor substrate is defined as a warpage amount, the warpage amount is 0 or more and 50 or less micrometers.

10. The compound semiconductor substrate according to claim 1, wherein

regions other than an area where a distance from an outer edge of a top surface of the compound semiconductor substrate is 5 millimeters or less do not contain cracks.

11. The compound semiconductor substrate according to claim 1, wherein

the compound semiconductor substrate has a disk shape and a diameter of 100 millimeters or more and 200 millimeters or less.

12. The compound semiconductor substrate according to claim 1, wherein

a top surface of the compound semiconductor substrate does not contain traces of meltback etching.

13. A compound semiconductor device comprising:

the compound semiconductor substrate according to claim 1,

first and second electrodes formed on the barrier layer, and

a third electrode which is formed on the barrier layer and controls current flowing between the first electrode and the second electrode according to applied voltage.