

CMOS INVERTERS CONFIGURED USING MULTIPLE-GATE TRANSISTORS

ABSTRACT OF THE DISCLOSURE

0056 An inverter that includes a first multiple-gate transistor including a source connected to a power supply, a drain connected to an output terminal, and a gate electrode; a second multiple-gate transistor including a source connected to a ground, a drain connected to the output terminal, and a gate electrode; and an input terminal connected to the gate electrodes of the first and second multiple-gate transistors. Each of the first and second multiple-gate transistors may further include a semiconductor fin formed vertically on an insulating layer on top of a substrate, a gate dielectric layer overlying the semiconductor fin, and a gate electrode wrapping around the semiconductor fin separating the source and drain regions.

FIG. 7