ABSTRACT

A method of operating a memory device includes receiving, from a memory controller, an operation command that is synchronized with a clock signal, receiving a data clock signal having a full-rate frequency and a synchronization pattern provided by at least one of a plurality of data signals. The clock signal and the data clock signal are then synchronized using a synchronization operation based on the synchronization pattern. The data clock signal may be received after a first delay time passes from a time point at which the operation command is received. The first delay time is a delay time necessary to prepare the synchronization operation.

FIG. 7