What is claimed is:

1. An electronic device comprising a semiconductor memory, wherein the semiconductor memory comprises:

a substrate including a first portion in a first region and a second portion in a second region;

a plurality of memory cells disposed over the first portion of the substrate;

a first insulating layer extending over the second portion of the substrate and at least partially filling a space between adjacent ones of the plurality of memory cells;

a second insulating layer disposed over the first insulating layer; and

a contact plug penetrating the second insulating layer and the first insulating layer in the second region,

wherein the first insulating layer has a dielectric constant smaller than that of the second insulating layer, a thermal conductivity smaller than that of the second insulating layer, or both, and

wherein a width of a first portion of the contact plug that penetrates the first insulating layer is larger than a width of a second portion of the contact plug that penetrates the second insulating layer.

2. The electronic device according to claim 1, wherein a thickness of the first insulating layer in the second region is smaller than that of the first insulating layer in the first region.

3. The electronic device according to claim 1, wherein a thickness of the first insulating layer in the second region is smaller than a thickness of the second insulating layer.

4. The electronic device according to claim 1, wherein the first insulating layer has an etching rate higher than that of the second insulating layer.

5. The electronic device according to claim 1, wherein the first insulating layer includes silicon and carbon, and wherein the second insulating layer includes silicon oxide.

6. The electronic device according to claim 5, wherein the first insulating layer includes SiOC, SIOCH, SiOCHN, SiC, SiCON, or SiCN.

7. The electronic device according to claim 1, wherein each of the plurality of memory cells includes a phase change material.

8. The electronic device according to claim 1, further comprising a microprocessor which includes:

a control unit configured to receive a signal including a command from an outside of the microprocessor, and performs extracting, decoding of the command, or controlling input or output of a signal of the microprocessor;

an operation unit configured to perform an operation based on a result that the control unit decodes the command; and

a memory unit configured to store data for performing the operation, data corresponding to a result of performing the operation, or an address of data for which the operation is performed,

wherein the semiconductor memory is part of the memory unit in the microprocessor.

9. The electronic device according to claim 1, further comprising a processor which includes:

a core unit configured to perform, based on a command inputted from an outside of the processor, an operation corresponding to the command, by using data;

a cache memory unit configured to store data for performing the operation, data corresponding to a result of performing the operation, or an address of data for which the operation is performed; and

a bus interface connected between the core unit and the cache memory unit, and configured to transmit data between the core unit and the cache memory unit,

wherein the semiconductor memory is part of the cache memory unit in the processor.

10. The electronic device according to claim 1, further comprising a processing system which includes:

a processor configured to decode a command received by the processor and control an operation for information based on a result of decoding the command;

an auxiliary memory device configured to store a program for decoding the command and the information;

a main memory device configured to call and store the program and the information from the auxiliary memory device such that the processor can perform the operation using the program and the information when executing the program; and

an interface device configured to perform communication between at least one of the processor, the auxiliary memory device and the main memory device and the outside,

wherein the semiconductor memory is part of the auxiliary memory device or the main memory device in the processing system.

11. The electronic device according to claim 1, further comprising a data storage system which includes:

a storage device configured to store data and conserve stored data regardless of power supply;

a controller configured to control input and output of data to and from the storage device according to a command inputted from an outside;

a temporary storage device configured to temporarily store data exchanged between the storage device and the outside; and

an interface configured to perform communication between at least one of the storage device, the controller and the temporary storage device and the outside,

wherein the semiconductor memory is part of the storage device or the temporary storage device in the data storage system.

12. The electronic device according to claim 1, further comprising a memory system which includes:

a memory configured to store data and conserve stored data regardless of power supply;

a memory controller configured to control input and output of data to and from the memory according to a command inputted from an outside;

a buffer memory configured to buffer data exchanged between the memory and the outside; and

an interface configured to perform communication between at least one of the memory, the memory controller and the buffer memory and the outside,

wherein the semiconductor memory is part of the memory or the buffer memory in the memory system.

13. A method for fabricating an electronic device including a semiconductor memory, the method comprising:

providing a substrate that includes a first portion in a first region and a second portion in a second region;

forming a first insulating layer which extends over the second portion of the substrate and at least partially fills a space between adjacent ones of a plurality of memory cells;

forming a second insulating layer over the first insulating layer;

performing a planarization process until upper surfaces of the plurality of memory cells are exposed;

forming a contact hole by etching the second insulating layer and the first insulating layer in the second region; and

forming a contact plug by filling the contact hole with a conductive material,

wherein the first insulating layer has a dielectric constant smaller than that of the second insulating layer, a thermal conductivity smaller than that of the second insulating layer, or both,

wherein an etching rate of the first insulating layer is higher than an etching rate of the second insulating layer, and

wherein a width of a first portion of the contact hole that penetrates the first insulating layer is larger than a width of a second portion of the contact hole that penetrates the second insulating layer.

14. The method according to claim 13,

wherein the plurality of memory cells including a plurality of variable resistance layers, respectively, and

wherein forming the first insulating layer includes:

adjusting a thickness of the first insulating layer in the second region to a given value or less while filling at least a part of a space between adjacent ones of the plurality of variable resistance layers.

15. The method according to claim 13, wherein the first insulating layer includes silicon and carbon, and wherein the second insulating layer includes silicon oxide.

16. The method according to claim 13, wherein the first insulating layer includes SiOC, SIOCH, SiOCHN, SiC, SiCON, or SiCN.