~~What is claimed is:~~

CLAIMS

1. A method for forming a semiconductor device comprising:

providing a substrate prepared with a dielectric layer formed thereon;

forming a first upper etch stop layer on the dielectric layer, the first upper etch stop layer comprising a first material;

patterning the dielectric layer and first upper etch stop layer to form an interconnect opening;

filling the interconnect opening with a conductive material to form an interconnect, the interconnect and first upper etch stop layer having coplanar top surfaces; and

forming a second upper etch stop layer over the coplanar top surfaces, wherein the second upper etch stop layer comprises a second material having sufficient adhesion with the first material to reduce diffusion of the conductive material.

2. The method of claim 1 comprises a lower etch stop layer in between the substrate and the dielectric layer.

3. The method of claim 1 comprises reducing an initial height H_I of the dielectric layer to a thickness with a height H_F.

4. The method of claim 1 wherein the first and second materials comprise dielectric materials.

5. The method of claim 4 wherein the dielectric materials comprise NBLOK, low k NBLOK or a combination thereof.

6. The method of claim 4 wherein the first material comprises NBLOK, low k NBLOK or a combination thereof.

7. The method of claim 1 comprises providing a mask layer over the first etch stop layer to form the interconnect opening.

8. The method of claim 1 comprises providing a barrier layer lining surfaces of the dielectric layer and the interconnect opening.

9. The method of claim 8 comprises planarizing the conductive and barrier layers on the surface of the dielectric layer to form coplanar top surfaces of the interconnect and first upper etch stop layer.

10. A method for forming a semiconductor device comprising:

providing a substrate prepared with a dielectric layer and a first upper etch stop layer formed thereon;

forming an interconnect opening in the dielectric and first upper etch stop layers;

filling the interconnect opening with a conductive material to form an interconnect, the interconnect and first upper etch stop layer having coplanar top surfaces; and

forming a second upper etch stop layer over the coplanar top surfaces, wherein the second upper etch stop layer has sufficient adhesion with the first upper etch stop layer to reduce diffusion of the conductive material.

11. The method of claim 10 comprises recessing an initial thickness H_I of the dielectric layer to a thickness H_F prior to forming the first upper etch stop layer thereon.

12. The method of claim 10 wherein the first and second upper etch stop layers comprise same material.

13. The method of claim 12 wherein the first and second upper etch stop layers comprise dielectric materials.

14. The method of claim 13 wherein the dielectric materials comprise NBLOK, low k NBLOK or a combination thereof.

15. The method of claim 10 comprises providing a barrier layer lining surfaces of the dielectric layer and the interconnect opening.

16. The method of claim 15 comprises planarizing the conductive and barrier layers on the surface of the dielectric layer to form coplanar top surfaces of the interconnect and first upper etch stop layer.

17. A semiconductor device comprising:

a substrate; and

a dielectric layer on the substrate with an interconnect;

a first etch stop layer comprising a first material disposed on the surface of the dielectric layer, wherein top surfaces of the interconnect and first etch stop layer are coplanar; and

a second etch stop layer disposed on top surfaces of the interconnect and first etch stop layer, wherein the second etch stop layer comprises a second material having sufficient adhesion with the first material to reduce diffusion of conductive material of the interconnect.

18. The semiconductor device of claim 17 wherein the first and second materials comprise same material.

19. The semiconductor device of claim 18 wherein the first and second materials comprise dielectric materials.

20. The semiconductor device of claim 17 wherein the first material comprises NBLOK, low k NBLOK or a combination thereof.

What is claimed is:

CLAIMS

1. A method for forming a semiconductor device comprising:

providing a substrate prepared with a dielectric layer formed thereon;

reducing an initial height H_I of the dielectric layer to a thickness with a height H_F prior to forming a first upper etch stop layer so that the height of the dielectric layer following formation of an interconnect is the same as H_I to improve time dependent dielectric breakdown (TDDB);

forming the first upper etch stop layer on the dielectric layer, the first upper etch stop layer comprising a first material;

patterning the dielectric layer and first upper etch stop layer to form an interconnect opening;

filling the interconnect opening with a conductive material to form the interconnect, the interconnect and first upper etch stop layer having coplanar top surfaces; and

forming a second upper etch stop layer over the coplanar top surfaces and directly contacting the coplanar top surfaces, wherein the second upper etch stop layer comprises a second material similar to the first material to provide sufficient adhesion with the first material to reduce diffusion of the conductive material.

2. The method of claim 1 wherein the first and second materials comprise dielectric materials.

3. The method of claim 2 wherein the dielectric materials comprise Nitrogen doped Silicon Carbide, low k Nitrogen doped Silicon Carbide or a combination thereof.

4. The method of claim 2 wherein the first material comprises Nitrogen doped Silicon Carbide, low k Nitrogen doped Silicon Carbide or a combination thereof.

5. The method of claim 1 comprises providing a mask layer over the first etch stop layer to form the interconnect opening.

6. The method of claim 1 comprises providing a barrier layer lining surfaces of the dielectric layer and the interconnect opening.

7. The method of claim 6 comprises planarizing the conductive and barrier layers on the surface of the dielectric layer to form coplanar top surfaces of the interconnect and first upper etch stop layer.

8. A method for forming a semiconductor device comprising:

providing a substrate prepared with a dielectric layer and a first upper etch stop layer formed thereon;

recessing an initial thickness H_I of the dielectric layer to a thickness H_F prior to forming the first upper etch stop layer thereon so that the thickness of the dielectric layer plus the thickness of the first upper etch stop layer equals H_I;

forming an interconnect opening in the dielectric and first upper etch stop layers;

filling the interconnect opening with a conductive material to form an interconnect, the interconnect and first upper etch stop layer having coplanar top surfaces; and

forming a second upper etch stop layer over the coplanar top surfaces and directly contacting the coplanar top surfaces, wherein the second upper etch stop layer is similar to

the first upper etch stop layer and has sufficient adhesion with the first upper etch stop layer to reduce diffusion of the conductive material.

9. The method of claim 8 wherein the first and second upper etch stop layers comprise same material.

10. The method of claim 9 wherein the first and second upper etch stop layers comprise dielectric materials.

11. The method of claim 10 wherein the dielectric materials comprise Nitrogen doped Silicon Carbide, low k Nitrogen doped Silicon Carbide or a combination thereof.

12. The method of claim 8 comprises providing a barrier layer lining surfaces of the dielectric layer and the interconnect opening.

13. The method of claim 12 comprises planarizing the conductive and barrier layers on the surface of the dielectric layer to form coplanar top surfaces of the interconnect and first upper etch stop layer.