(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 December 2000 (14.12.2000)

PCT

(10) International Publication Number
WO 00/75988 A1

(51) International Patent Classification[7]: H01L 23/532

(21) International Application Number: PCT/US00/15801

(22) International Filing Date: 8 June 2000 (08.06.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/328,646 9 June 1999 (09.06.1999) US

(71) Applicant: ALLIEDSIGNAL INC. [US/US]; 101 Columbia Avenue, P.O. Box 2245, Morristown, NJ 07960 (US).

(72) Inventors: LIN, James; No. 14, 2nd Floor, Alley 154 Tong Yven Str., Taipei (TW). CHUNG, Henry; 11762 Trinity Spring Court, Cupertino, CA 95014 (US). WANG, Shi-Qing; 495 Virginia Avenue, Campbell, CA 95008 (US).

(74) Agents: CRISS, Roger, H. et al.; AlliedSignal Inc., 101 Columbia Avenue, P.O. Box 2245, Morristown, NJ 07960 (US).

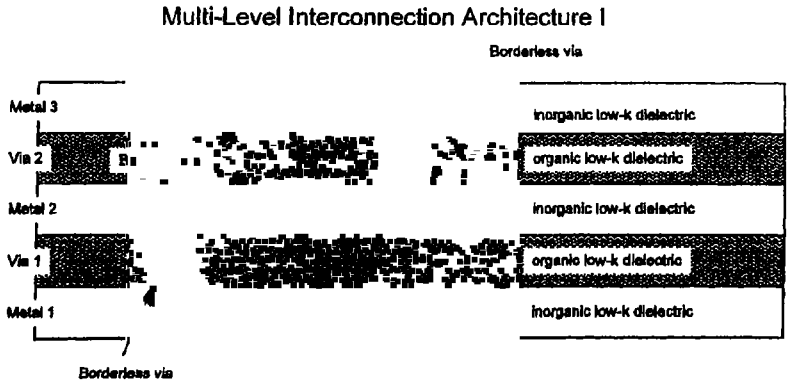
(81) Designated States *(national)*: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report*
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

[Continued on next page]

(54) Title: INTEGRATED CIRCUITS WITH MULTIPLE LOW DIELECTRIC-CONSTANT INTER-METAL DIELECTRICS





G00001

(57) Abstract: The invention provides processes for the formation of structures in microelectronic devices such as integrated circuit devices. More particularly, the invention relates to the formation of vias, interconnect metallization and wiring lines using multiple low dielectric-constant inter-metal dielectrics. The processes use two or more dissimilar low-k dielectrics for the inter-metal dielectrics of Cu-based dual damascene backends of integrated circuits. The use of both organic and inorganic low-k dielectrics offers advantages due to the significantly different plasma etch characteristics of the two kinds of dielectrics. One dielectric serves as the etchstop in etching the other dielectric so that no additional etchstop layer is required. Exceptional performance is achieved due to the lower parasitic capacitance resulting from the use of low-k dielectrics. An integrated circuit structure is formed having a substrate; an inorganic layer on the substrate which is composed of a pattern of metal lines on the substrate and an inorganic dielectric on the substrate between the metal lines; and an organic layer on the inorganic layer which is composed of an organic dielectric having metal filled vias therethrough which connect to the metal lines of the inorganic layer.

WO 00/75988 A1



162162

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.