WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a stack structure including a plurality of interlayer insulating layers and a plurality of gate conductive layers that are alternately stacked;

a channel plug at least partially passing through the stack structure on a cell region;

a plurality of support structures at least partially passing through the stack structure on a contact region, the plurality of support structures include a first support structure of a line type and a second support structure of a hole type; an auxiliary support structure formed on the stack structure, the first support structure, and the second support structure on the contact region,

wherein the auxiliary support structure includes a plurality of open regions,

wherein the plurality of open regions are spaced apart from each other in a first direction, and

wherein the first support structure overlaps at least two open regions spaced apart from each other in the first direction.

2. The semiconductor device of claim 1, wherein the plurality of open regions have a dash type.

3. The semiconductor device of claim 2, wherein the plurality of open regions are arranged in a matrix structure.

4. The semiconductor device of claim 1, wherein the auxiliary support structure has a mesh structure.

5. The semiconductor device of claim 1, further comprising:

a vertical structure of a line shape passing through an upper portion of the stack structure at a central portion of the cell region.

6. The semiconductor device of claim 5, wherein the auxiliary support structure extends to the cell region and has an open region overlapping with the vertical structure to expose a portion of the vertical structure.

7. The semiconductor device of claim 5, wherein the vertical structure passes through at least one gate conductive layer from the plurality of gate conductive layers that is a drain select line.

8. A semiconductor device comprising:

a stack structure including a plurality of interlayer

insulating layers and a plurality of gate conductive layers that are alternately stacked;

first and second channel plugs formed on a cell region by vertically passing through a portion or an entirety of the stack structure;

a plurality of support structures formed on a contact region by vertically passing through a portion or an entirety of the stack structure; and

an auxiliary support structure disposed on the stack structure and the plurality of support structures,

wherein the plurality of support structures include a first support structure of a line type,

wherein the auxiliary support structure includes a plurality of open regions which are spaced apart from each other in a first direction, and

wherein the first support structure overlaps at least two open regions spaced apart from each other in the first direction.

9. The semiconductor device of claim 8, wherein the plurality of support structures further include a second support structure of a hole type.

10. The semiconductor device of claim 8, wherein the auxiliary support structure is formed in a mesh structure.

11. The semiconductor device of claim 10, wherein each of the plurality of open regions has a dash type.

12. The semiconductor device of claim 8, further comprising:

a vertical structure of a line shape passing through an upper portion of the stack structure at a central portion of the cell region.

13. The semiconductor device of claim 12, wherein the open region exposes the vertical structure.

14. A method of manufacturing a semiconductor device, the method comprising the following steps:

forming a stack structure in which a plurality of interlayer insulating layers and a plurality of sacrificial layers are alternately stacked on a substrate including a cell region and a contact region;

etching the stack structure on the contact region to form first holes for forming a contact plug passing through a portion or an entirety of the stack structure, trenches for forming a first support structure, and second holes for forming a second support structure together;

forming contact plugs by filling the first holes with a barrier layer and a conductive layer;

filling the second holes and the trenches with the barrier layer and the conductive layer;

forming an auxiliary support structure including a plurality of open regions overlapping a portion of the trenches and a portion of the second holes on the stack structure;

removing the barrier layer and the conductive layer remaining in the trenches and the second holes exposed through the plurality of open regions of the auxiliary support structure; and

forming the first support structures and the second support structures by filling the trenches and the second holes with an insulating layer,

wherein the plurality of open regions are spaced apart from each other in a first direction, and

wherein each of the first support structures overlaps with at least two open regions spaced apart from each other in the first direction.

15. The method of claim 14, wherein each of the plurality of open regions has a dash type.

16. The method of claim 14, wherein the step of forming

the auxiliary support structure comprises forming the auxiliary support structure so that the auxiliary support structure extends above the stack structure on the cell region to expose a portion of the cell region.

17. The method of claim 16, further comprising before removing the barrier layer and the conductive layer remaining in the trenches and the second holes:

forming a slit by partially etching an upper end of the stack structure on the cell region exposed through the auxiliary support structure.

18. The method of claim 17, wherein in forming the first support structures and the second support structures, the insulating layer is filled in the slit to form a vertical structure.

19. The method of claim 14, wherein the first support structures are formed in a line shape, and widths of each of the first support structures are different from each other.