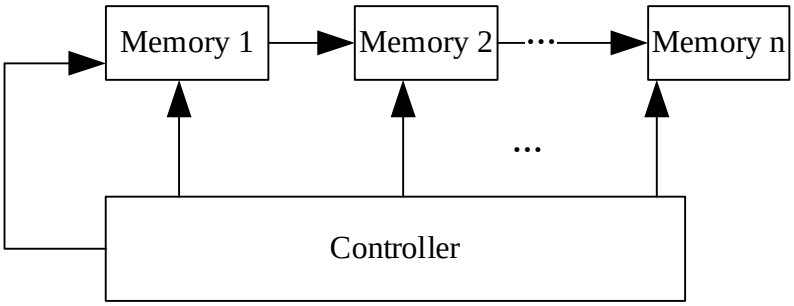


FIG. 1

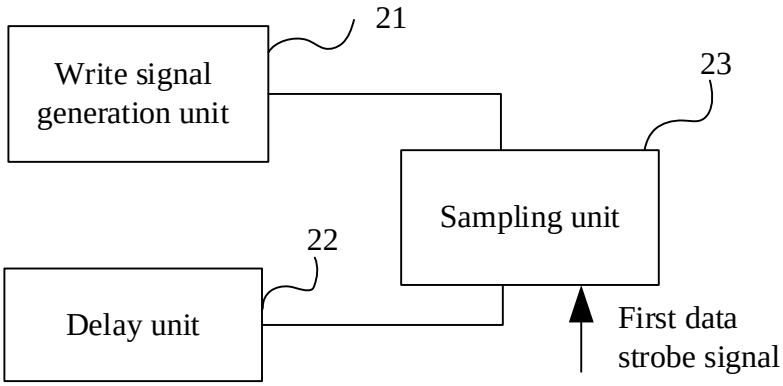


FIG. 2

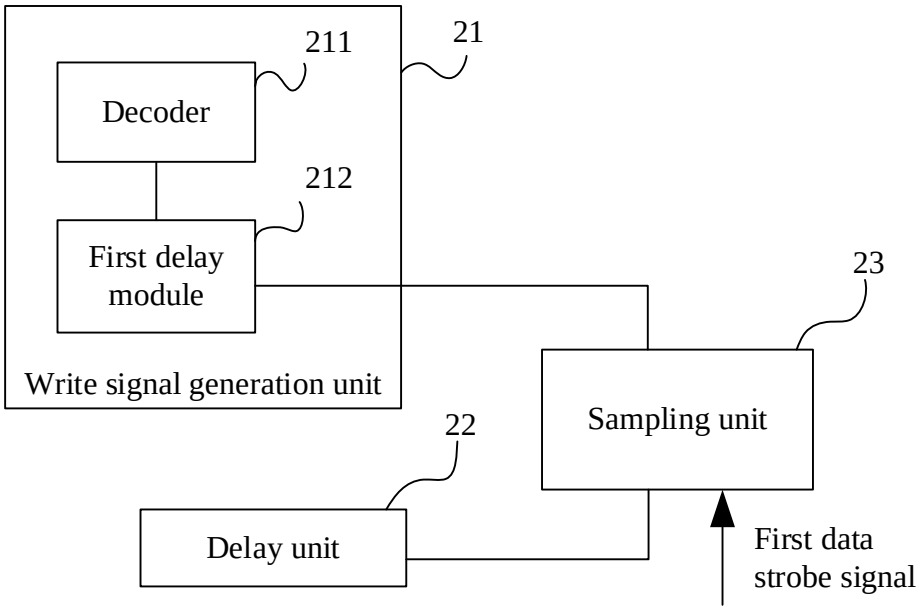


FIG. 3

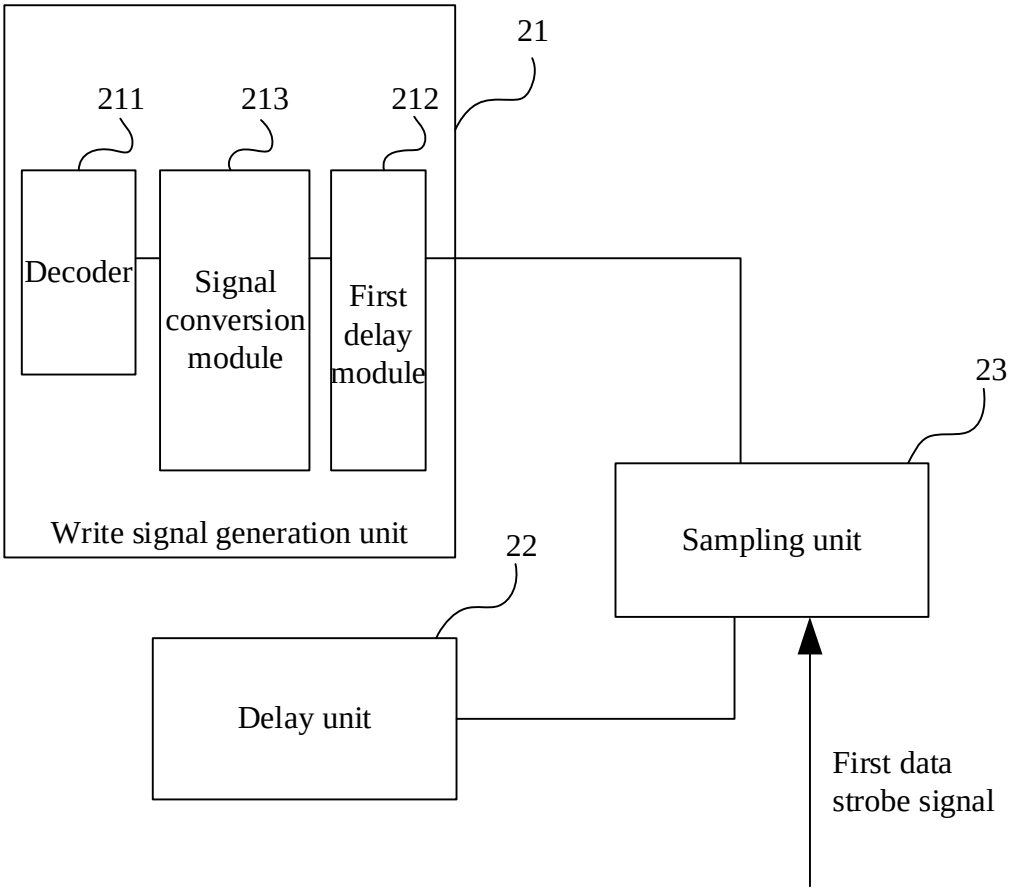

21
211
213
212
Decoder
Signal conversion module
First delay module
Write signal generation unit
23
Sampling unit
22
Delay unit
First data strobe signal

FIG. 4

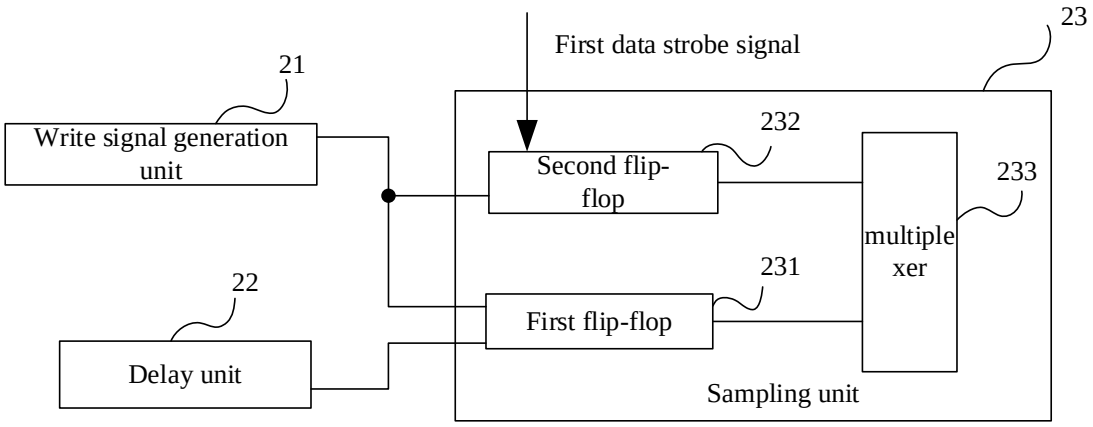

First data strobe signal
23
21
Write signal generation unit
232
Second flip-flop
233
multiple xer
231
First flip-flop
22
Delay unit
Sampling unit

FIG. 5

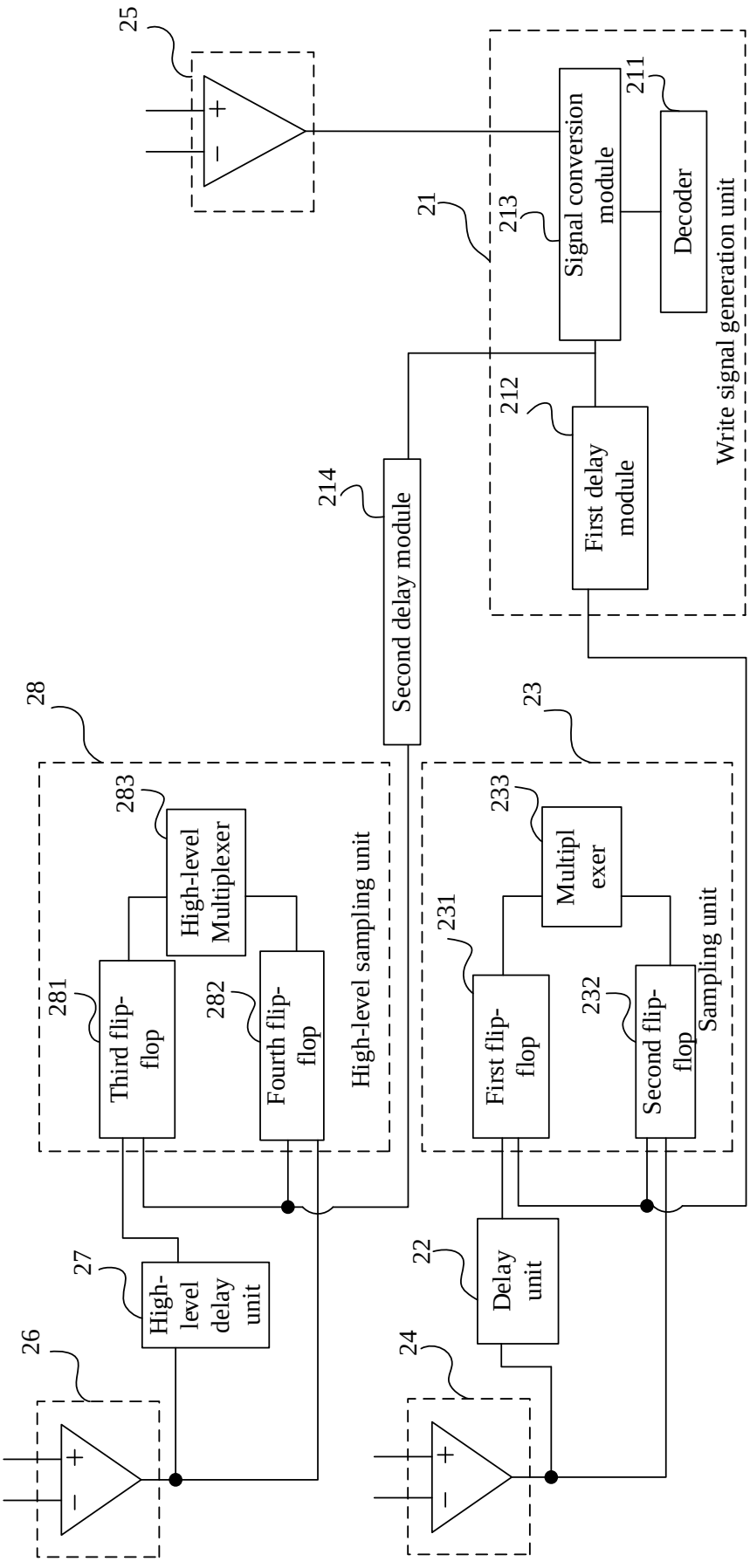

25
21
211
Decoder
213
Signal conversion module
212
First delay module
Write signal generation unit
214
Second delay module
28
23
283
High-level Multiplexer
233
Multipl exer
281
Third flip-flop
282
Fourth flip-flop
High-level sampling unit
231
First flip-flop
232
Second flip-flop
Sampling unit
27
High-level delay unit
22
Delay unit
26
24

FIG. 6

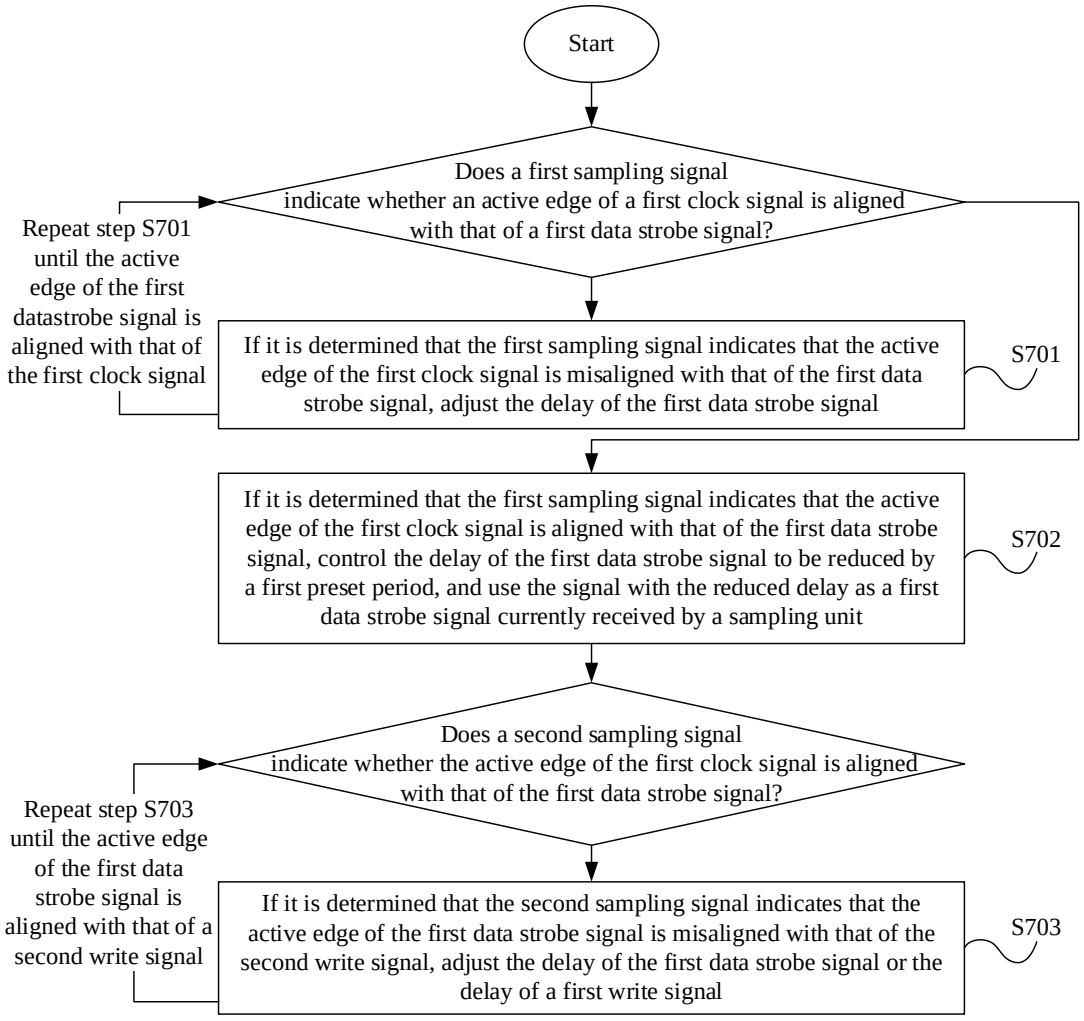

Start
Does a first sampling signal indicate whether an active edge of a first clock signal is aligned with that of a first data strobe signal?
Repeat step S701 until the active edge of the first datastrobe signal is aligned with that of the first clock signal
If it is determined that the first sampling signal indicates that the active edge of the first clock signal is misaligned with that of the first data strobe signal, adjust the delay of the first data strobe signal
S701
If it is determined that the first sampling signal indicates that the active edge of the first clock signal is aligned with that of the first data strobe signal, control the delay of the first data strobe signal to be reduced by a first preset period, and use the signal with the reduced delay as a first data strobe signal currently received by a sampling unit
S702
Does a second sampling signal indicate whether the active edge of the first clock signal is aligned with that of the first data strobe signal?
Repeat step S703 until the active edge of the first data strobe signal is aligned with that of a second write signal
If it is determined that the second sampling signal indicates that the active edge of the first data strobe signal is misaligned with that of the second write signal, adjust the delay of the first data strobe signal or the delay of a first write signal
S703

FIG. 7

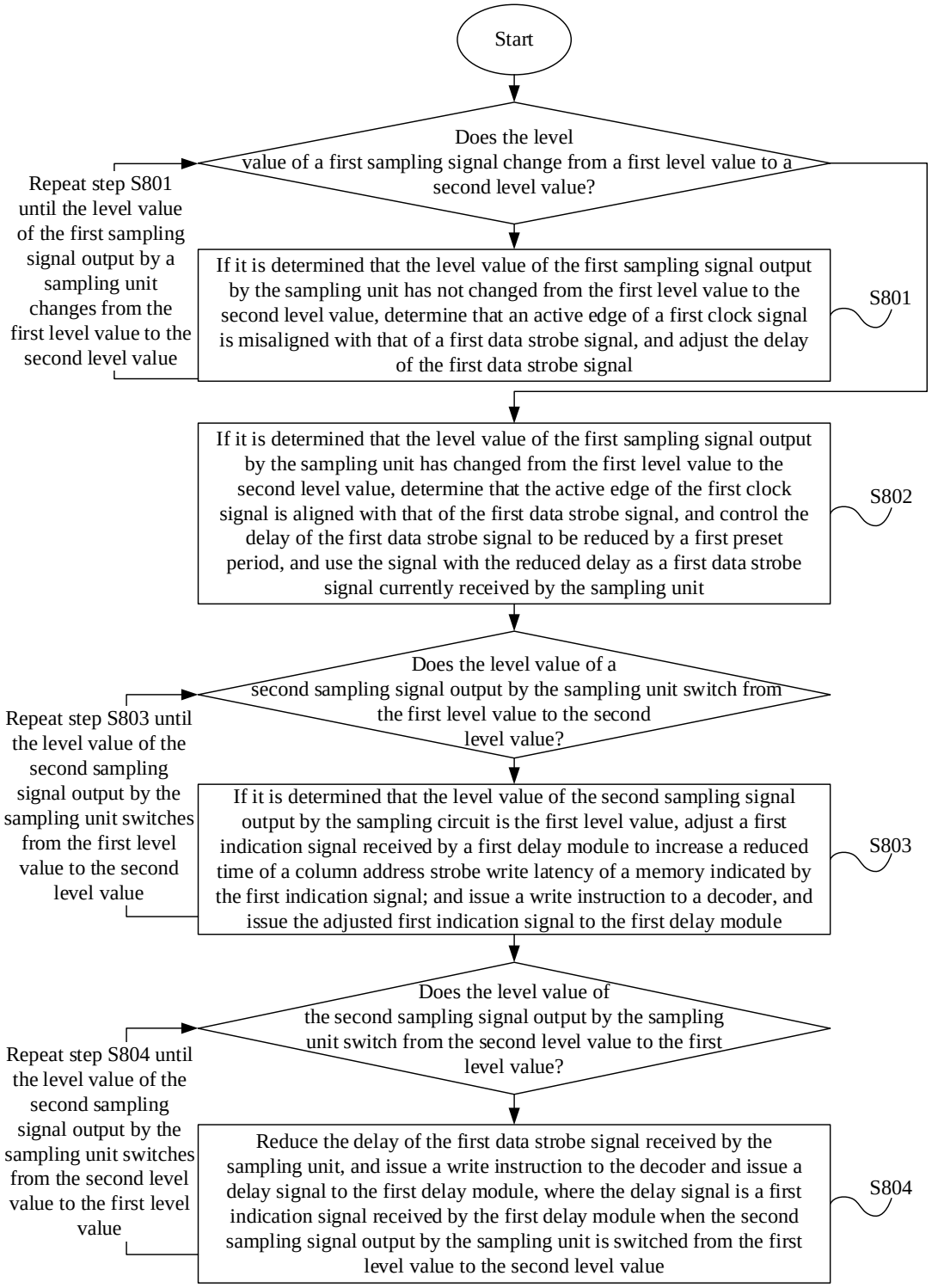

Start
Does the level value of a first sampling signal change from a first level value to a second level value?
Repeat step S801 until the level value of the first sampling signal output by a sampling unit changes from the first level value to the second level value
If it is determined that the level value of the first sampling signal output by the sampling unit has not changed from the first level value to the second level value, determine that an active edge of a first clock signal is misaligned with that of a first data strobe signal, and adjust the delay of the first data strobe signal
S801
If it is determined that the level value of the first sampling signal output by the sampling unit has changed from the first level value to the second level value, determine that the active edge of the first clock signal is aligned with that of the first data strobe signal, and control the delay of the first data strobe signal to be reduced by a first preset period, and use the signal with the reduced delay as a first data strobe signal currently received by the sampling unit
S802
Does the level value of a second sampling signal output by the sampling unit switch from the first level value to the second level value?
Repeat step S803 until the level value of the second sampling signal output by the sampling unit switches from the first level value to the second level value
If it is determined that the level value of the second sampling signal output by the sampling circuit is the first level value, adjust a first indication signal received by a first delay module to increase a reduced time of a column address strobe write latency of a memory indicated by the first indication signal; and issue a write instruction to a decoder, and issue the adjusted first indication signal to the first delay module
S803
Does the level value of the second sampling signal output by the sampling unit switch from the second level value to the first level value?
Repeat step S804 until the level value of the second sampling signal output by the sampling unit switches from the second level value to the first level value
Reduce the delay of the first data strobe signal received by the sampling unit, and issue a write instruction to the decoder and issue a delay signal to the first delay module, where the delay signal is a first indication signal received by the first delay module when the second sampling signal output by the sampling unit is switched from the first level value to the second level value
S804

FIG. 8

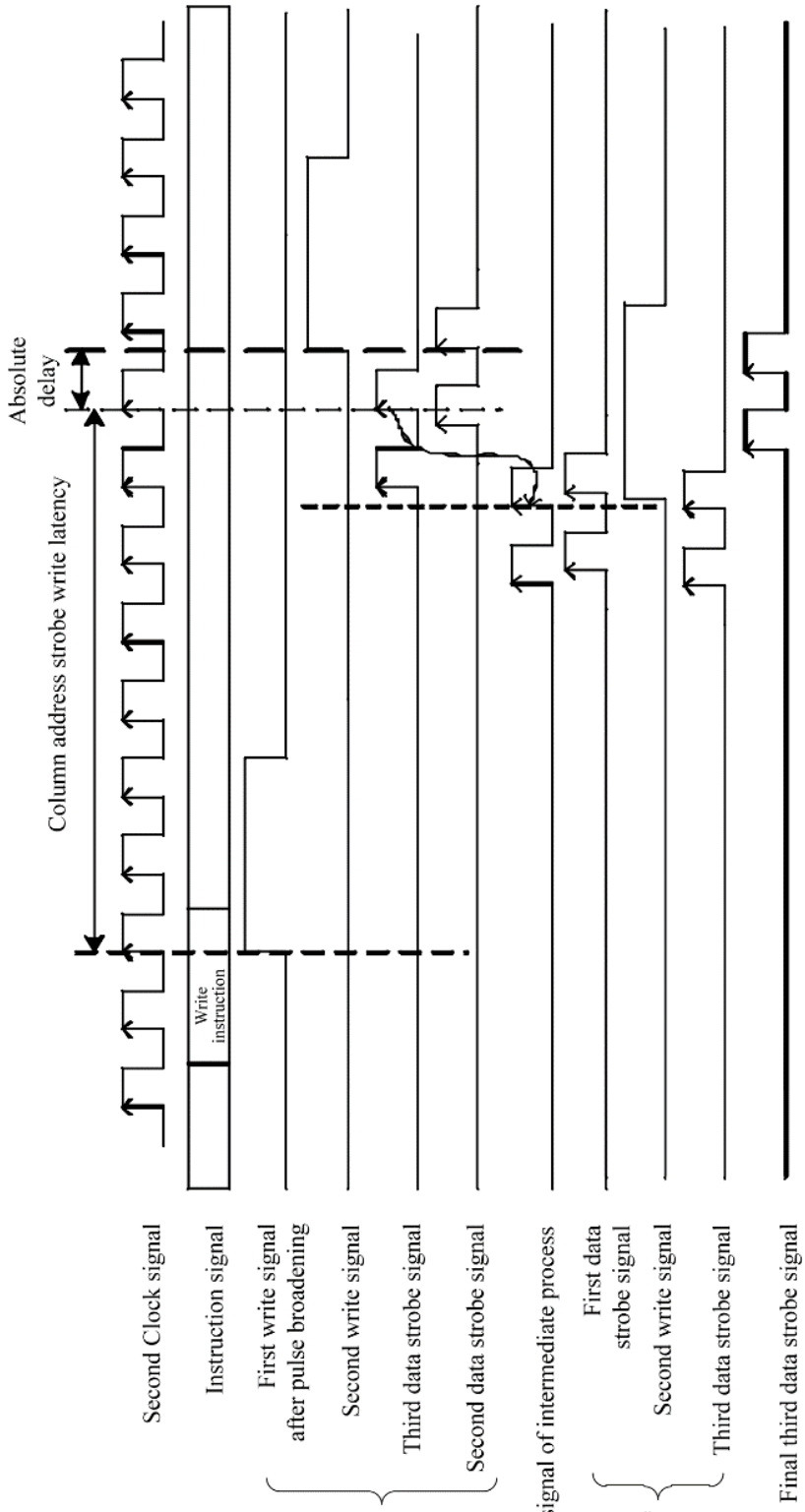

Absolute delay
Column address strobe write latency
Write instruction
Second Clock signal
Instruction signal
First write signal after pulse broadening
Second write signal
Third data strobe signal
Second data strobe signal
External write leveling
Third data strobe signal of intermediate process
First data strobe signal
Second write signal
Third data strobe signal
Internal write leveling
Final third data strobe signal

FIG. 9

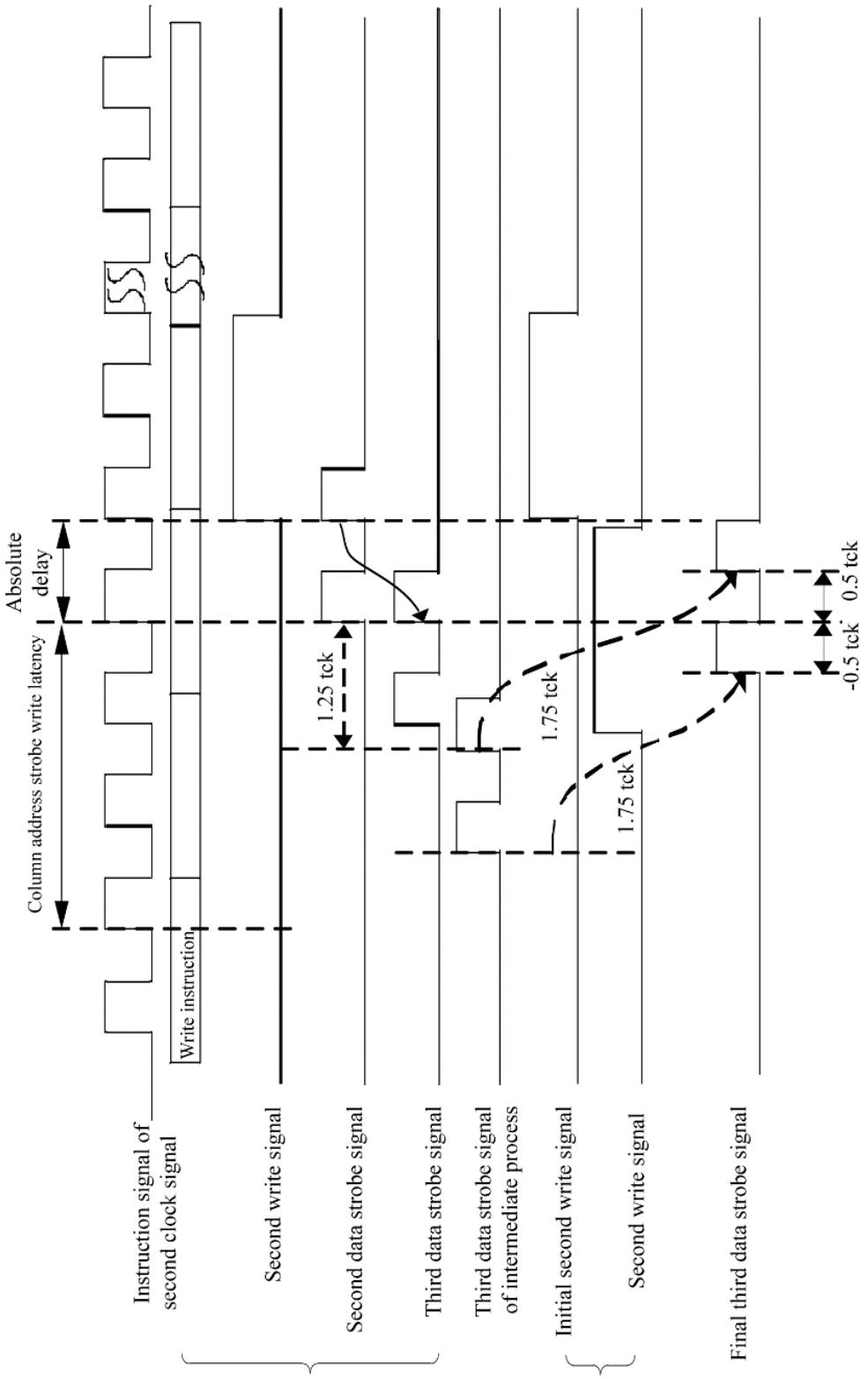

Absolute delay
Column address strobe write latency
Write instruction
Instruction signal of second clock signal
Second write signal
Second data strobe signal
Third data strobe signal
Third data strobe signal of intermediate process
Initial second write signal
Second write signal
Final third data strobe signal
1.25 tck
1.75 tck
1.75 tck
-0.5 tck
0.5 tck
External write leveling
Internal write leveling

FIG. 10

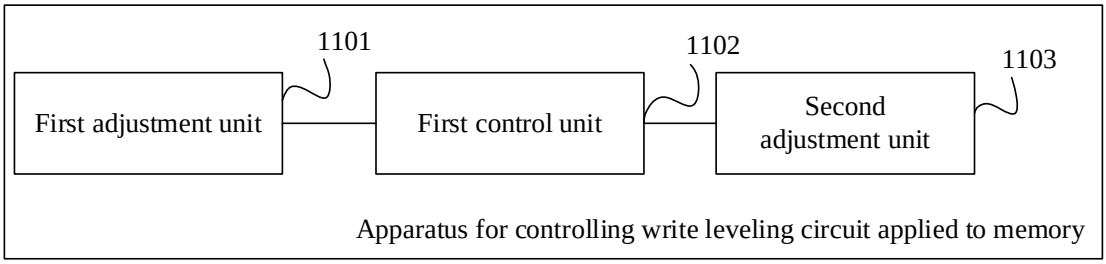

1101
1102
1103
First adjustment unit
First control unit
Second adjustment unit
Apparatus for controlling write leveling circuit applied to memory

FIG. 11

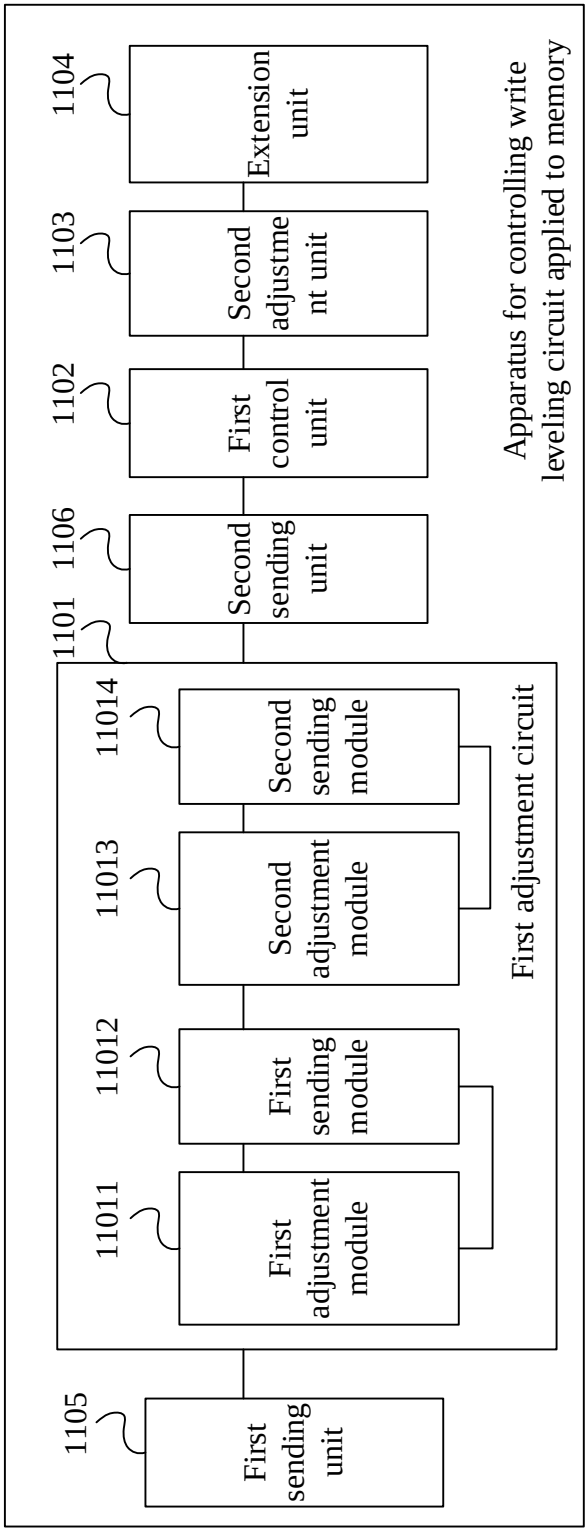

Apparatus for controlling write leveling circuit applied to memory
1101
First adjustment circuit
11011
First adjustment module
11012
First sending module
11013
Second adjustment module
11014
Second sending module
1102
First control unit
1103
Second adjustment unit
1104
Extension unit
1105
First sending unit
1106
Second sending unit

FIG. 12

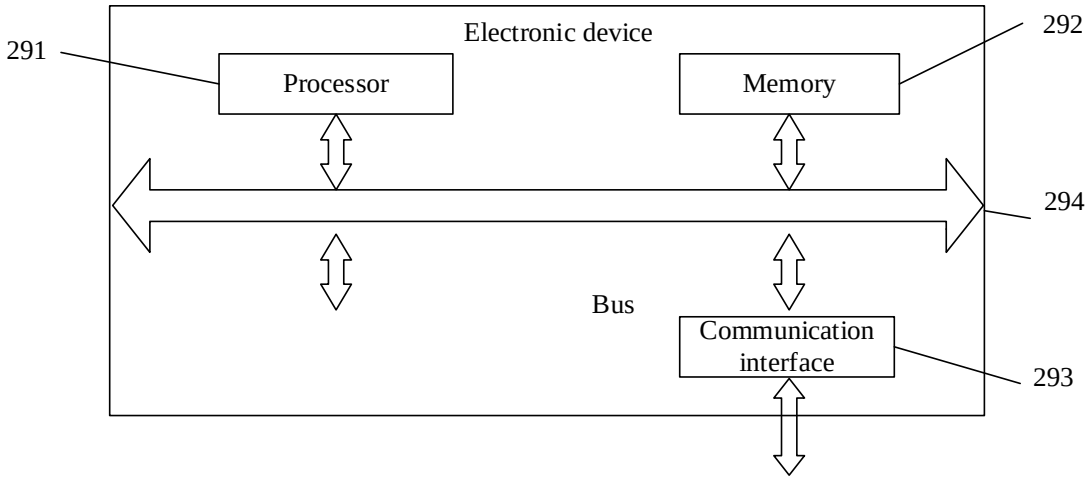

Electronic device
291
Processor
Memory
292
294
Bus
Communication interface
293

FIG. 13