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(54) **Title:** SYSTEM, METHOD, AND APPARATUS FOR WAFER-SCALE MEMORY

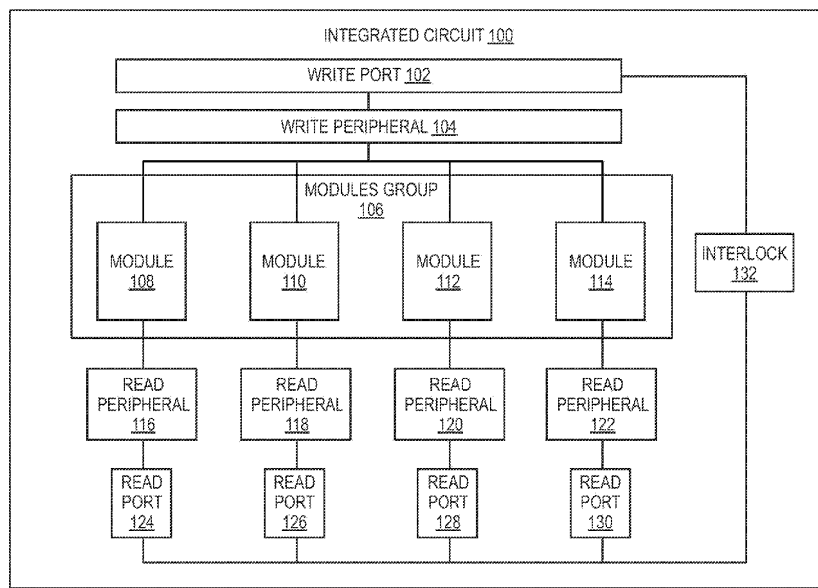


FIG. 1

(57) **Abstract:** A semiconductor package is provided that includes a memory wafer and an application wafer bonded together to create a system for data processing and memory storage. The memory wafer hosts multiple modules groups, each with several modules, a shared write port, and independent read ports, allowing for concurrent read operations. The application wafer, which communicates operatively with the memory wafer, may include various processing elements such as FPGA cores, GPUs, CPUs, and neural network accelerators. Both wafers can have coextensive outer perimeters, supporting configurations like rectangular, square, and round shapes, and providing substantial memory capacity. The package may use bump-less bonding technology to reduce thermal and electrical resistance and incorporates through-silicon vias (TSVs) for robust interconnectivity.

[Continued on next page]

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