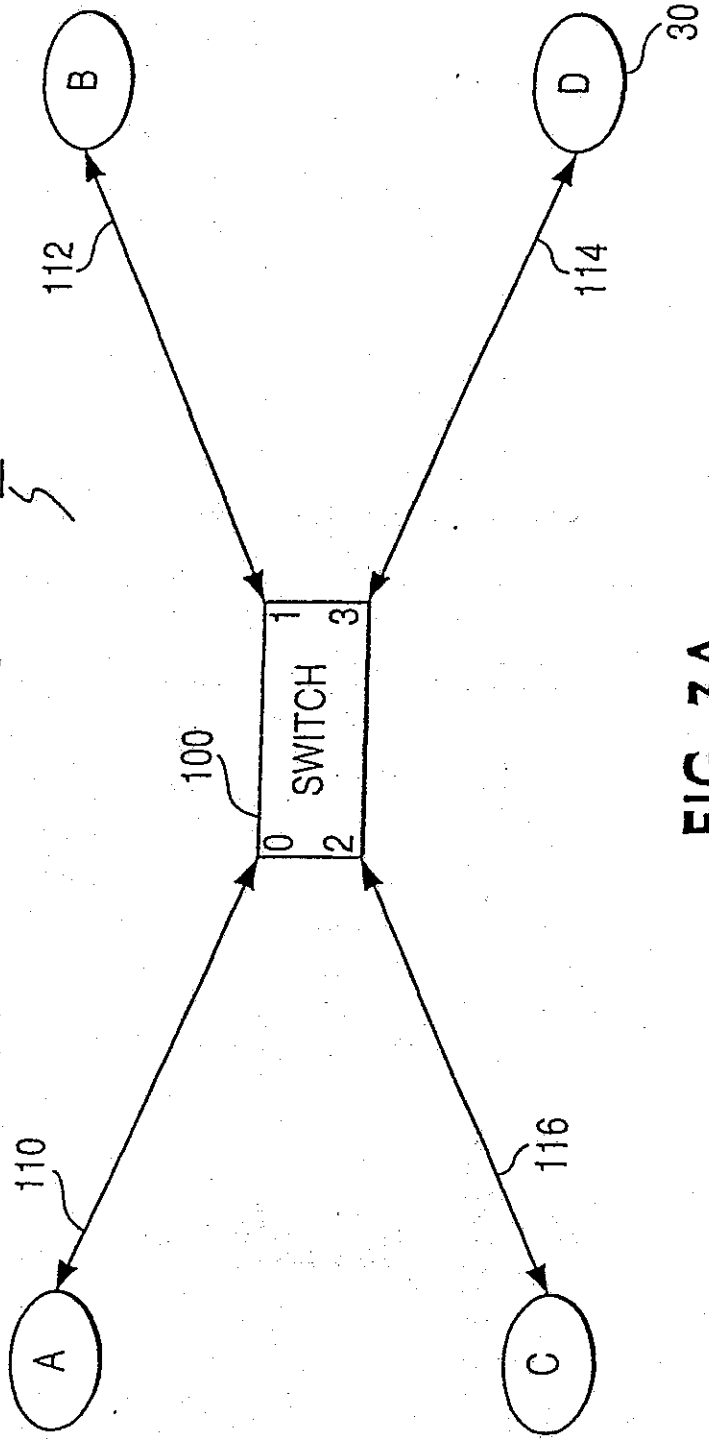

10
A
B
C
D
30
110
112
114
116
100
SWITCH
0
1
2
3

FIG. 1

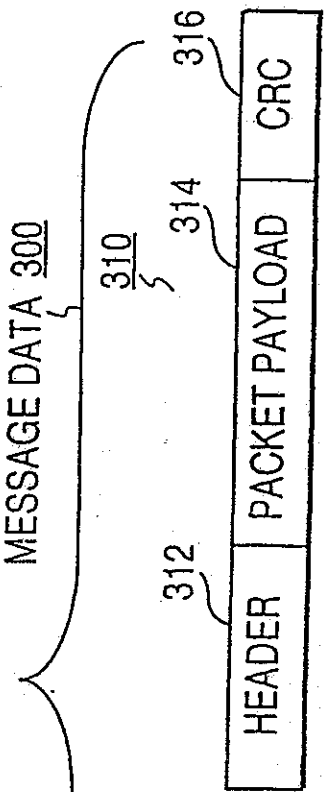

MESSAGE DATA 300
310
312
HEADER
314
PACKET PAYLOAD
316
CRC

FIG. 3A

FIG. 2

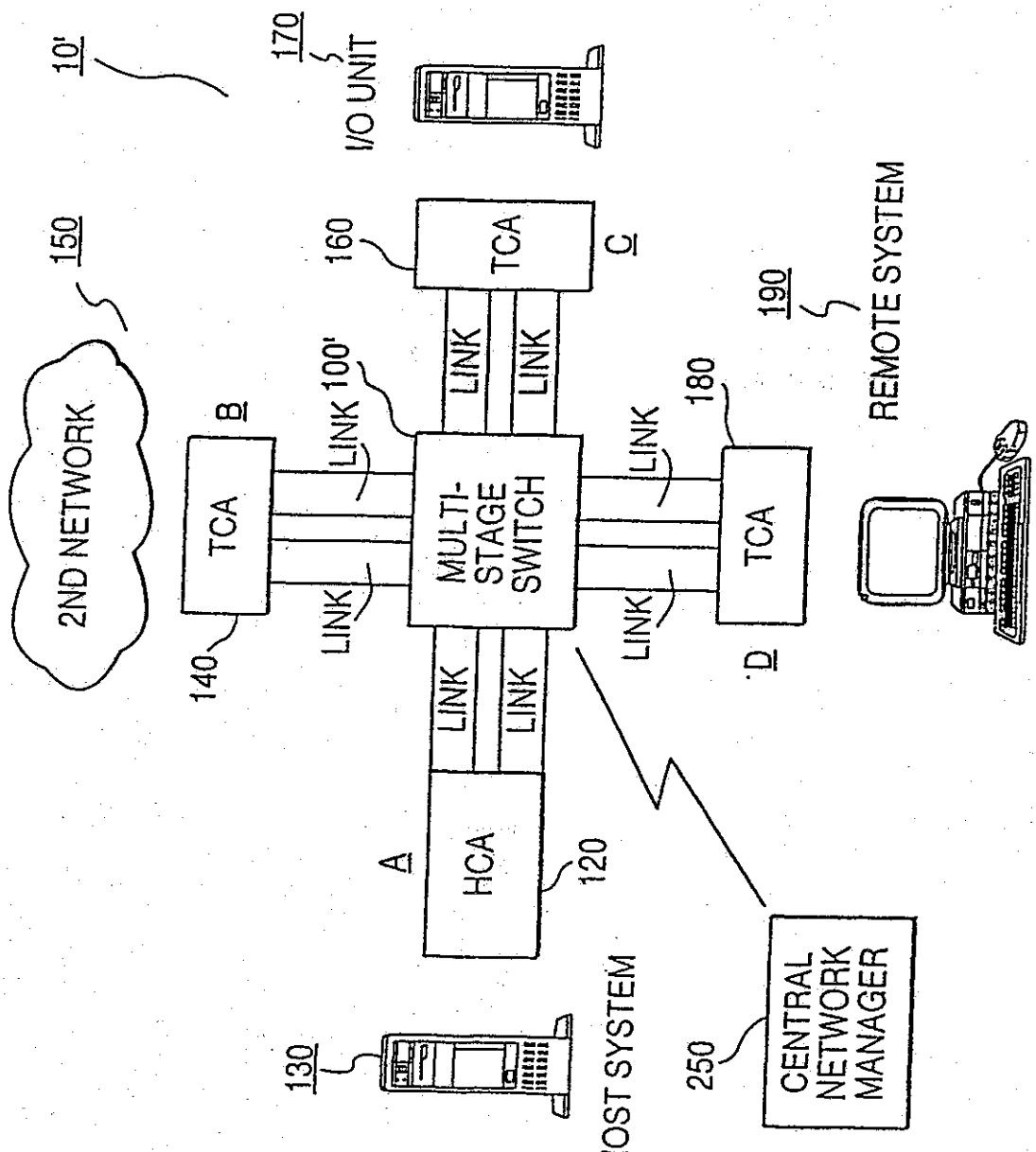
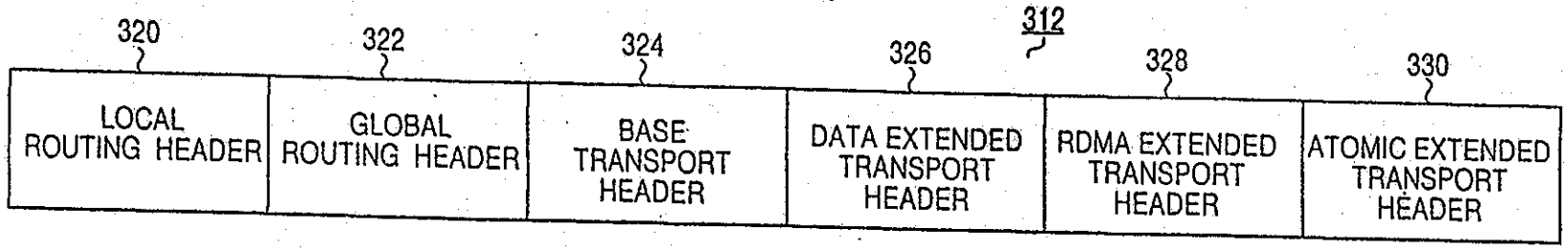

10'
170
I/O UNIT
150
2ND NETWORK
160
TCA
C
LINK
LINK
100'
B
TCA
LINK
MULTI-
STAGE
SWITCH
LINK
180
190
REMOTE SYSTEM
TCA
D
LINK
LINK
140
LINK
LINK
A
HCA
120
130
HOST SYSTEM
250
CENTRAL
NETWORK
MANAGER

FIG. 3B


312
320
LOCAL ROUTING HEADER
322
GLOBAL ROUTING HEADER
324
BASE TRANSPORT HEADER
326
DATA EXTENDED TRANSPORT HEADER
328
RDMA EXTENDED TRANSPORT HEADER
330
ATOMIC EXTENDED TRANSPORT HEADER

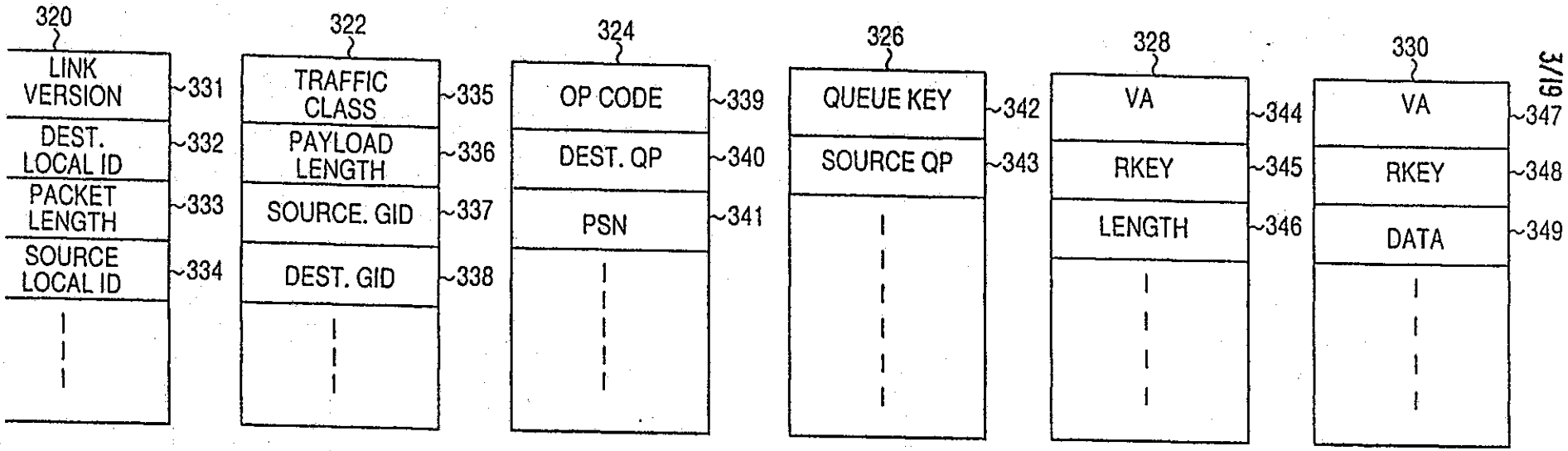

320
LINK VERSION
331
DEST. LOCAL ID
332
PACKET LENGTH
333
SOURCE LOCAL ID
334
322
TRAFFIC CLASS
335
PAYLOAD LENGTH
336
SOURCE. GID
337
DEST. GID
338
324
OP CODE
339
DEST. QP
340
PSN
341
326
QUEUE KEY
342
SOURCE QP
343
328
VA
344
RKEY
345
LENGTH
346
330
VA
347
RKEY
348
DATA
349

FIG. 3C

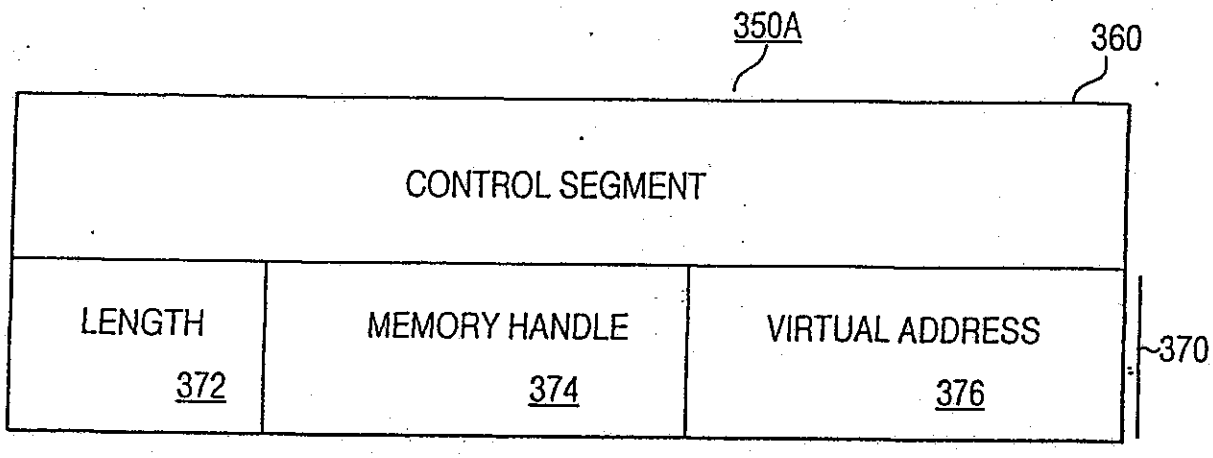

350A
360
CONTROL SEGMENT
LENGTH
372
MEMORY HANDLE
374
VIRTUAL ADDRESS
376
370

FIG. 3D

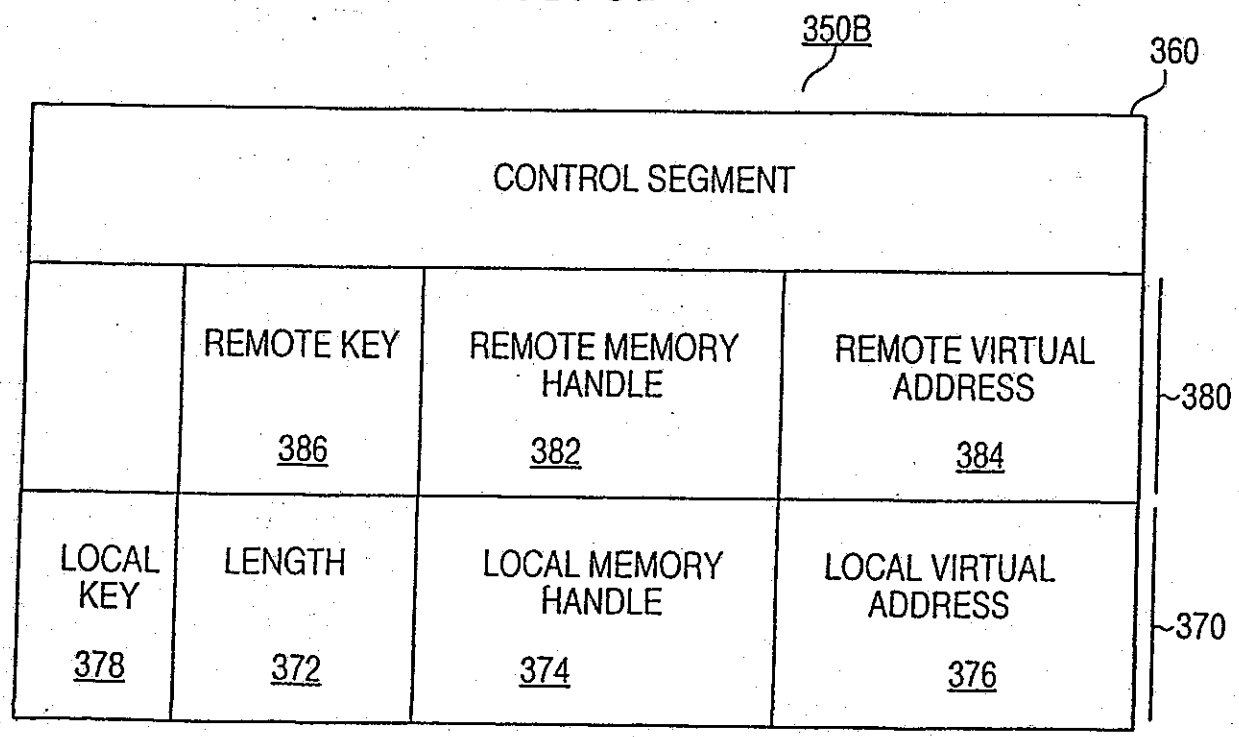

350B
360
CONTROL SEGMENT
REMOTE KEY
386
REMOTE MEMORY HANDLE
382
REMOTE VIRTUAL ADDRESS
384
380
LOCAL KEY
378
LENGTH
372
LOCAL MEMORY HANDLE
374
LOCAL VIRTUAL ADDRESS
376
370

FIG. 4A

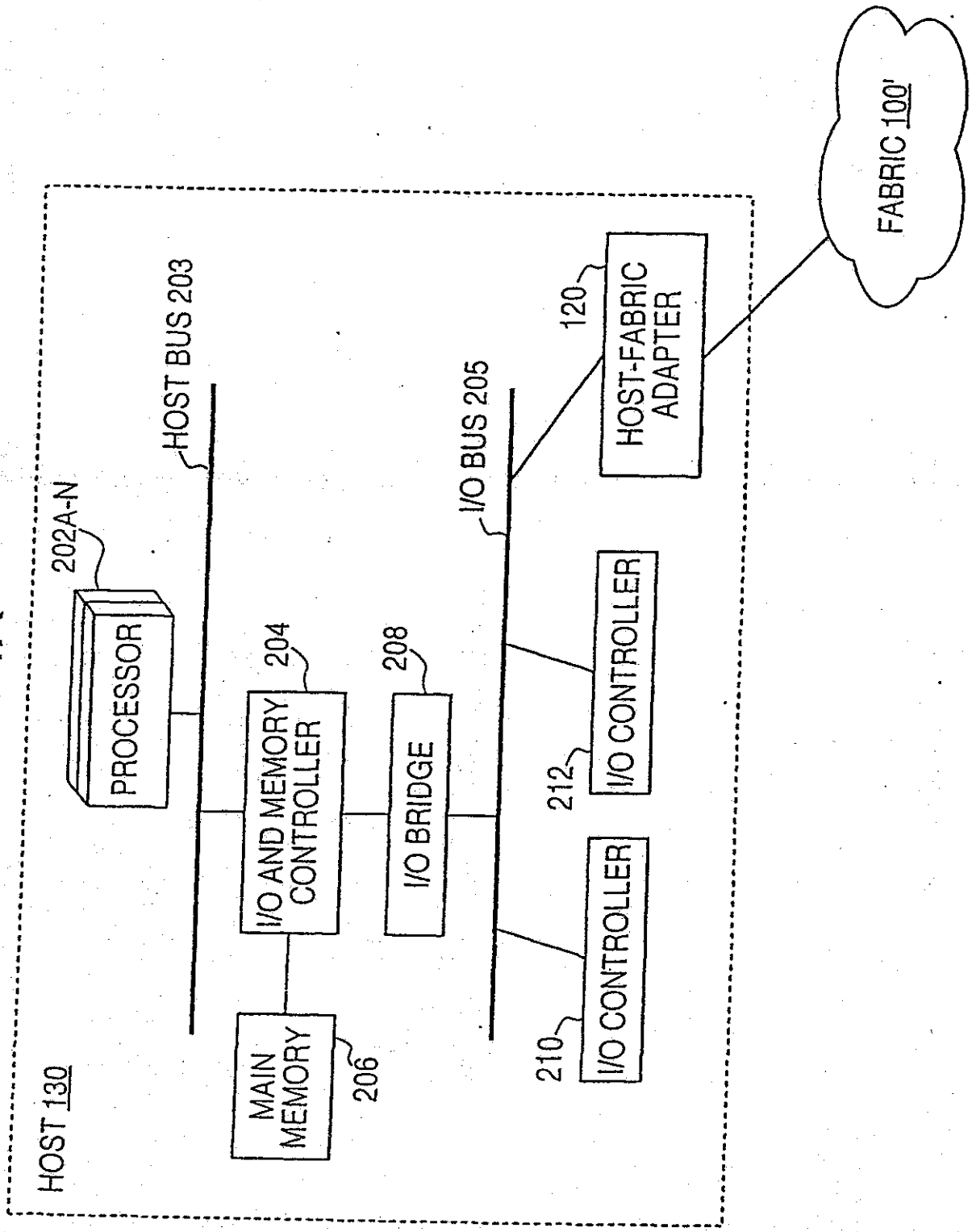

HOST 130
PROCESSOR
202A-N
HOST BUS 203
I/O AND MEMORY CONTROLLER
204
MAIN MEMORY
206
I/O BRIDGE
208
I/O BUS 205
I/O CONTROLLER
210
I/O CONTROLLER
212
HOST-FABRIC ADAPTER
120
FABRIC 100'

FIG. 4B

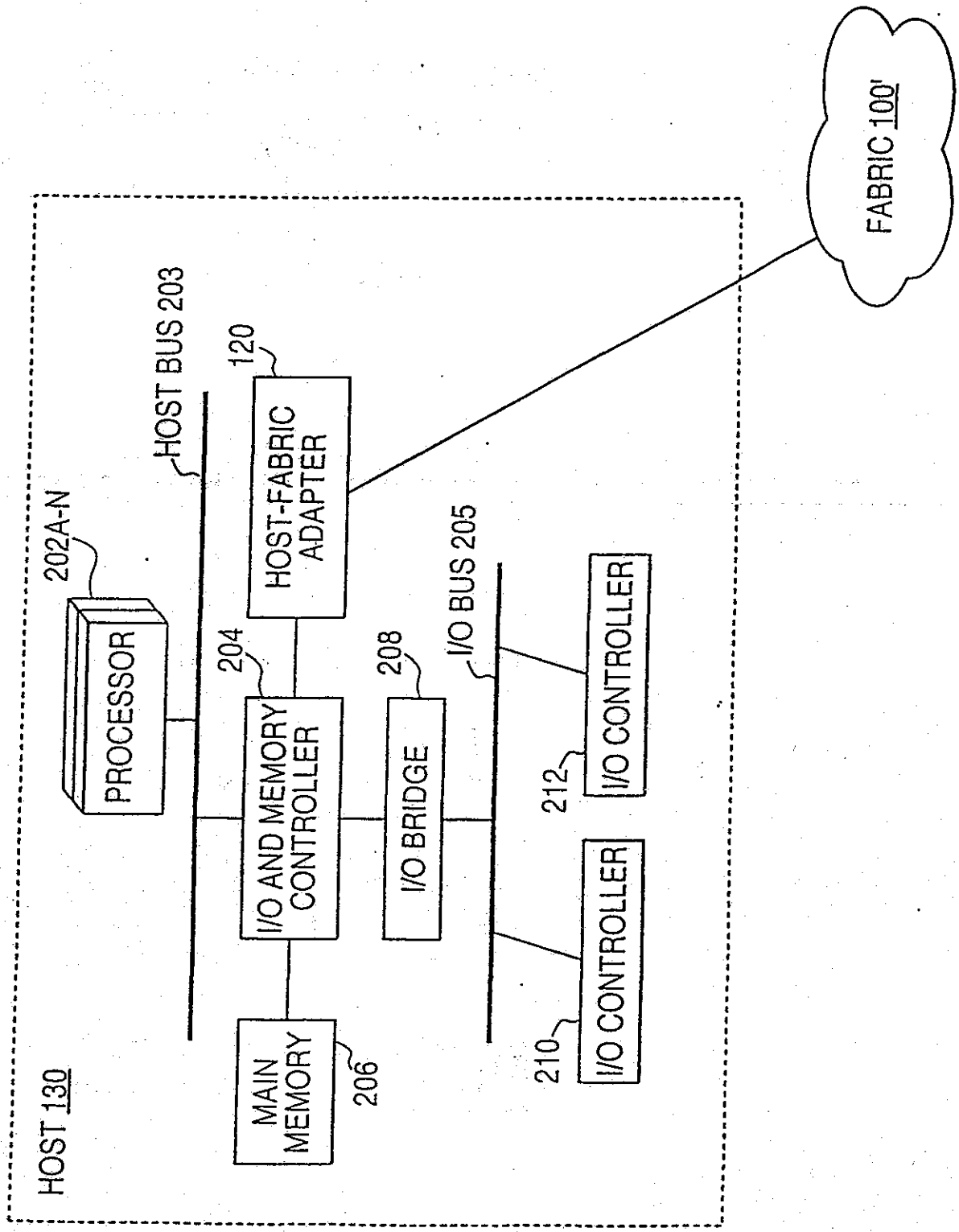

FABRIC 100'
HOST 130
HOST BUS 203
120
HOST-FABRIC ADAPTER
202A-N
PROCESSOR
204
I/O AND MEMORY CONTROLLER
208
I/O BRIDGE
I/O BUS 205
MAIN MEMORY
206
212
I/O CONTROLLER
210
I/O CONTROLLER

FIG. 5

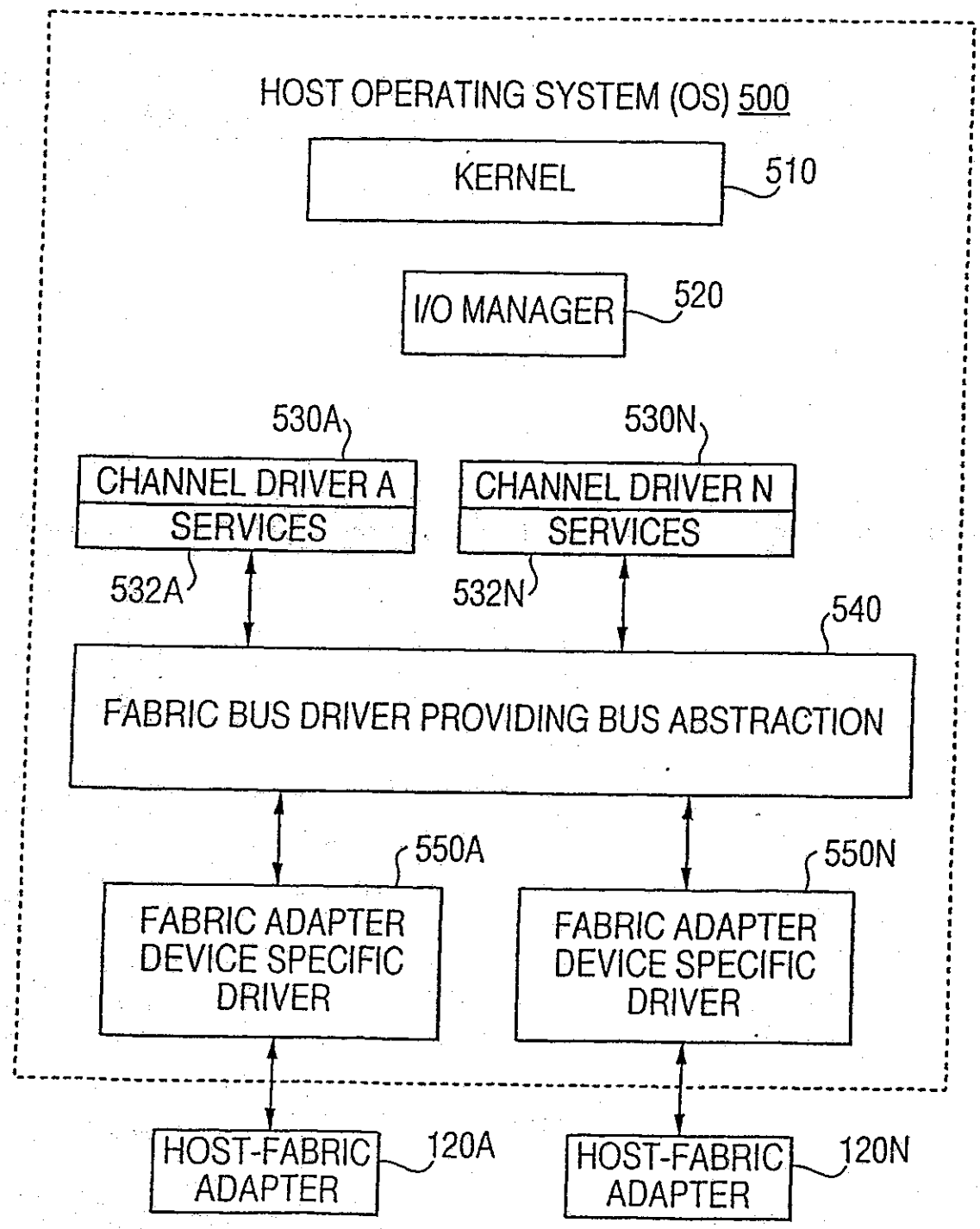

HOST OPERATING SYSTEM (OS) 500
KERNEL
510
I/O MANAGER
520
530A
530N
CHANNEL DRIVER A SERVICES
CHANNEL DRIVER N SERVICES
532A
532N
540
FABRIC BUS DRIVER PROVIDING BUS ABSTRACTION
550A
550N
FABRIC ADAPTER DEVICE SPECIFIC DRIVER
FABRIC ADAPTER DEVICE SPECIFIC DRIVER
HOST-FABRIC ADAPTER
120A
HOST-FABRIC ADAPTER
120N

FIG. 6

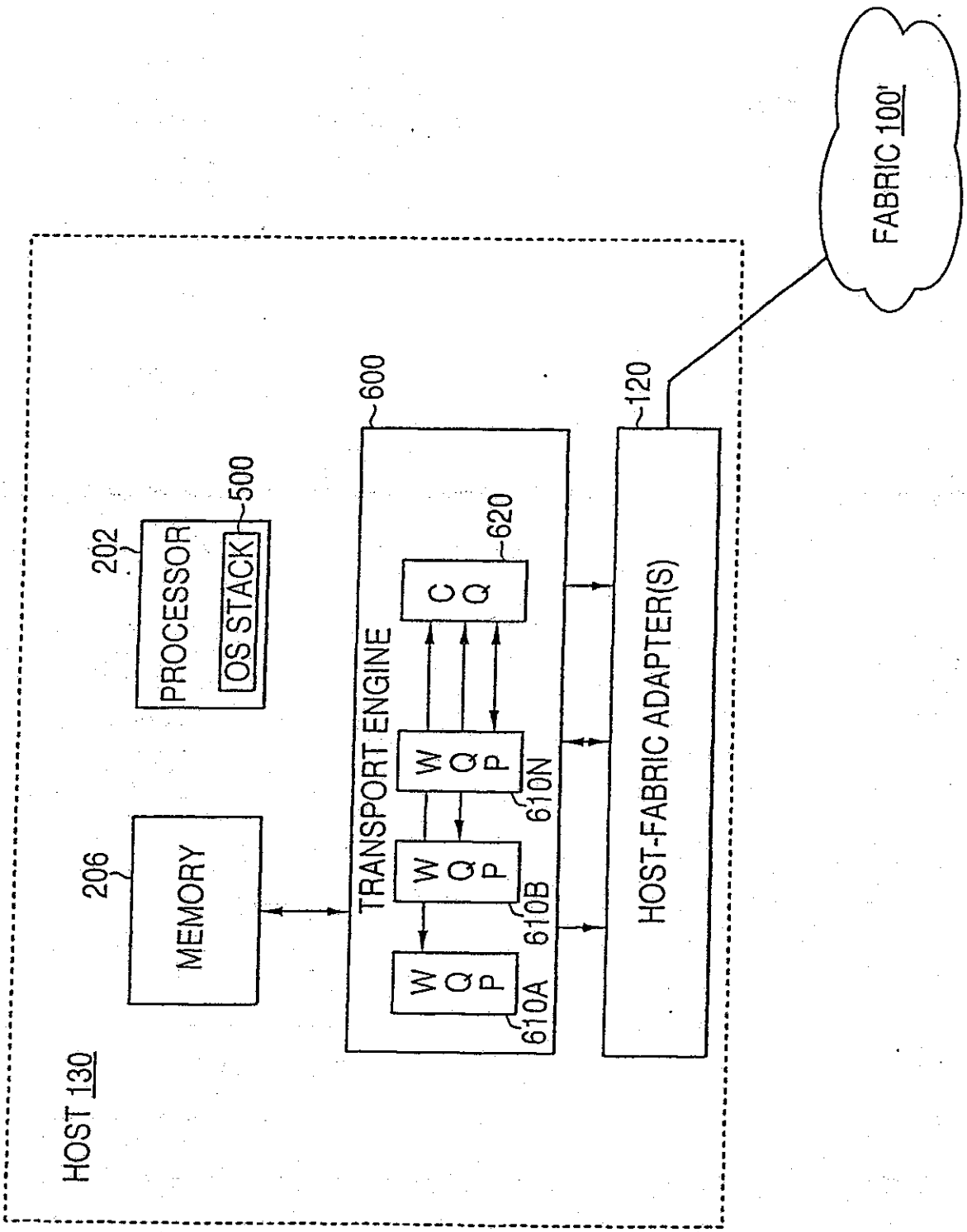

FABRIC 100'
HOST 130
PROCESSOR
202
OS STACK
500
MEMORY
206
TRANSPORT ENGINE
600
WQP
610A
WQP
610B
WQP
610N
CQ
620
HOST-FABRIC ADAPTER(S)
120

FIG. 7

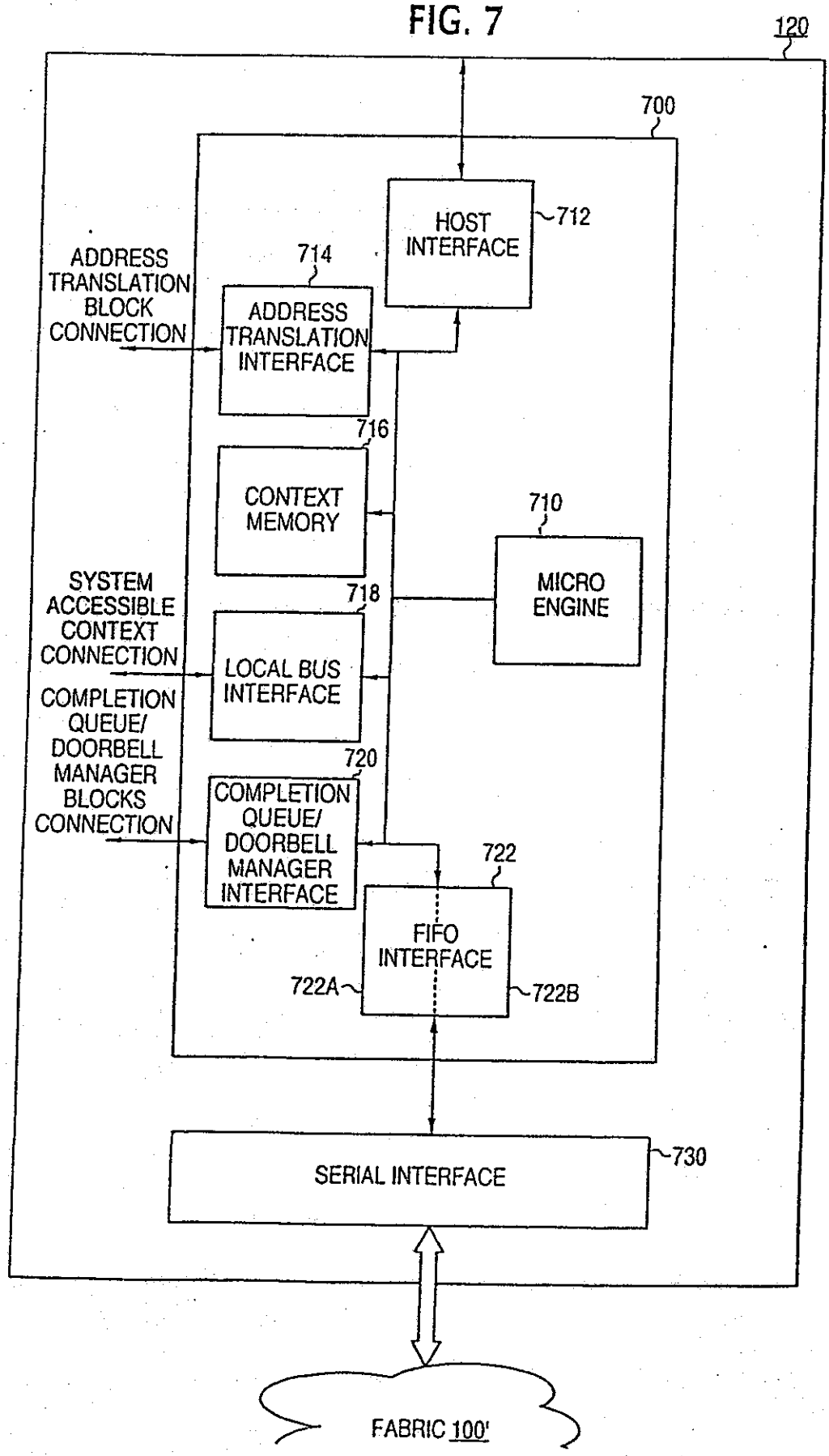

120
700
HOST INTERFACE
712
ADDRESS TRANSLATION BLOCK CONNECTION
714
ADDRESS TRANSLATION INTERFACE
716
CONTEXT MEMORY
710
MICRO ENGINE
SYSTEM ACCESSIBLE CONTEXT CONNECTION
718
LOCAL BUS INTERFACE
COMPLETION QUEUE/ DOORBELL MANAGER BLOCKS CONNECTION
720
COMPLETION QUEUE/ DOORBELL MANAGER INTERFACE
722
FIFO INTERFACE
722A
722B
SERIAL INTERFACE
730
FABRIC 100'

FIG. 8

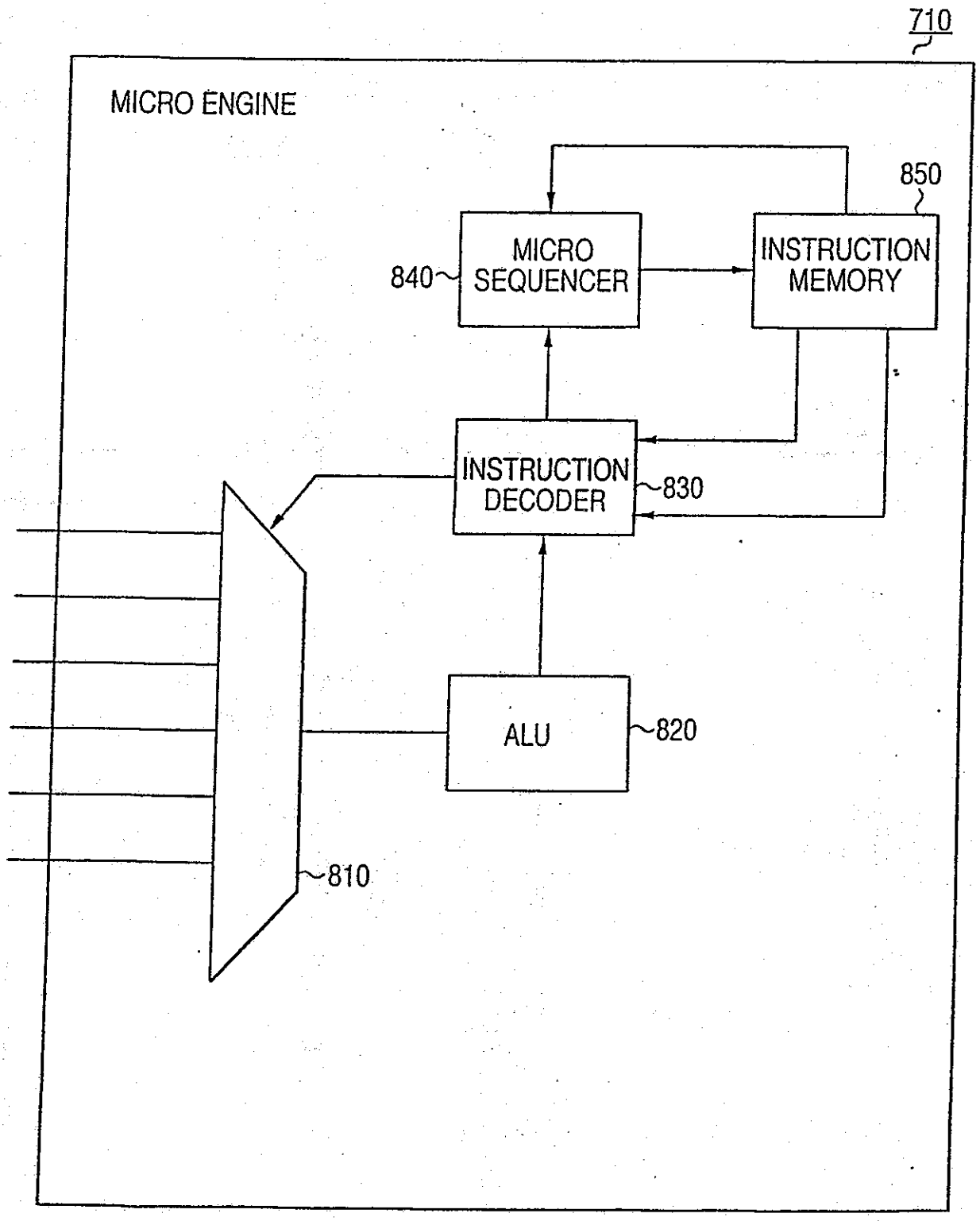

710
MICRO ENGINE
850
MICRO SEQUENCER
840
INSTRUCTION MEMORY
INSTRUCTION DECODER
830
ALU
820
810

FIG. 9

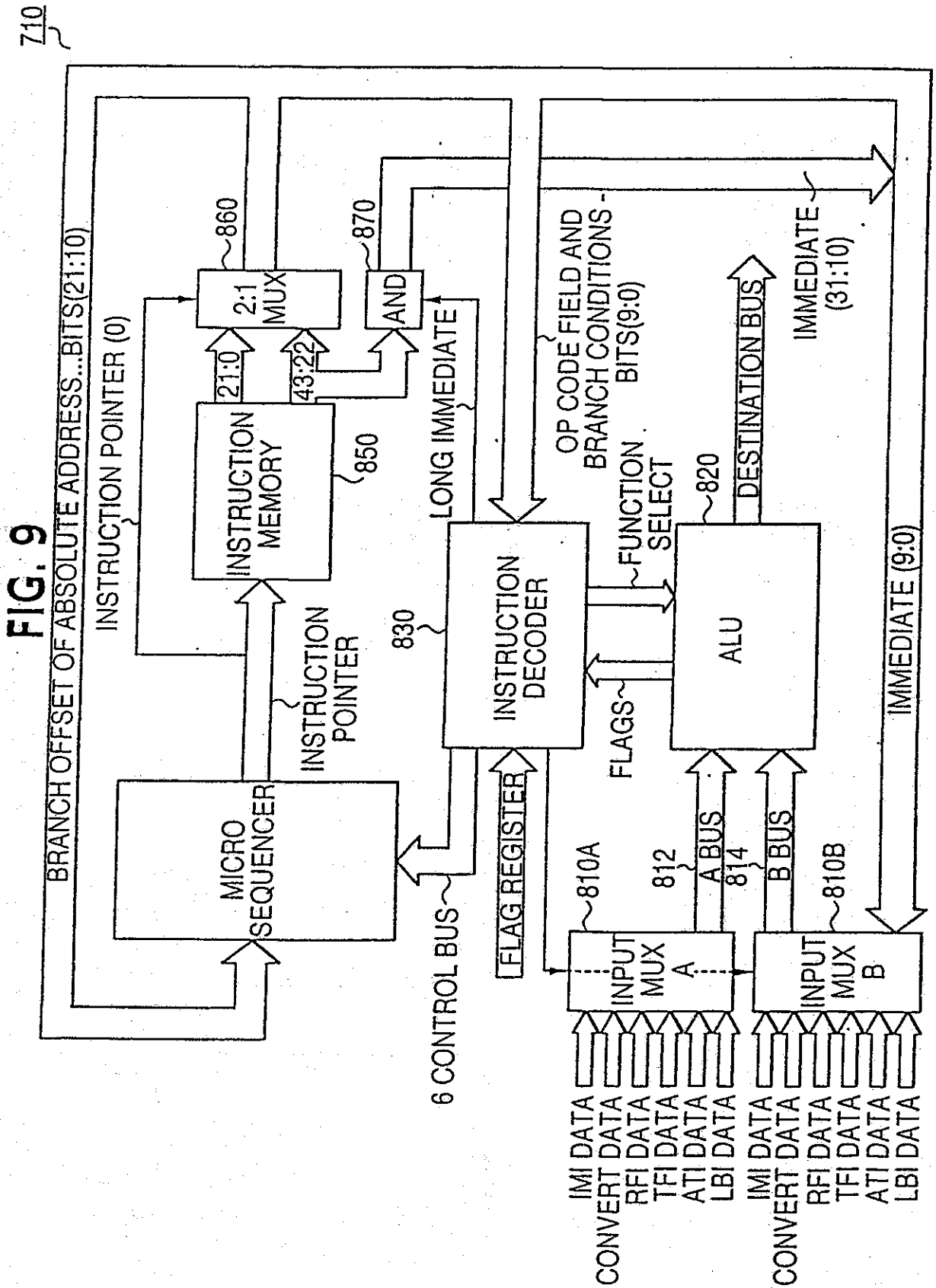

710
BRANCH OFFSET OF ABSOLUTE ADDRESS...BITS(21:10)
INSTRUCTION POINTER (0)
860
2:1 MUX
870
AND
21:0
43:22
INSTRUCTION MEMORY
850
LONG IMMEDIATE
OP CODE FIELD AND BRANCH CONDITIONS - BITS(9:0)
IMMEDIATE (31:10)
DESTINATION BUS
820
FUNCTION SELECT
INSTRUCTION DECODER
830
ALU
INSTRUCTION POINTER
MICRO SEQUENCER
6 CONTROL BUS
FLAG REGISTER
FLAGS
IMMEDIATE (9:0)
810A
812
A BUS
814
B BUS
810B
INPUT MUX A
INPUT MUX B
IMI DATA
CONVERT DATA
RFI DATA
TFI DATA
ATI DATA
LBI DATA
IMI DATA
CONVERT DATA
RFI DATA
TFI DATA
ATI DATA
LBI DATA

FIG. 10

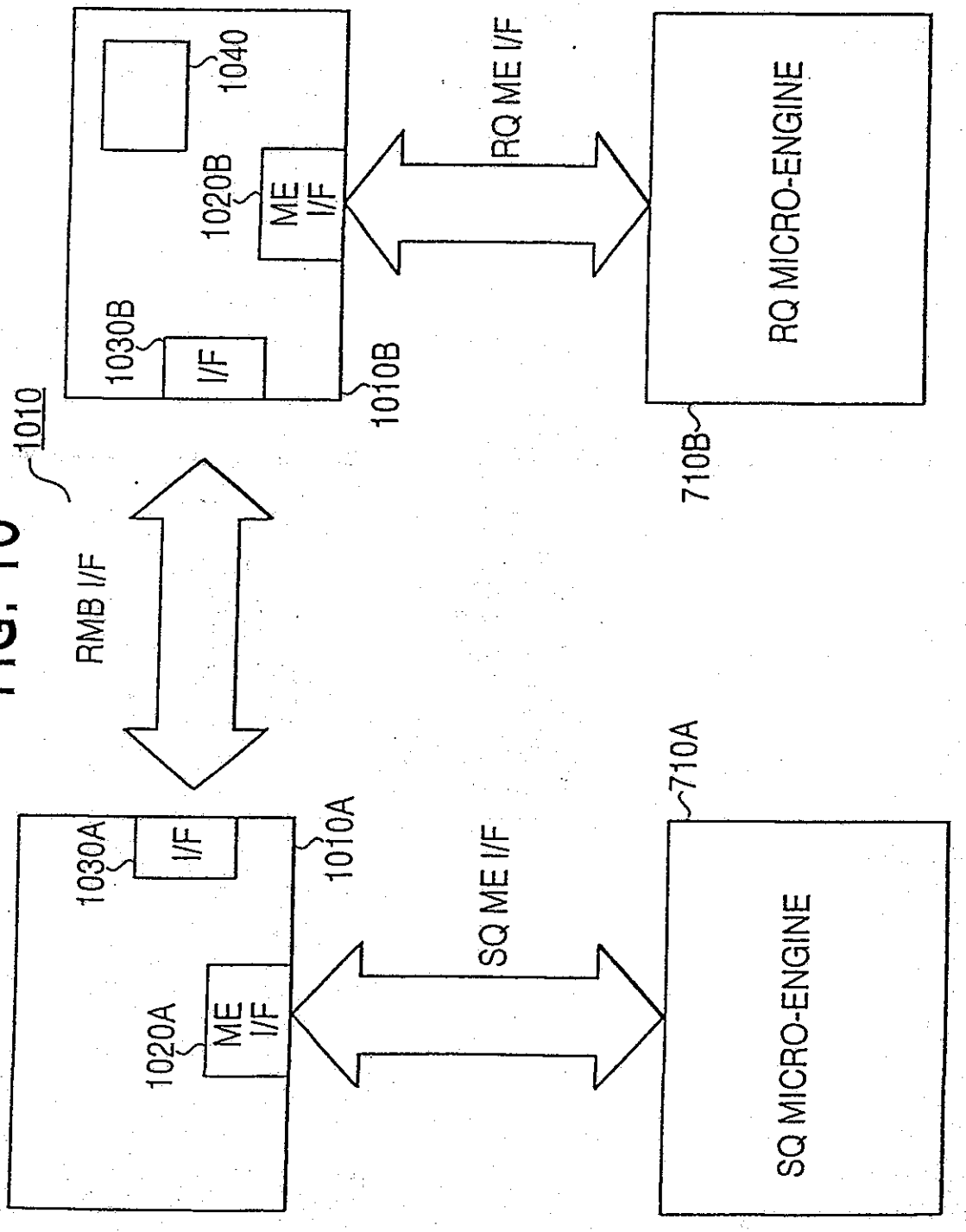

1010
RMB I/F
1010B
1030B
I/F
1020B
ME I/F
1040
RQ ME I/F
RQ MICRO-ENGINE
710B
1010A
1030A
I/F
1020A
ME I/F
SQ ME I/F
SQ MICRO-ENGINE
710A

FIG. 11

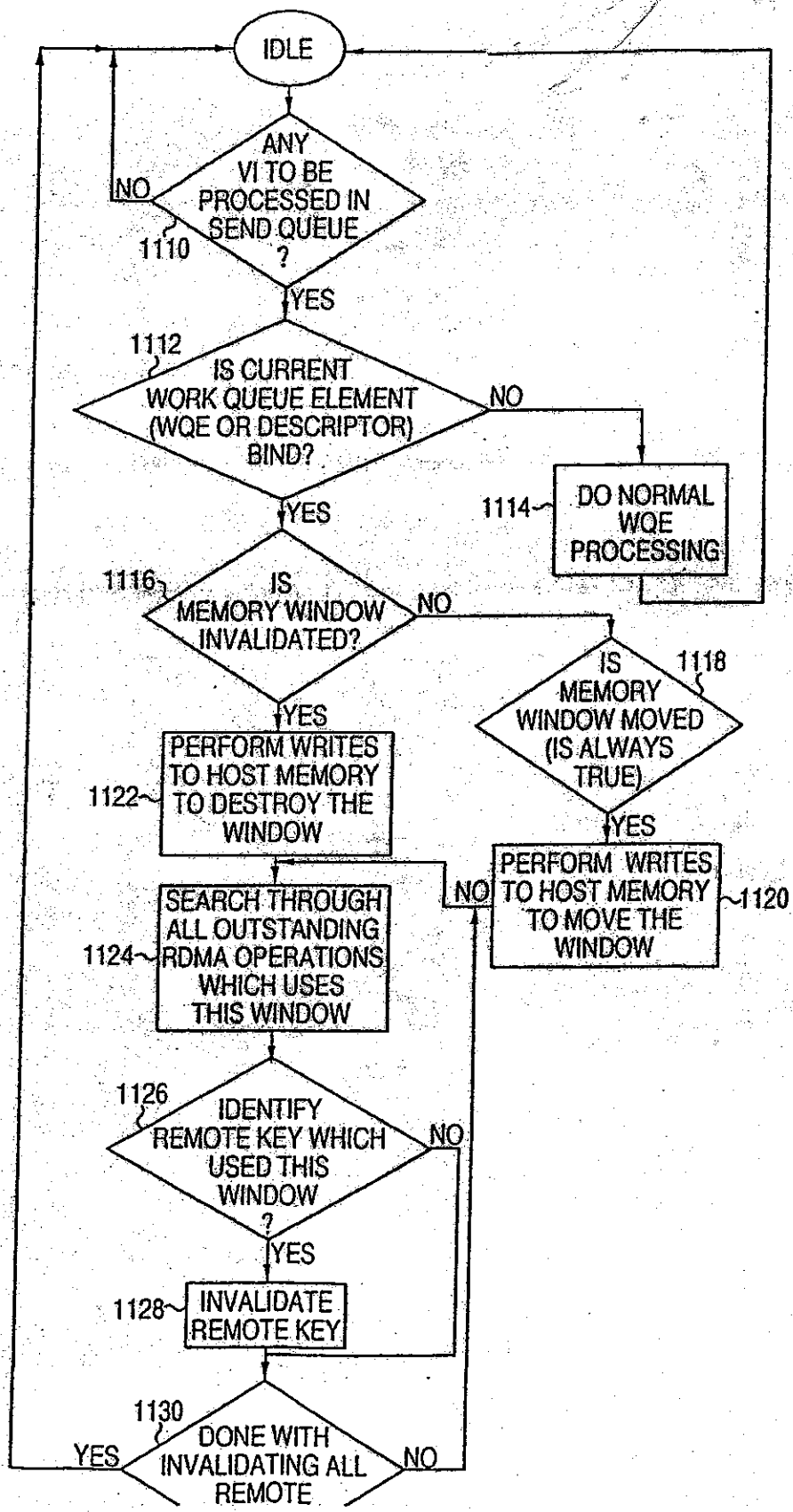
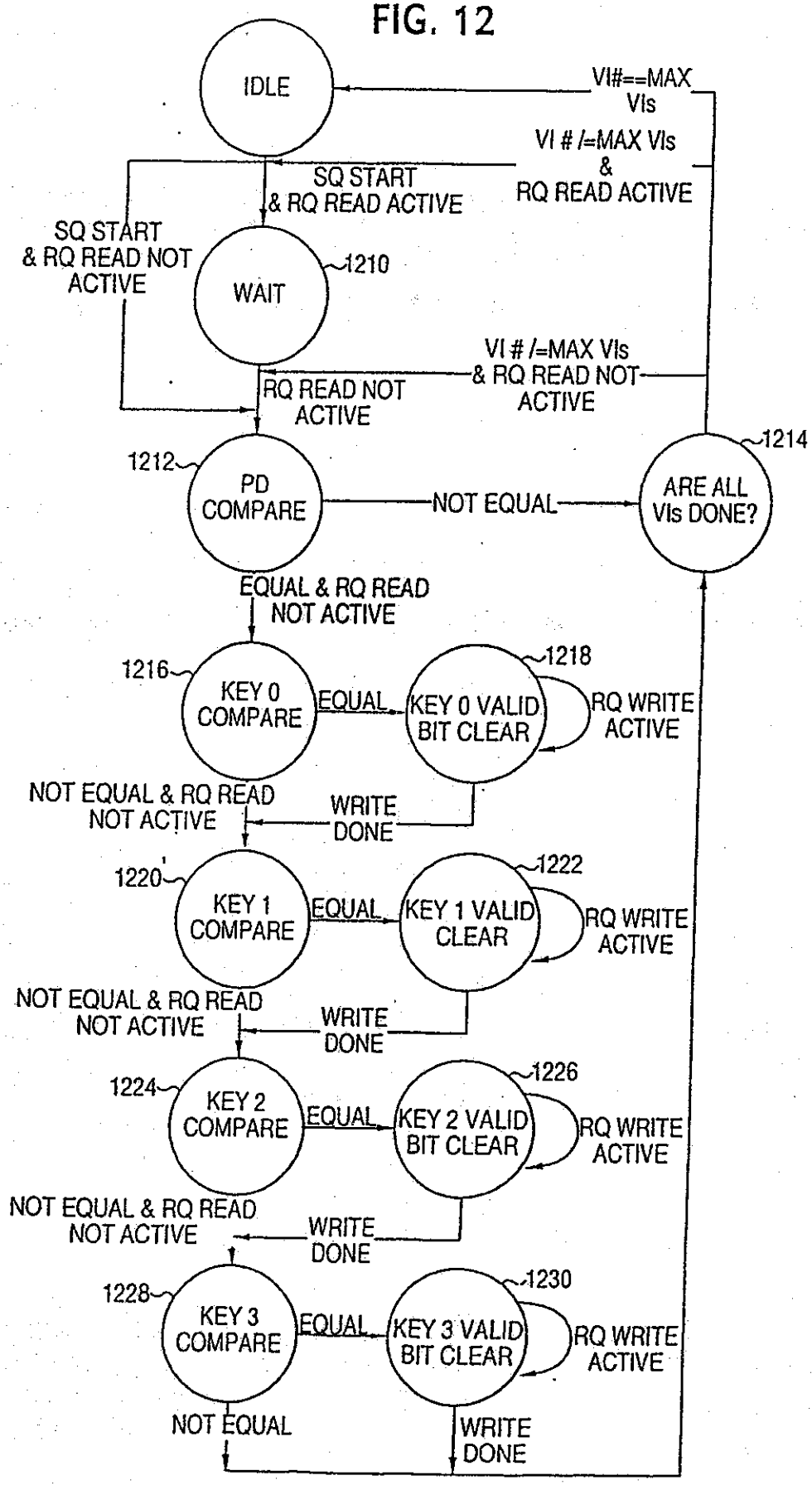

IDLE
ANY VI TO BE PROCESSED IN SEND QUEUE ?
NO
1110
YES
1112
IS CURRENT WORK QUEUE ELEMENT (WQE OR DESCRIPTOR) BIND?
NO
1114
DO NORMAL WQE PROCESSING
YES
1116
IS MEMORY WINDOW INVALIDATED?
NO
1118
IS MEMORY WINDOW MOVED (IS ALWAYS TRUE)
YES
PERFORM WRITES TO HOST MEMORY TO DESTROY THE WINDOW
1122
YES
PERFORM WRITES TO HOST MEMORY TO MOVE THE WINDOW
1120
NO
SEARCH THROUGH ALL OUTSTANDING RDMA OPERATIONS WHICH USES THIS WINDOW
1124
1126
IDENTIFY REMOTE KEY WHICH USED THIS WINDOW ?
NO
YES
1128
INVALIDATE REMOTE KEY
1130
DONE WITH INVALIDATING ALL REMOTE
YES
NO

FIG. 12


IDLE
VI#==MAX VIs
VI # /=MAX VIs & RQ READ ACTIVE
SQ START & RQ READ ACTIVE
SQ START & RQ READ NOT ACTIVE
WAIT
1210
VI # /=MAX VIs & RQ READ NOT ACTIVE
RQ READ NOT ACTIVE
1212
PD COMPARE
NOT EQUAL
ARE ALL VIs DONE?
1214
EQUAL & RQ READ NOT ACTIVE
1216
KEY 0 COMPARE
EQUAL
1218
KEY 0 VALID BIT CLEAR
RQ WRITE ACTIVE
NOT EQUAL & RQ READ NOT ACTIVE
WRITE DONE
1220
KEY 1 COMPARE
EQUAL
1222
KEY 1 VALID CLEAR
RQ WRITE ACTIVE
NOT EQUAL & RQ READ NOT ACTIVE
WRITE DONE
1224
KEY 2 COMPARE
EQUAL
1226
KEY 2 VALID BIT CLEAR
RQ WRITE ACTIVE
NOT EQUAL & RQ READ NOT ACTIVE
WRITE DONE
1228
KEY 3 COMPARE
EQUAL
1230
KEY 3 VALID BIT CLEAR
RQ WRITE ACTIVE
NOT EQUAL
WRITE DONE

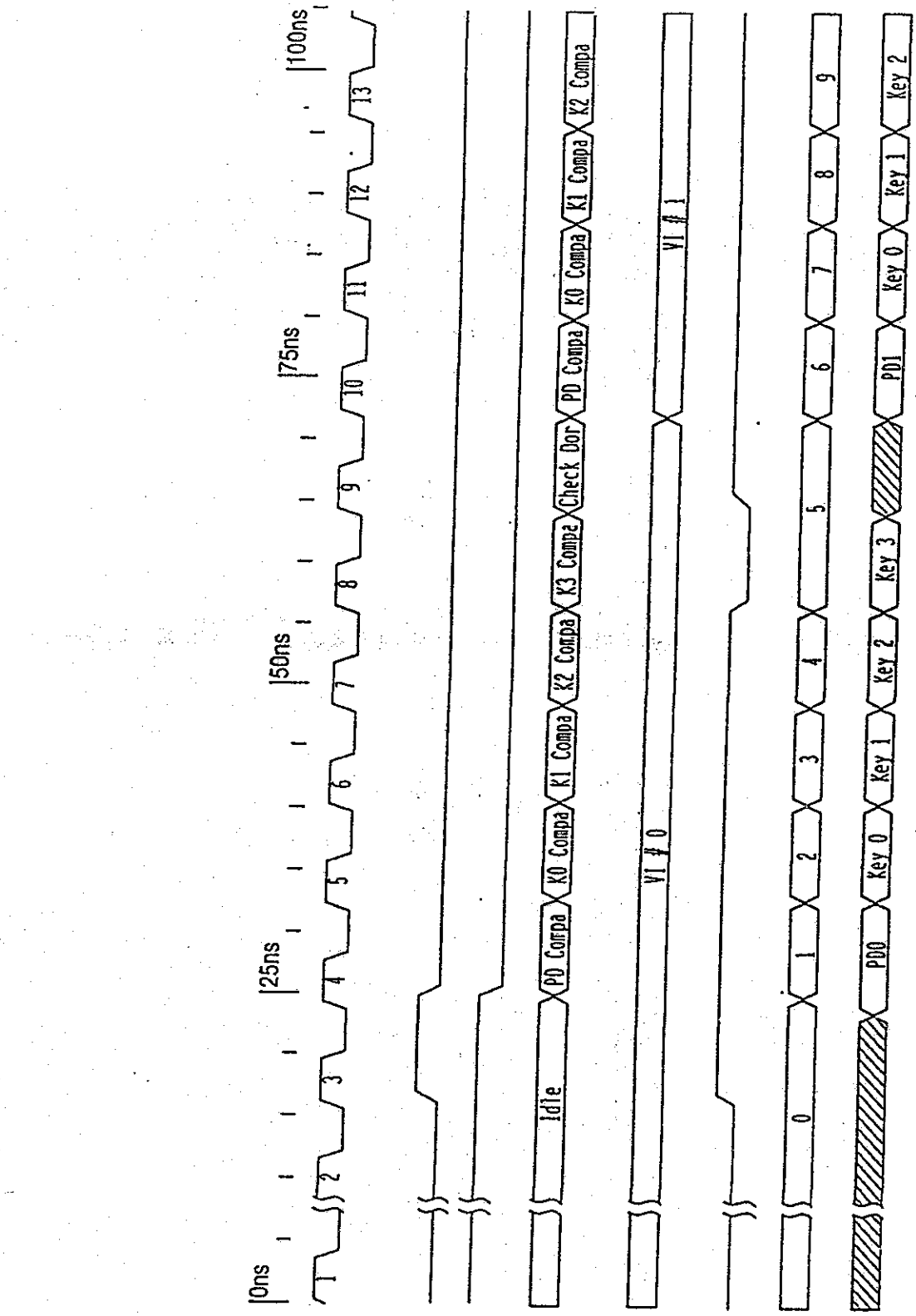


FIG. 13A cclk

FIG. 13B SQ start

FIG. 13C Done to SQ

FIG. 13D cur_state

FIG. 13E VI#

FIG. 13F rmb_mem_re

FIG. 13G rmb_mem_rd_addr

FIG. 13H rmb_mem_rd_data

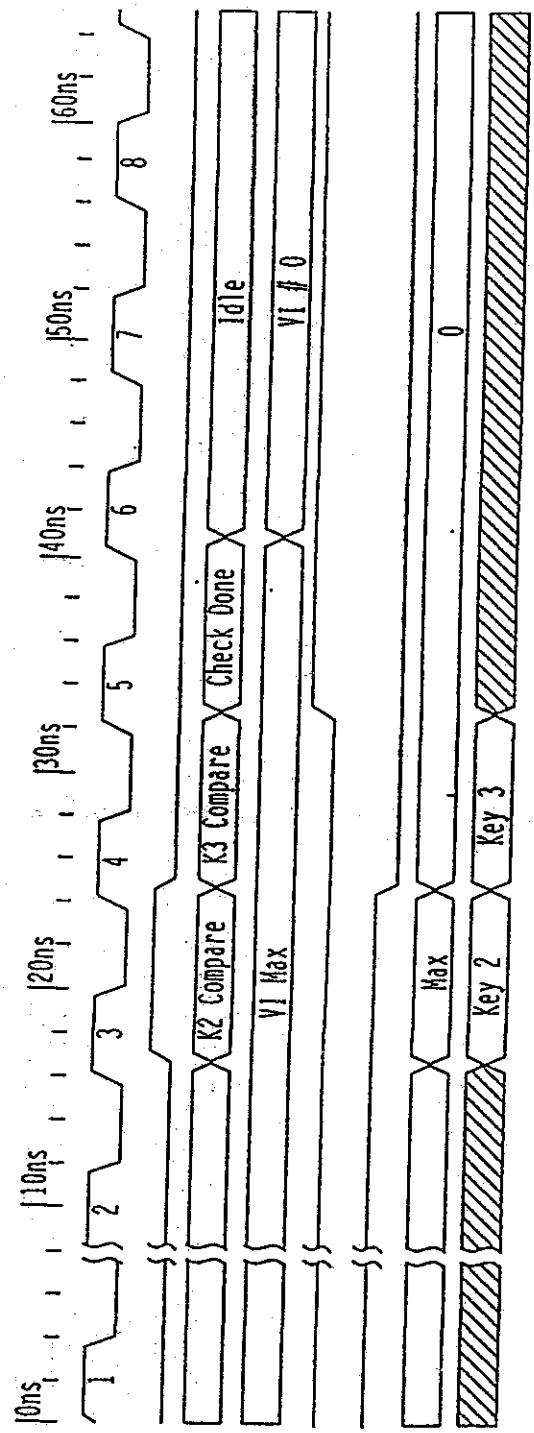


FIG. 14A
FIG. 14B
FIG. 14C
FIG. 14D
FIG. 14E
FIG. 14F
FIG. 14G
FIG. 14H

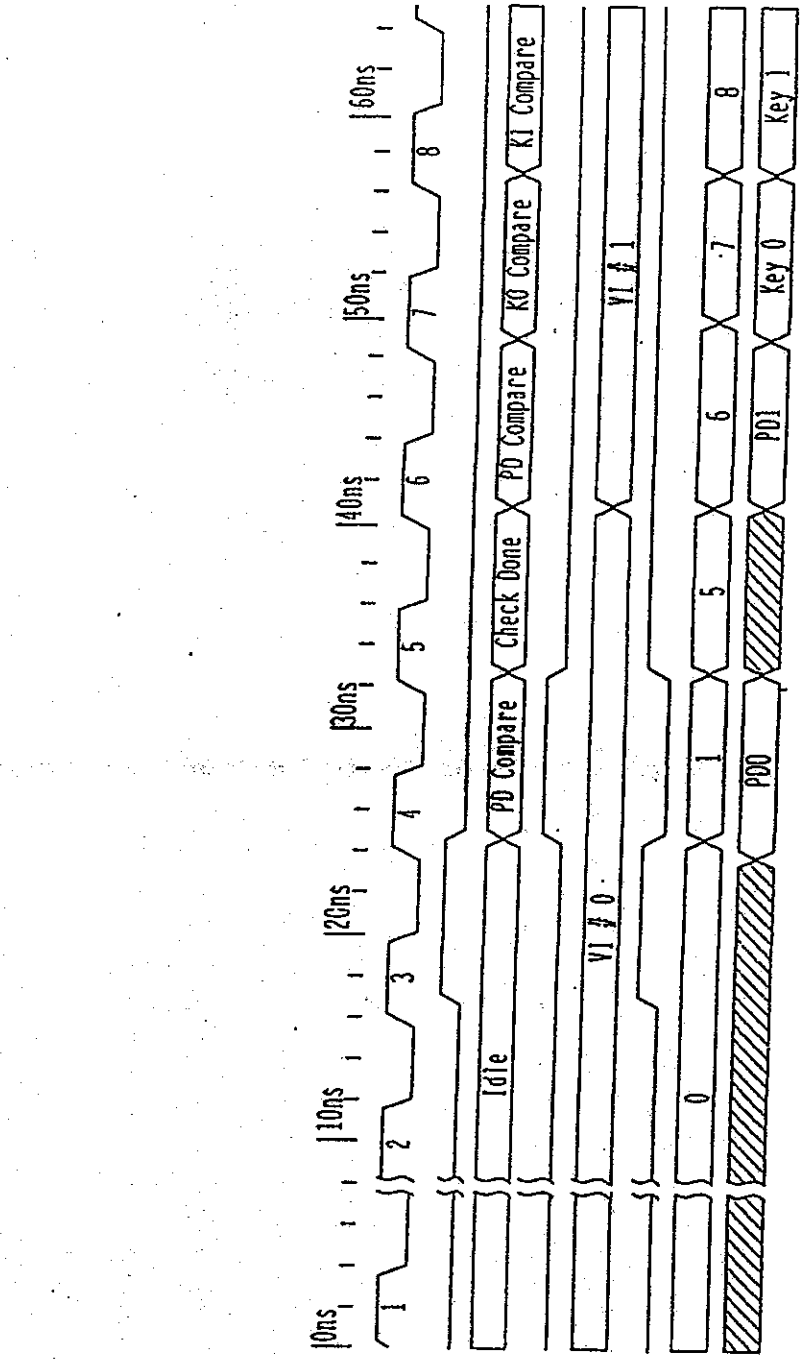


FIG. 15A
FIG. 15B
FIG. 15C
FIG. 15D
FIG. 15E
FIG. 15F
FIG. 15G
FIG. 15H

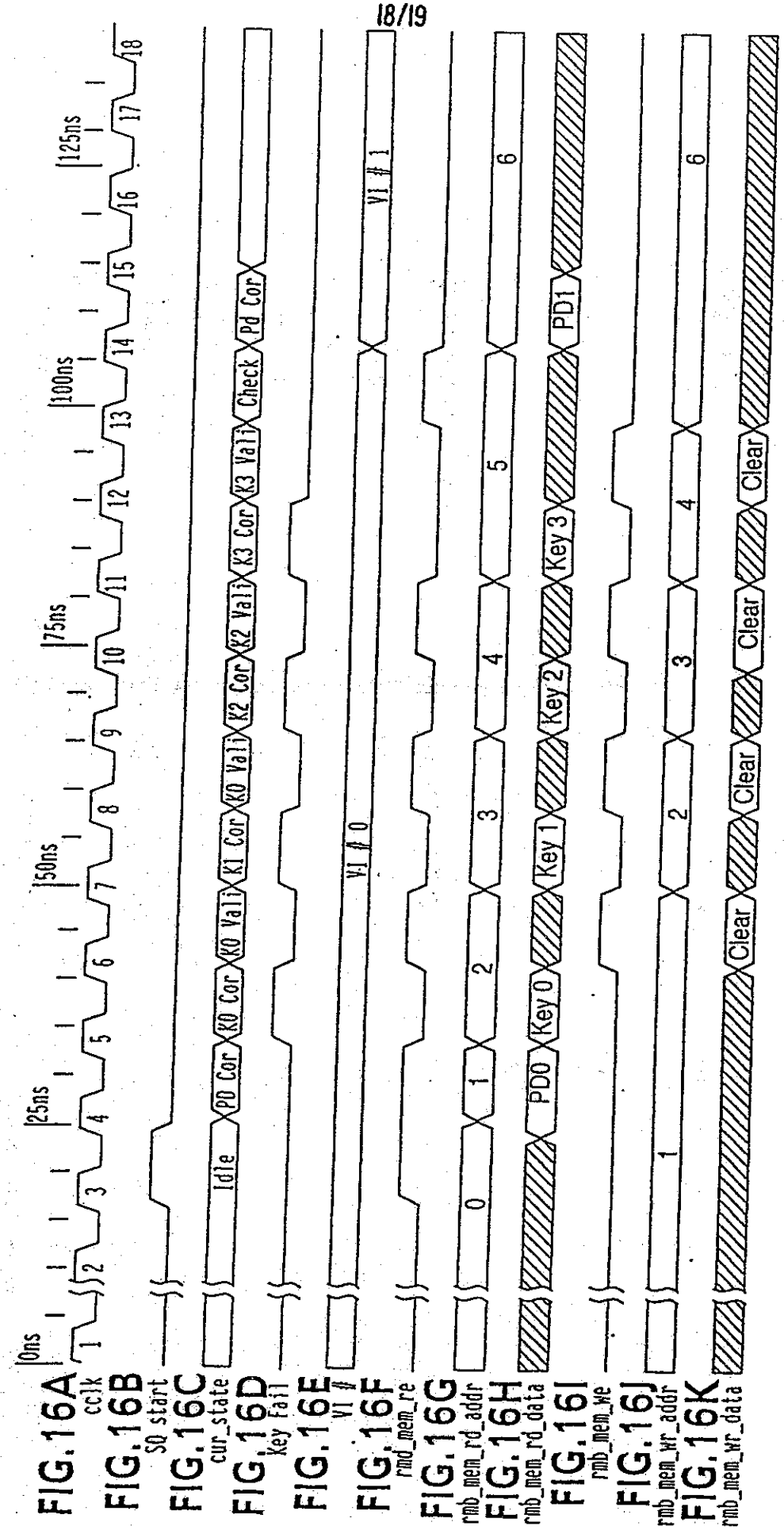


FIG. 16A

FIG. 16B

FIG. 16C

FIG. 16D

FIG. 16E

FIG. 16F

FIG. 16G

FIG. 16H

FIG. 16I

FIG. 16J

FIG. 16K

FIG.17A cclk

FIG.17B SQ start

FIG.17C RQ_me-src_addr

FIG.17D RQ_me_wr

FIG.17E cur_state

FIG.17F key fail

FIG.17G V1#

FIG.17H rmb_mem_re

FIG.17I rmb_mem_rd_addr

FIG.17J rmb_mem_rd_data

FIG.17K rmb_mem_we

FIG.17L rmb_mem_wr_addr

FIG.17M rmb_mem_wr_data