

**METHOD AND APPARATUS FOR CONVERTING
AN ANALOG SIGNAL INTO DIGITAL FORMAT**

FIELD OF THE INVENTION

5 The present invention relates to a method and system for converting an analog signal into digital format, and more particularly, to a low cost, easy to manufacture analog to digital converter.

BACKGROUND AND SUMMARY OF THE INVENTION

10 Analog to digital conversion is widespread. In one application to digital radios, a high speed analog to digital converter is required to convert speech and other related signals into digital format. In analog (FM) radios, however, the analog to digital conversion requirements are typically less rigorous, (1) because the speech is not digitized, and
15 (2) because the analog signals that are digitized, e.g., signal strength measurements, battery voltage measurements, power amplifier current measurements, etc., do not necessarily have to be digitized at high speed. In fact, the radio microprocessor may monitor received signal strength, battery voltage, power amplifier current, etc. only once
20 every several milliseconds.

To make such a slower speed analog to digital converter for an analog radio, a single analog to digital converter could be coupled to an analog multiplexer that selects one of the various analog signals to be digitized. For example, an eight input analog multiplexer can have its

5 eight inputs allocated as follows: (1) a reference voltage input (V_{ref}), (2) measured received signal strength, (3) measured battery voltage, (4) measured power amplifier current, (5) sensed temperature, (6) the reflected transmitter power, (7) the transmitter voltage controlled oscillator (VCO) voltage, and (8) zero reference voltage (e.g., ground).

10 The multiplexer may then select one input signal to be connected to a grounded capacitor charging it to the voltage of the selected signal. To convert that signal into a digital value, a smaller capacitor connected to the input capacitor may then be used to cyclically remove increments of charge from the input capacitor. The number of

15 increments of charge required to return the input capacitor to ground potential as detected by a comparator may be stored in a counter. By comparing the counter output obtained when converting the selected voltage with the counter output obtained by converting ground potential or the reference voltage such as V_{ref} during an occasional

20 calibration, the digital value of the input analog signal may be determined.

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One drawback with such an arrangement is that it requires a comparator which can detect zero voltage. Conventional, inexpensive comparators do not accurately detect when an input voltage reaches a zero voltage reference because at zero voltage, no current is flowing
5 through the comparator amplifiers. Instead, it is much easier for conventional comparators to compare with a reference voltage which is on the order of halfway between zero voltage and the reference voltage (V_{ref}), i.e., $V_{ref}/2$. One approach to making a zero voltage detector is to construct a comparator that uses a negative power supply. However,
10 an additional negative power supply or an additional power converter circuit is a significant drawback in such applications where cost and weight are a significant factor as they are in portable, hand-held radios.

15 Another consideration when implementing the analog to digital conversion arrangement described above is the particular type of element used to switch the smaller capacitor in and out of series with the input capacitor. Bipolar junction transistor and diode switches are very sensitive to temperature, therefore making calibration quite
20 difficult. Consequently, it is uncertain what particular digital output will be generated in response to a given input voltage level. Therefore,

continuing calibration techniques would have to be used slowing down the analog to digital conversion process as well as adding complexity and expense. For example, it may be necessary to measure on a relatively frequent basis, the number of pulses required to charge or
5 discharge a standard reference voltage before each input voltage is measured to calibrate the selected input voltage by dividing it by the total number of pulses and multiplying it by the reference voltage. Such division and multiplication operations in practice are sufficiently complicated to implement in a binary-based data processing system
10 that they slow down the conversion operation considerably. Bipolar junction transistors are also relatively expensive because most semiconductor foundries manufacture transistors using metal oxide on silicon (MOS) processes.

15 It is an object of the present invention to construct an analog to digital converter which overcomes the problems noted above.

 It is a particular object of the present invention to employ a switching arrangement which uses only MOS switches to remove
20 increments of charge from or add increments of charge to an input capacitor.

It is an object of the present invention to provide a dynamic comparator which effectively compares an input signal to a zero voltage reference without requiring a negative power supply or a power converter to effectively perform that zero voltage detection.

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It is also an object of the present invention to provide a low cost analog to digital converter that incrementally removes or adds charge from an input capacitor using only field effect transistor (FET) switches and using a conventional comparator which compares an
10 input signal with a non-zero threshold voltage.

These objects and others are accomplished with an analog to digital converter that includes a first capacitor connected at a first terminal to an input analog signal for a time sufficient to charge the
15 capacitor in accordance with the current voltage level of that analog signal. Electronic circuitry alternately connects a second capacitor between the first capacitor and a power supply to remove increments of charge from the first capacitor until the first capacitor is discharged. The number of removed increments of charge associated with
20 discharging the first capacitor is used to generate a digital value corresponding to the current voltage of the analog signal. An analog

multiplexer may be employed for receiving multiple analog signals and selecting one of the received analog signals for connection to the first capacitor. The multiplexer then disconnects the analog signal from the first capacitor after the first capacitor charges to a level commensurate
5 with the current voltage level of the selected analog signal. A comparator detects when the voltage across the first capacitor is zero, and the output of the comparator is used to trigger generation of the corresponding digital value.

10 Preferably, the switching circuitry that alternately connects the first capacitor to ground and then to the power supply includes first and second pairs of field effect transistor switches. The first pair of FET switches connects between ground and the power supply to charge the second capacitor. The second pair of FET switches connects
15 the second capacitor between the first terminal of the capacitor and ground to remove increments of charge from the first capacitor.

In another embodiment of an analog to digital converter in accordance with the present invention, control circuitry connects to an
20 input capacitor to store an analog input capacitor. Dynamic detection circuitry includes a comparator which ultimately provides a zero

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voltage level signal to the control circuitry indicating when the input capacitor has discharged to a zero voltage level. Significantly however, the dynamic detection circuitry does not employ a comparator that requires a negative power supply to detect a zero voltage level.

- 5 Instead, the dynamic detection circuitry processes the input signal stored on the input capacitor such that when that input signal is detected in a conventional comparator as being equal to or greater than a non-zero threshold voltage, the zero voltage level signal is sent to the control circuit.

10

- The dynamic detection circuitry is connected through a pump capacitor to a pumping output signal of the control circuit. The control circuit alternately charges and discharges the pump capacitor using the pumping output signal and discharges the input capacitor by an
- 15 increment of charge after each charge/discharge cycle of the pump capacitor until the dynamic detection circuitry indicates that the input capacitor is discharged. The total number of incremental charge/discharge cycles of the input capacitor is used to generate a digital value corresponding to the input analog voltage.

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Preferably, the dynamic detection circuitry includes first and second field effect transistors (FETs) having a common source electrode connected to the pump capacitor. The gate electrode of the first FET is connected to ground, and the gate electrode of the second FET is connected to the input capacitor. The drain electrodes of the first and second FETs are connected to a power supply with the drain electrode of the second FET also being connected to an input terminal of the comparator. When the pumping signal is in a first logic state, current flows in a first direction from either or both of the first and second FETs through the common source electrodes and the pump capacitor thereby discharging it.

The FETs are preferably formed in a "P-well" semiconductor device readily manufactured using conventional CMOS processes. As a result, the common source connection of the first and second FETs is connected to ground through a diode formed at the P-well and N-substrate interface. When the pumping signal is in a second logic state, current flows in a second direction opposite the first direction through the diode thereby charging the pump capacitor.

The dynamic detection circuitry in this second embodiment of the present invention can be employed advantageously and independently in a method to detect when an input signal reaches a zero voltage level. A first capacitor is charged in accordance with the voltage level of the input signal. A second capacitor is then alternately charged during a first time interval and discharged during a second time interval. During the first time interval, a portion of charge stored on the first capacitor is discharged. During the second time interval, the current voltage across the first capacitor is detected and processed. The processed signal is compared with a non-zero reference voltage. The current voltage across the capacitor is indicated as having reached a zero voltage level when the proposed signal is the same as or greater than the non-zero voltage of the reference voltage. Advantageously, this zero voltage detection method does not require a negative power supply for the comparator to detect zero. In fact, the comparator threshold may be set halfway between zero voltage and a power supply voltage.

In accordance with another preferred embodiment of the present invention, an analog to digital converter includes a first capacitor connected at a first terminal to an analog signal for a time to charge

the capacitor in accordance with the current voltage level of the analog signal. A comparator is connected at one input to the capacitor and another input to a non-zero reference voltage for generating (1) a first signal when the voltage across the first capacitor is greater than the reference voltage, (2) a second signal when the voltage across the first capacitor is less than the non-zero reference voltage, and (3) a third signal when the voltage across the first capacitor is the same as the non-zero reference voltage. Electronic control circuitry supplies increments of charge to the first capacitor when the voltage across the first capacitor is less than the non-zero voltage until it is the same as the non-zero reference voltage. Alternatively, increments of charge are removed from the first capacitor when the voltage across the first capacitor is greater than the non-zero reference voltage until it is the same as the non-zero reference voltage. The number of charge increments or decrements is counted to generate a digital value corresponding to the current voltage level of the analog signal.

A second capacitor stores the increment or decrement of charge added to or removed from the first capacitor. A plurality of MOS FET switches are connected to the second capacitor and alternately switch the second capacitor between various states depending on the output

of the comparator. Thus, this embodiment of the present invention provides a low cost analog to digital converter formed on a semiconductor substrate using metal-oxide-silicon (MOS) technology which may be integrated with other digital MOS circuitry on the same
5 semiconductor substrate that does not require a comparator that detects a zero voltage level.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will be
10 more clearly understood from the following description taken in conjunction with the accompanying drawings in which:

Figs. 1(A) and 1(B) are schematic diagrams of a first preferred embodiment of the present invention;

Fig. 2 is a schematic diagram of the present invention in
15 accordance with a second preferred embodiment; and

Fig. 3 is a schematic diagram of a third preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

20 In the following description, for purposes of explanation and not limitation, specific details are set forth, such as particular circuits,

circuit components, techniques, etc. in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced in other embodiments that depart from these specific circuit details. In other instances, detailed descriptions of well known methodologies, devices, manufacturing processes, and circuits are omitted so as not to obscure the description of the present invention with unnecessary detail.

10 Fig. 1(A) illustrates in schematic form a preferred embodiment of an analog to digital converter 100 in accordance with the present invention. An analog multiplexer 110 which may be comprised of a plurality of transmission gates enabled by a select signal from controller 120 receives at its input terminals a plurality of both analog
15 voltage inputs, a positive potential V_{cc} , and a zero volts reference potential hereafter referred to as "ground." In accordance with the select signal from controller 120, the analog multiplexer connects one of the inputs to the multiplexer 110 to input capacitor 130 connected at one end to the multiplexer and at the other end to ground. A
20 comparator 140 includes a first input terminal connected to ground, i.e., zero volts, and a second input terminal connected to the first

terminal of the input capacitor 130. In this arrangement,
comparator 140 detects a zero voltage, either by using a negative
supply or a convention circuit of appropriate sophistication. The
comparator 140 output is connected to a digital counter 160 and
5 effectively generates a STOP command when zero volts is detected
across capacitor 130.

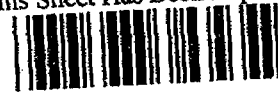
A second capacitor 220 (referred to hereafter as the "pumping"
capacitor) is shown enclosed in the dashed block labeled switching
10 circuit 150. Switching circuit includes a plurality of switches 200, 205,
210, and 215 (shown as nodes) which function in pairs to connect the
input capacitor 130 through pumping capacitor 220 to ground or to
connect pumping capacitor to the V_{cc} . More specifically, switches 200
and 215 function as a first switch pair, and switches 205 and 210
15 function as a second switch pair.

When the second switch pair 205, 210 is activated to connect the
pumping capacitor 220 to V_{cc} , pumping capacitor 220 is charged to its
full capacity. The value of capacitor 220 zero is preferably
20 considerably smaller than input capacitor 130 since greater resolution
is achieved in the incremental removal of charge from input

capacitor 130. In one example, to implement an 8-bit analog to digital converter (an analog to digital converter having a resolution of 8-bits), the input capacitor value should be 256 times the capacitor value of the pumping capacitor 220. In this example, counter 160 should be at
5 least an 8-bit counter. Preferably, a fully charged input capacitor 130 should be capable of being discharged in this example in 256 discharge cycles.

Switch pair 205, 210 charges pumping capacitor 220 with a
10 positive polarity on the right plate connected to switch node 210 and a negative polarity on the left plate connected to switch node 205. As a result of this polarity, when input capacitor 130 is connected via switch pair 200, 215 in series with capacitor 220, capacitor 130 (which is charged to the opposite polarity) discharges by an amount in
15 accordance with the charge stored on pumping capacitor 220.

A counter 160 is connected to receive a start signal and a clock signal that may be generated by controller 120. Of course, the clock signal can be generated from a clock source independent of
20 controller 120. The counting output terminal 180 of counter 160 is in this example embodiment the switch control signaling which controls



the activation of the first and second switch pairs 200, 215 and 205.
210. As the counter transitions from high to low, one set of switch
pairs is activated, and as the counter transitions from low to high the
other switch pair is activated. Once the counter is stopped, it
5 generates a digital readout corresponding to the analog voltage
initially stored on input capacitor 130.

In operation, controller 120 enables, via a select signal, one of
the transmission gates in the analog multiplexer 110 to connect one of
10 the voltage inputs to input capacitor 120. Thereafter, the voltage
input is removed, and the controller 120 transmits a start signal to
counter 160. The counter then counts clock signals generating an
oscillating counter output control signal at terminal 180 for selectively
activating the switch pairs 200, 215 and 205, 210. The initial logic
15 level of the counter control signal activates switches 205 and 210 to
connect pumping capacitor 220 to V_{cc} . When the counter control signal
switches to an opposite logic level with pumping capacitor 220 having
been charged, the first switch pair 205, 210 is deactivated and the
second switch pair 200, 215 is activated. Since the polarities of the
20 input capacitor 130 and pumping capacitor 220 are opposite, current
flows from input capacitor 130 through pumping capacitor 220 to

ground discharging input capacitor by an incremental amount corresponding to the charge initially stored across pumping capacitor 220. When the counter output changes back to the initial logic level, the incremental discharge of input capacitor is completed,
5 the second pair of switches 200, 215 is deactivated, and the first pair of switches 205, 210 is again activated to recharge the pumping capacitor 220.

This alternating charge/discharge cycle continues in accordance
10 with the counter control signal with the counter keeping track of the number of clock cycles accumulated since the counter was started. Comparator 140 compares the voltage across input capacitor 130. When the capacitor 130 is substantially discharged, the voltage across capacitor 130 is substantially zero. Such substantially zero voltage is
15 received at the first input terminal of comparator 140 and compared with ground potential. Comparator 140 then generates a "stop" output signal to stop counter 160 if the voltage across capacitor 130 is substantially zero. The counter 160 then outputs the accumulated count value which corresponds to a digital value for the analog input
20 voltage. The larger the input voltage, the larger the amount of charge stored across input capacitor 130, and the greater the number of

increments needed to discharge the input capacitor 130. Accordingly, a larger count value represents a larger amplitude analog signal.

Fig. 1(B) illustrates one example and preferred implementation of the switches 200, 205, 210, 215 employed in switching circuit 150. Specifically, each switch includes a complementary pair of N-type and P-type, insulated gate, field effect transistors (FETs) connected at their respective drains and sources and is termed a "bilateral switch." Each FET has a gate control signal Q or $\bar{Q}$ which controls whether the FET conducts or does not conduct current. For example, the second pair of switches 200 and 215 receive a control signal of logic level Q from counter 160 at the gates of their respective N-type FETs, and an opposite logic state signal $\bar{Q}$ at the gates of their respective P-type FETs. When Q equals a high logic level "1" (e.g., 5 volts), the N-type FETs conduct. Similarly, at the same time, the opposite logic level "0" (corresponding to zero volts) is applied to the gates of P-type FETs which then also conduct. The combined currents flowing through the N-type and P-type FETs result in a near perfect switch which passes all of the current, operates over the full voltage range $0-V_{cc}$, and provides cancellation of switching glitches due to gate capacitance.

Switches 205 and 210 have gate inputs of the opposite polarity. In other words, the control signal having a logic level of $\bar{Q}$ is applied to the gate terminal of the N-type transistor, and the control signal having a logic level of Q is applied to the gate input of the P-type FET in each complementary switch 205 and 210. When $Q = 0$ and $\bar{Q} = 1$, switches 205 and 210 conduct. When $Q = 1$ and $\bar{Q} = 0$, switches 200 and 215 conduct. While complementary FET switches are preferred, simple FET switches may also be used satisfactorily.

One of the drawbacks with the embodiments shown in Figs. 1(A) and 1(B) is the need for a zero voltage level comparator, i.e., comparator 140. As described above, zero-crossing comparators traditionally require a negative supply which requires power conversion circuitry increasing the part count, weight, and cost of the ultimate device, e.g., a radio, or alternatively employ a level of circuit sophistication which also increases cost as well as power consumption. The analog to digital converter shown in Fig. 2 employs dynamic conversion circuitry which permits detection of zero voltage across input capacitor 130 using a conventional comparator 300 that compares an input signal with a non-zero reference voltage, e.g., $V_{cc}/2$.

A reference of $V_{cc}/2$ is preferred because that is a voltage in the center of the range in which conventional comparators are designed to detect.

As in the embodiment in Fig. 1, an analog multiplexer 110
5 receives multiple inputs including ground and a reference voltage V_{cc} .
A select signal from counter, control, and discharge circuitry 230
enables one of the transmission gates in multiplexer 110 which
charges input capacitor 130 to a level commensurate with the current
voltage level of the selected input signal. Circuitry 230 receives as
10 inputs a clock signal and an output from comparator 300.
Circuitry 230 generates a digital readout corresponding to the analog
voltage level of the selected input signal, a periodic discharge signal to
input capacitor 130, and an oscillating counter control signal referred
to hereafter as a pump signal. The pump signal is connected through
15 resistor 235 to pumping capacitor 220 which is also connected to the
common source connection of FETs 260 and 265. FETs 260 and 265
are N-type FETs which are formed in a "P-well" 250 of P-type
semiconductor material diffused into an N-type substrate 245. The
substrate 245 is connected to ground via metallized ring 240. The gate
20 terminal of N-type FET 260 is connected to ground, and the gate
terminal of N-type FET 260 is connected to the input capacitor 130.

The drains of FETs 260 and 265 are connected preferably (although not necessarily) to a current mirror 260. Current mirror 260 includes two P-type FETs 285 and 290 connect at their respective gates. The sources of P-type transistors 285 and 290 are connected to V_{cc} , and their drains are connected to the drains of FET 260 and FET 265, respectively. The common gate connection between FETs 285 and 290 also connects to the drain of FET 290. The drain of FET 285 is connected at node 280 as the input to comparator 300 for comparison with a non-zero reference voltage which in this example embodiment may be $V_{cc}/2$.

In operation, counter, control, and discharge circuitry 230 controls the analog multiplexer 110 to select a voltage input which charges input capacitor 130 to its current voltage level. Circuitry 230 then controls the analog multiplexer 110 to disconnect the input capacitor 130 from all inputs. The pump output (which may for example correspond to the oscillating clock signal) is applied to pump capacitor 220. Initially, the pump signal switches from a zero level voltage to a high level voltage (0 to 1) which charges pumping capacitor 220 through current limiting resistor 235, the common source connection, and the P-N junction diode (indicated symbolically

at 255) formed at the interface of the P-well 250 and the N-type substrate 245 to ground. During this cycle, the gate of transistor 265 is connected to ground, and therefore, FET 265 is turned off and does not conduct. Transistor 260 may not be cut off because although its source voltage is at the nominal forward bias voltage of the P-well diode 255 of 0.7 volts, its gate voltage is equal to the input voltage on capacitor 130 which may be greater. However, since transistor 265 does not conduct during this cycle, no current flows through current mirror transistors 285 and 290, and hence, no current can flow through transistor 260. Node 280 is therefore pulled low, i.e., below $V_{cc}/2$ in these circumstances, indicating that the voltage on capacitor 130 is greater than zero.

When the pump signal switches from a high to a low voltage level, the left plate of pump capacitor 220 connected to resistor 235 is pulled to zero volts which (because the voltage across capacitor 220 cannot change instantaneously) forces the right plate of capacitor 220 to a temporary negative voltage. That temporary negative voltage is applied to the common source connection of transistors 260 and 265, and as a result, both transistors can now conduct. Even transistor 265, whose gate is connected to ground, can conduct because

if the voltage applied to the source of FET 265 is negative, the voltage between the gate and source is positive which "turns-on" transistor 265.

5 If the voltage across capacitor 130 is larger than zero, a larger gate voltage is applied to transistor 260 than the gate voltage applied to transistor 265. As a result, more current is "pulled" through transistor 260 than is pulled through transistor 265. At the common source, the currents join to flow through capacitor 220 and dissipating
10 resistor 235. As long as the gate voltage of transistor 260 connected to the input capacitor 130 is greater than the zero gate voltage applied to transistor 265, transistor 260 will conduct more current than transistor 265.

15 The current flowing in transistor 265 is "mirrored" through transistor 285. Since transistor 285 is an identical P-type transistor with both gate and source connected to the same points as the gate and source of transistor 290, an identical current flows into the drain of transistor 285 which is connected to node 280. Thus, the current
20 mirror 260 "repeats" the drain current of transistor 265 into node 280. At the same time, current through transistor 285 is "pulling" the

voltage at node 280 up towards the voltage supply V_{cc} while the current through transistor 260 is "pulling" the voltage at node 280 down. The larger current "wins," and the voltage at node 280 either falls or rises.

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As long as the gate of transistor 260 is larger than zero, indicating that the input capacitor 130 is not fully discharged, the voltage at node 280 will be pulled down below the threshold reference voltage $V_{th}/2$ detected by comparator 300. During the time period

10 when the pump output is at a low level, the output from comparator 300 is read by the counter control and discharge circuitry 230. When comparator 300 indicates to circuitry 230 that the voltage at node 280 is less than $V_{th}/2$, (during the low level period of the pump signal), circuitry 230 applies an incremental discharge pulse

15 to input capacitor 130 to remove a single increment of charge. The counter keeps track of the total number of increments of charge removed from input capacitor 130 until the voltage across capacitor 130 is zero. When that occurs, the currents splitting between transistors 260 and 265 equalize which causes the potential at

20 node 280 to rise in voltage until it exceeds the $V_{th}/2$ threshold detected by comparator 300. The comparator output signal applied to counter,



control, and discharge circuitry 230 stops the counter as well as the cyclical application of discharge pulses to input capacitor 130. The final count is output at the digital readout.

5 This embodiment of the invention provides an inexpensive analog to digital converter which employs a conventional, non-zero level detecting comparator 300 and uses FET switches suitable for integration on a single chip along with the counter, control, and discharge circuitry 230, etc. It also provides an advantageous dynamic
10 zero crossing comparator that does not need a negative supply, and that may be used in a variety of different applications. The signal to be compared with zero is applied to charge up input capacitor 130, and the pump signal is thereafter applied through pump capacitor 220 to transistors 260 and 265. The pumping action applied to
15 transistors 260 and 265 coupled with the current mirror 260 effectively shifts the level of the input voltage. Consequently, when the voltage at node 280 exceeds the non-zero comparator threshold, the output of comparator 300 indicates a zero voltage input. Although transistors 290 and 295 have been shown as preferred elements for
20 performing the current mirror function, other circuit components could also perform this function as well, such as matched drainload resistors.

The use of a current mirror however provides higher voltage gain and thus more accurate zero-crossing detection.

Another preferred embodiment of the present invention is now
5 described in conjunction with Fig. 3. Fig. 3 shows a simpler
comparator circuit that permits comparison to a threshold, for
example, of half the voltage supply ($V_{cc}/2$) thereby avoiding comparison
with zero voltage level. As with the embodiments described in Figs. 1
and 2, the analog multiplexer 110 is controlled by the controller and
10 counter circuit 125 to select an analog voltage input for conversion for
connection to input capacitor 130. After capacitor 130 charges to that
selected input voltage, the analog multiplexer 110 is open circuited to
disconnect capacitor 130.

15 The control circuit 125 reads the output of comparator 300 to
determine if the input voltage across the input capacitor 130 is greater
than or less than the $V_{cc}/2$ threshold. If the input voltage is less than
the threshold, control circuit 125 operates FET switches 305, 310, 315,
320, and 325 to incrementally pump the charge stored on input
20 capacitor using pumping capacitor 220 until it reaches the threshold
voltage $V_{cc}/2$. Conversely, if the input voltage initially was above the

threshold $V_{cc}/2$, the control circuit 125 operates the FET switches to incrementally pump down the voltage stored across input capacitor 130 until it crosses the $V_{cc}/2$ threshold as indicated by the output of comparator 300.

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Assuming that the initial comparator output indicates that the input voltage is less than the threshold voltage $V_{cc}/2$, the following control signals generated by controller 125 are applied to the gates of the FET switches. Initially, $Q1 = 0$ and $\bar{Q}1 = 1$ which causes the FET switch 305 to disconnect the input capacitor 130 from the pumping capacitor 220. $Q2$ is set equal to 0 to apply a low level to P-type FET 310 so that it conducts connecting the leftmost plate of pumping capacitor 220 to V_{cc} . At the same time, $Q5$ is set equal to 1 so that the N-type FET 320 conducts connecting the right plate of pumping capacitor 220 to ground. This switch configuration charges the pumping capacitor 220 to V_{cc} with positive polarity on the left plate and zero polarity on the right plate of the capacitor.

Thereafter, $Q2$ and $Q5$ are set equal to 1 to "turn off" FET switches 305 and 320. $Q4$ is then set equal to 0 which causes P-type FET 325 to conduct, pulling the rightmost plate of pumping



capacitor 220 to V_{cc} . Because of conservation of charge, the potential on the right hand plate of pumping capacitor 220 rising from 0 to V_{cc} attempts to force the potential on the left plate of capacitor 220 to rise to $2V_{cc}$ in order to maintain the immediately preceding potential difference of V_{cc} across capacitor 220. At the same time, Q1 is set equal to 1 and $\bar{Q}$ equal to 0 activating switch 305 to connect the left plate of capacitor 220 to input capacitor 130. The difference between $2V_{cc}$ stored across capacitor 220 and the voltage across input capacitor 130, (which is somewhere between zero and $V_{cc}/2$), multiplied by the capacitance value of capacitor 220 determines the amount of charge transferred from pumping capacitor 220 to input capacitor C11. Thus in this example, the voltage across input capacitor 130 rises by an incremental amount between $(1.5 V_{cc} \times C220/C130)$ and $(2.0 V_{cc} \times C220/C130)$.

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If the initial voltage stored across input capacitor 130 is greater than $V_{cc}/2$, the input capacitor 130 is pumped down using the following example procedures. Initially, Q1 is set equal to 0 and $\bar{Q}$ equal to 1 to disconnect input capacitor 130 from pumping capacitor 220. The gate voltage applied to N-type FET 315 is set equal to 1 so that FET 315 conducts connecting the left plate of pumping capacitor 220 to ground.

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At the same time, the gate voltage applied to P-type FET 325 is set equal to 0 which effectively connects the right plate of pumping capacitor 220 to the power supply voltage V_{cc} charging pumping capacitor 220 to a potential of V_{cc} with positive polarity on the right
5 plate and zero polarity on the left plate. Thereafter, gate voltage Q3 is set equal to 0 and Q4 is set equal to 1 to turn-off FETs 315 and 325.

Gate voltage Q5 is then set equal to 1 to turn-on N-type FET 320, connecting pumping capacitor 220 to ground which pulls the
10 voltage on the right plate of capacitor from V_{cc} to zero. Conservation of charge requires that the potential on the left plate of capacitor 220 attempt to move from 0 to $-V_{cc}$ in order to maintain the initial voltage drop of V_{cc} across capacitor 220. At the same time, gate voltage input Q1 is set equal to 1 and Q is set equal to 0, connecting the left plate of
15 pumping capacitor 220 to input capacitor 130. The difference between the voltage across capacitor 220 and the voltage stored on input capacitor 130 (which is somewhere between $V_{cc}/2$ and V_{cc}) times the pumping capacitance gives the amount of incremental charge transferred from capacitor 220 to input capacitor 130. As a result of
20 the charge transfer, the voltage across input capacitor is reduced by an

incremental amount between $(1.5 V_{cc} \times C220/C100)$ and $(2.0 V_{cc} \times C220/C130)$.

This embodiment of the present invention provides an analog to
5 digital converter which uses FET switches to pump an input voltage
below a non-zero reference voltage up to that reference voltage or to
pump a voltage above the non-zero reference voltage down to the
reference voltage thereby obtaining symmetrical control about a non-
zero reference voltage. The incremental step size for pumping up or
10 pumping down the input capacitor C130 is slightly dependent upon the
input voltage but in a symmetrical way that provides greater
resolution (finer steps) in the center of the analog to digital convertor's
useful range, (e.g., $V_{cc}/2$), with less resolution (coarser steps) at the
extremes of the range, (e.g., zero and V_{cc}). This is advantageous
15 because most voltages to be measured by the A to D convertor would
first be arranged by suitable scaling to fall with the greatest
probability in the center of the A to D convertor range, where the
inventive circuit provides highest accuracy.

20 Although MOS-type switches are preferred for their low cost,
ease of manufacture, and superior response with respect to other

electronic switches, other switches including bipolar junction transistors or technologies such as GaAs could be used to implement switching functions in the present invention. Thus, the present invention provides a low cost, easily manufactured analog to digital
5 converter which uses MOS switching technology and can be combined on an integrated circuit with other signal processing circuitry.

While the invention has been described in connection with what is presently considered to be the most practical and preferred
10 embodiment, it is to be understood that the invention is not to be limited to the disclosed embodiment, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

WHAT IS CLAIMED IS:

1 1. An analog to digital converter, comprising:
2 a first capacitor connected at a first terminal to an analog signal
3 to charge the capacitor in accordance with a current voltage level of
4 the analog signal and at a second terminal to ground;
5 a second capacitor; and
6 electronic control circuitry for alternately connecting the second
7 capacitor between the first capacitor and a power supply to remove
8 increments of charge from the first capacitor until the first capacitor is
9 discharged,
10 wherein a number of removed increments of charge associated
11 with discharging the first capacitor is used to generate a digital value
12 corresponding to the current voltage level of the analog signal.

1 2. The analog to digital converter in claim 1, further
2 comprising:
3 a multiplexer for receiving multiple analog signals and selecting
4 one of the received analog signals for connection to the first capacitor
5 in response to a control signal received from the electronic control
6 circuitry,





7 wherein after the first capacitor charges to a level commensurate
8 with the current voltage level of the selected analog signal, the
9 electronic control circuitry causes the multiplexer to disconnect the
10 analog signal from the first capacitor.

1 3. The analog to digital converter in claim 1, further
2 comprising:

3 a comparator having one input connected to the first terminal of
4 the first capacitor and another input connected to ground for detecting
5 when the voltage across the first capacitor is at or nearly zero and then
6 generating a detection signal causing the electronic control circuitry to
7 generate the digital value.

1 4. The analog to digital converter in claim 2, further
2 comprising a clock source, wherein the electronic control circuitry
3 includes a counter for counting clock pulses generated by the clock
4 source from a predetermined starting point after the first capacitor is
5 charged until the detection signal is received from the comparator
6 halts the counting, with the digital readout from the counter
7 corresponding to the digital value.



1 5. The analog to digital converter in claim 1, further
2 comprising:
3 a switching circuit connected to the first terminal of the first
4 capacitor, to ground, and to the power supply including:
5 a first pair of switches with one switch connected to a first
6 terminal of the second capacitor and the other switch connected to a
7 second terminal of the second capacitor, and
8 a second pair of switches with one switch connected to a
9 first terminal of the second capacitor and the other switch connected to
10 a second terminal of the second capacitor,
11 wherein the electronic control circuitry generates switching
12 control signals alternately connecting the second capacitor through the
13 first pair of switches between ground and the power supply and
14 through the second pair of switches between the first terminal of the
15 first capacitor and ground to remove the increments of charge from the
16 first capacitor.

1 6. The analog to digital converter in claim 5, wherein each
2 switch in the first and second pairs of switches is a complementary
3 semiconductor switch having an N-type, insulated gate, field effect





4 transistor (FET) and a P-type, insulated gate, field effect transistor
5 (FET).

1 7. The analog to digital converter in claim 5, further
2 comprising:
3 a clock source for generating clock signals,
4 the electronic control circuitry including a counter for counting
5 the clock signals and generating a counter output signal that
6 alternates between a first state and a second state,
7 wherein the switching control signals include the counter output
8 signal such that the first pair of switches is selected to connect the
9 second capacitor between ground and the power supply when the
10 counter output is in the first state and the second pair of switches is
11 selected to connect the second capacitor between the first terminal of
12 the first capacitor and ground.

1 8. An analog to digital converter comprising:
2 an input capacitor connected at a first terminal to store an analog
3 voltage and at a second terminal to ground;
4 control circuitry connected to the input capacitor at the first
5 terminal;





6 dynamic detection circuitry connected to the first terminal of the
7 input capacitor for determining whether an input signal applied to a
8 first input terminal of a comparator generated in response to the
9 voltage across the input capacitor is equal to or greater than a
10 nonzero, threshold voltage applied to a second input terminal of the
11 comparator and for providing an output signal from the comparator to
12 the control circuit indicating whether the input capacitor is discharged,
13 wherein said dynamic detection circuitry is connected through a
14 pump capacitor to a pump output signal of the control circuit, the
15 control circuit alternately charging and discharging the pump
16 capacitor using the pump output signal and discharging the input
17 capacitor by an increment of charge after each charge and discharge
18 cycle of the pump capacitor, until the dynamic detection circuitry
19 indicates that the input capacitor is discharged, a total number of
20 incremental discharges of the input capacitor being used to generate a
21 digital value for the analog voltage.

1 9. The analog to digital converter in claim 8, wherein the
2 control circuit includes a counter for counting the number of
3 incremental discharges to provide a digital code corresponding to a
4 final count value.





1 10. The analog to digital converter in claim 8, further
2 comprising:
3 a multiplexer for receiving multiple analog signals and selecting
4 one of the received analog signals for connection to the input capacitor
5 in response to a control signal received from the control circuit,
6 wherein after the input capacitor charges to a level
7 commensurate with the current voltage level of the selected analog
8 signal, the control circuit causes the multiplexer to disconnect the
9 analog signal from the input capacitor.

1 11. The analog to digital converter in claim 8, further
2 comprising:
3 a resistor connected in series with the pump capacitor between
4 the control circuit and the dynamic detector.

1 12. The analog to digital converter in claim 8, wherein the
2 dynamic detection circuitry includes a first field effect transistor (FET)
3 having a gate electrode connected to ground and a second field effect
4 transistor (FET) having a gate electrode connected to the first terminal





5 of the first capacitor with drain electrodes being connected to a power
6 supply,
7 the first and second FETs having a common source electrode
8 connected to the pump capacitor, and
9 a drain electrode of the second FET connected to the first input
10 terminal of the comparator.

1 13. The analog to digital converter in claim 12, wherein when
2 the pump signal is in a first logic state, current flows in a first
3 direction from either or both of the first and second FETs from the
4 common source electrodes through the pump capacitor discharging the
5 pump capacitor, and wherein the comparator compares a voltage at
6 the first input terminal with the nonzero, threshold voltage during a
7 comparison time interval when the pump signal is in the first logic
8 state.

1 14. The analog to digital converter in claim 13, wherein the
2 common source is connected by a diode to ground such that when the
3 pump signal is in a second logic state, current flows in a second
4 direction opposite the first direction through the diode to charge up the
5 pump capacitor, and wherein during a discharge time interval when





6 the pump signal is in the second logic state, the control circuit
7 discharges the input capacitor by an increment discharge if the
8 comparator indicates during an immediately preceding comparison
9 time interval that the input capacitor is not discharged.

1 15. The analog to digital converter in claim 12, wherein the
2 dynamic detection circuitry further includes a current mirror circuit
3 connected between the drain electrodes of the first and second FETs
4 and the power supply.

1 16. The analog to digital converter in claim 15, wherein the
2 current mirror includes a third FET connected at its source electrode
3 to a voltage supply and at its drain electrode to the second FET and to
4 the first input terminal of the comparator and a fourth FET connected
5 at its source electrode to the power supply, at its drain electrode to the
6 drain electrode to the drain electrode of the first FET, and at its gate
7 electrode to the a gate electrode of the third FET and to the drain
8 electrode of the fourth FET.





1 17. The analog to digital converter in claim 12, wherein the
2 first and second transistors are formed in a well of a first conductivity
3 type diffused into a substrate of a second conductivity type.

1 18. A method of detecting when an input signal has a zero
2 voltage level comprising the steps of:
3 storing a voltage across a first capacitor in accordance with a
4 voltage level of an input signal;
5 generating a representative voltage signal that represents a
6 current voltage across the first capacitor;
7 alternately charging a second capacitor during a first time
8 interval and discharging the second capacitor during a second time
9 interval;
10 during the first time interval, discharging a portion of charge
11 stored on a first capacitor;
12 during the second time interval, detecting whether the current
13 voltage across the first capacitor has a zero voltage level by comparing
14 the representative voltage with a nonzero reference voltage; and
15 indicating that the current voltage across the first capacitor has
16 reached a zero voltage level when the representative voltage is the
17 same as or greater than the nonzero reference voltage.



1 19. The method in claim 18, wherein the second capacitor
2 charges through a diode to ground in a first current direction and
3 discharges through a series connected resistor in a second opposite
4 current direction.

1 20. An apparatus comprising a positive power supply and a
2 comparator circuit connected to the positive power supply for detecting
3 when an input voltage reaches zero voltage that does not require a
4 negative power supply and does not employ a converter to convert
5 positive polarity power from the positive power supply into negative
6 polarity power.

1 21. An analog to digital converter, comprising:
2 a first capacitor connected at a first terminal to an analog signal
3 to charge the capacitor in accordance with a current voltage level of
4 the analog signal and at a second terminal to ground;
5 a comparator having one input terminal connected to the first
6 terminal of the first capacitor and another input terminal connected to
7 a reference voltage for generating:



8 (a) a first signal when the voltage across the first
9 capacitor is greater than the reference voltage,
10 (b) a second signal when the voltage across the first
11 capacitor is less than the reference voltage, and
12 (c) a third signal when the voltage across the first
13 capacitor is the same as the reference voltage; and
14 electronic control circuitry for supplying increments of charge to
15 the first capacitor when the second signal is generated until the third
16 signal is generated and for removing increments of charge from the
17 first capacitor when the first signal is generated until the third signal
18 is generated,
19 wherein the electronic control circuitry counts a number of charge
20 increments or decrements to generate a digital value corresponding to
21 the current voltage level of the analog signal.

1 22. The analog to digital converter in claim 21, further
2 comprising:
3 a second capacitor for storing the increment of charge, and
4 a plurality of switches connected to the second capacitor,



5 wherein the electronic control circuitry alternately switches the
6 second capacitor between various states depending on the output from
7 the comparator.

1 23. The analog to digital converter in claim 21, wherein when
2 the comparator generates the first signal, the electronic control
3 circuitry generates control signals to successively activate switches to
4 connect the second capacitor between a power supply and ground and
5 then to connect the second capacitor to the first capacitor thereby
6 removing increments of charge from the first capacitor until the third
7 signal generated.

1 24. The analog to digital converter in claim 21, wherein when
2 the comparator generates the second signal, the control circuitry
3 generates control signals to activate switches to successively connect
4 the second capacitor between a power supply and ground and then to
5 connect the second capacitor to the first capacitor to add increments of
6 charge from the first capacitor until the third signal generated.

1 25. The analog to digital converter in claim 21, wherein the
2 reference voltage is a nonzero voltage.



1 26. The analog to digital converter in claim 21, further
2 comprising:

3 a multiplexer for receiving multiple analog signals and selecting
4 one of the received analog signals for connection to the first capacitor
5 in response to a control signal received from the electronic control
6 circuitry,

7 wherein after the first capacitor charges to a level commensurate
8 with the current voltage level of the selected analog signal, the
9 electronic control circuitry causes the multiplexer to disconnect the
10 analog signal from the first capacitor.

1 27. The analog to digital converter in claim 23, wherein each
2 switch is an insulated gate, field effect transistor (FET).

1 28. The analog to digital converter in claim 24, wherein each
2 switch is an insulated gate, field effect transistor (FET).

3

4 29. A method for converting an analog signal into a digital
5 signal comprising the steps of:



6 charging a first capacitor in accordance with a current voltage
7 level of the analog signal;
8 comparing the voltage across the first capacitor to a reference
9 voltage;
10 supplying increments of charge to the first capacitor when a
11 voltage across the capacitor is less than a reference voltage and
12 removing increments of charge when the voltage across the first
13 capacitor is greater than the reference voltage; and
14 counting a number of the charge increments or decrements to
15 generate a digital value corresponding to the current voltage level of
16 the analog signal.

1 30. The method in claim 29, wherein the increments of charge
2 are supplied until the charge across the first capacitor is the same as
3 the reference voltage.

1 31. The method in claims 29, wherein the increments of charge
2 are removed until the charge across the first capacitor is the same as
3 the reference voltage.

1 32. The method in claim 29, further comprising the step of:

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- 2 discontinuing supplying increments of charge when the first
- 3 capacitor is discharged and then performing the counting step.