

A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICEFIELD OF THE INVENTION

5 The present invention relates to the reduction of the power dissipation in a semiconductor integrated circuit device, and has particular application to a CMOS IC circuit.

10 BACKGROUND OF THE INVENTION

Conventionally, a bus-controller constituted as a semiconductor integrated circuit device is designed to decode an external signal input designating the status of the microprocessor output and to output a control signal at appropriate timings. This conventional bus-controller has a circuit construction using bipolar transistors, and there is no bus-controller circuit aiming to lower the power dissipation.

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As a prior art semiconductor integrated circuit device aiming to lower the power dissipation there is an 8-bit parallel microprocessor M5M80C88P produced by Mitsubishi Electric Co., Ltd.. This device has a sleep mode where some internal clocks are halted by executing the HALT instruction. Additionally, in this

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device external signals are decoded to halt the internal clocks in a special state, whereby the power dissipation is reduced.

5 SUMMARY OF THE INVENTION

According to the present invention, there is provided a semiconductor integrated circuit device, other than a microprocessor in the form of an integrated circuit, which comprises a circuit means for receiving an external clock signal and normally transmitting it as an internal clock signal, the circuit means also receiving an externally applied signal and a signal internal to the device, and responding to a predetermined state of the externally applied signal to interrupt the transmission of the clock signal, so as to reduce the power consumption of the device by removing the internal clock signal, when the signal internal of the device is in a first state and not when the internal signal is in a second state.

In one embodiment, the device is a bus controller.

Preferably the semiconductor integrated circuit device has a circuit construction using CMOS transistors in which the power dissipation is further reduced.

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An embodiment of the present invention, given by way of example, will now be described with reference to the accompanying drawings, in which:

5 BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a circuit in a semiconductor integrated circuit device embodying the present invention;

10 Figure 2 is a timing chart for exemplifying the operation of the embodiment.

Figure 3(a) is a circuit diagram showing an inverter constituted by NMOS transistors, and Figure 3(b) is a
15 circuit model of Figure 3(a) obtained by replacing the circuit elements;

Figure 4(a) is a circuit diagram showing an inverter constituted by CMOS transistors, and Figure 4(b) is a
20 circuit model of Figure 4(a) obtained by replacing the circuit elements; and

Figure 5 is a circuit diagram of the inverter of Figure 4(a) for exemplifying the AC current which
25 flows through this circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a circuit construction in a semiconductor integrated circuit device embodying the present invention. In this embodiment an external clock input such as a system clock is controlled in accordance with an external signal input designating the status of a microprocessor output.

10 In Figure 1 there are provided an input terminal 1 for an internal control signal c, and input terminals 2, 3 and 4 for receiving each bit b_1 to b_3 of an external signal which is output from the microprocessor. The microprocessor outputs an external signal b_1 to b_3 in
15 accordance with its state, and when it is stopped it outputs an external signal of "111". There are also provided an input terminal for an external clock a, and an inverter 6 which receives an internal control signal c through the input terminal 1. This internal
20 control signal c is a signal produced for generating a power saving signal PD when the external signal is "111". A power saving signal generator comprising an AND gate 7 is provided to receive the external signal b_1 to b_3 through the input terminals 2 to 4, and the
25 output of the inverter 6. This AND circuit 7

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generates a power saving signal PD in a special condition of the external signal b_1 to b_3 and the output of the inverter 6. A NOR gate 8 is provided to receive the power saving signal PD from the power saving signal generator 7 and the external clock a through the input terminal 5, and this NOR gate 8 outputs an internal clock d at its output terminal 9. The inverter 6, the power saving signal generator 7, and the NOR gate 8 are constituted by CMOS integrated circuits using CMOS transistors. These circuits 6, 7, and 8 constitute a circuit for reducing the power dissipation in the semiconductor device.

Before describing the operation of the device, the reason why the power dissipation is reduced in a circuit construction using CMOS transistors will be described with reference to Figures 3 and 4.

Figure 3 shows an inverter constituted by NMOS transistors, and Figure 4 shows an inverter constituted by CMOS transistors. Generally, MOS transistors have extremely high input impedance, and a current for driving the next stage can be ignored except for transient states in both of NMOS and CMOS transistors.

The NMOS inverter shown in Figure 3 is constituted by a load transistor 10 and a driver transistor 11, and a circuit model shown in Figure 3(b) is obtained by replacing the load transistor 10 by a resistor R and the driver transistor 11 by a switch 1a. When a signal "L" is input in this circuit, the switch 1a is opened so that the circuit will output a signal "H". When a signal "H" is input, the switch 1a is closed so that the circuit will output a signal "L". In this circuit state, a DC current flows constantly from the power supply Vcc to the ground.

On the other hand, a CMOS inverter is constituted by a P channel transistor 12 and an N channel transistor 13 as shown in Figure 4(a), and a circuit model shown in Figure 4(b) is obtained by replacing the P and N channel transistors 12 and 13 by switches 1c and 1d, respectively. When a signal "L" is input in this circuit, the switches 1c and 1d are closed and opened, respectively, so that the circuit will output a signal "H". When a signal "H" is input, the switches 1c and 1d are opened and closed, respectively, so that the circuit will output a signal "L". In this way, the switches 1c and 1d are complementarily opened or closed, thereby incurring no DC current flow.

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Accordingly, the dissipation current is reduced in CMOS circuits.

5 The operation of the device of Figure 1 will be described below.

When all bits b_1 and b_3 of the external signal designating the status of the microprocessor output are "H" (it means that the microprocessor is stopped) and the internal control signal c shown in Figure 2(c) is "L" (time period T_1 in Figure 2), the control signal c of "L" is inverted by the inverter 6, and it is input to the power saving signal generator 7. Then, the power saving signal PD that is to be output from the generator 7 becomes "H", and this output "H" is input to the NOR gate 8. Thus, the NOR gate 8 outputs "L" regardless of the external clock a having a periodic waveform as shown in Figure 2(a). In this way, the internal clock d at the output terminal 9 is fixed to "L" as shown in Figure 2(d), and the device is set at the power dissipation reduction mode.

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When the internal control signal c shown in Figure 2(c) becomes "H" (time period T_2 in Figure 2), the power saving signal PD that is to be output from the

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generator 7 falls down to "L" immediately regardless of the state of the external signal b_1 to b_3 , and the inverted signal of the external clock a appears at the output of the NOR gate 8 as shown in Figure 2(d). In this way, the power dissipation reduction mode is cancelled, and the device returns to the usual operation mode.

When all the bits b_1 to b_3 of the external signal becomes "H" and the internal control signal c becomes "L" (time period T_3 in Figure 2), the device enters the power dissipation mode in the same manner as described above.

By the way, in a condition other than that all the bits b_1 to b_3 of the external signal are "H", the power saving signal PD does not become "H" even if the internal control signal c is "L". Such a case is not illustrated in Figure 2.

As described above, the internal clock is temporarily fixed to a specific value in this embodiment. When the internal clock is halted in CMOS circuit the power dissipation is reduced as described below.

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Only quite a small DC current flows in a CMOS circuit as described above, and an AC current having a low order is dominant in the dissipation current. This AC current is a current which flows transiently at the switching, and it includes as its main components a current for charging or discharging the load capacitance CL and a current which instantaneously flows through the circuit, for example, that which flows from the power supply Vcc to the ground while the P channel and the N channel transistors are turned to be ON at the same time while the input is switched from "H" to "L" (refer to Figure 5). Such an AC current is approximately proportional to the switching frequency because it only flows at the switching. Accordingly, it is possible to lower the AC current to approximately zero and thereby to reduce the dissipation current by halting the clock which is switched ON and OFF repeatedly at a high speed. Only a leak current having a much lower order becomes a dissipation current.

In this way, the device is set to the power dissipation reduction mode by the output of the power saving signal generator 7 when the inputs of the external signal b_1 to b_3 and the internal control

signal c comply with a special condition, and the internal clock d that is to be output from the NOR gate 8 is temporarily fixed to a specific value, whereby the dissipation current by the charge and discharge of the load capacitance is reduced. This means that the reduction of the power dissipation is realized by only providing a few additional logic gates.

10 In the above-illustrated embodiment, the power dissipation reduction circuit is constituted by the inverter 6, the AND gate 7, and the NOR gate 8, but it may be constituted by some other logic circuit with the same effects.

15 As is evident from the foregoing, in an embodiment of the present invention, a semiconductor integrated circuit device is constituted by CMOS integrated circuit using CMOS transistors, and the internal system clock is temporarily fixed to a specific value, whereby the power dissipation is reduced.

20 Various changes and modifications of the described embodiment will be apparent to those skilled in the art.

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CLAIMS:

1. A semiconductor integrated circuit device,
other than a microprocessor in the form of an
5 integrated circuit, which comprises a circuit means
for receiving an external clock signal and normally
transmitting it as an internal clock signal, the
circuit means also receiving an externally applied
signal and a signal internal to the device, and
10 responding to a predetermined state of the externally
applied signal to interrupt the transmission of the
clock signal, so as to reduce the power consumption of
the device by removing the internal clock signal, when
the signal internal of the device is in a first state
15 and not when the internal signal is in a second state.
2. A device according to claim 1, which is a CMOS
integrated circuit device.
- 20 3. A device according to claim 1 or claim 2,
which is a bus controller.
4. A device according to any one of claims 1 to 3,
which comprises an AND gate for receiving the
25 externally applied signal and the internal signal, and
a NOR gate for receiving the external clock signal and



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the output of the AND gate and outputting the internal clock signal.

5 5. An integrated semiconductor circuit system having a system clock signal, the system comprising a microprocessor and a device according to any one of the preceding claims, the external clock signal being the system clock signal and the externally applied signal indicating the status of the microprocessor.

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6. Semiconductor integrated circuit device substantially as herein described with reference to the accompanying drawings.
