Description

The present invention relates to a process for fabricating a semiconductor device having p-channel and n-channel MISFETs that have good characteristics with regard to the threshold voltage (V_{th}) vs. the channel length (L_g).

In MOS devices, there is a tendency to reduce the channel length. As a consequence, the electric field between the source region and the drain region is increased. Therefore, hot charriers are injected into the gate oxide film, deterioriating the characteristics of the device. To prevent this problem, it was proposed to reduce the electric field between the source region and the drain region by a lightly doped drain (LDD) construction (see, for example, IEEE Transactions on Electron Devices ED-29 (1982) No. 4, pages 590 to 596).

However, employment of the LDD structure makes it necessary to provide side walls and to effect ion implantation before and after the formation of the side walls, resulting in more manufacturing steps and higher manufacturing costs.

Still more manufacturing steps are required when the LDD construction is adapted to CMOS devices. Ion implantation must be effected one more time on the p-channel metal oxide semiconductor field-effect transistor (P-MOSFET) and on the n-channel metal oxide semiconductor field-effect transistor (N-MOSFET), respectively. Therefore, a photoresist mask must be formed two more times, compared with a conventional device not of LDD construction. The process is thus complicated in addition to the extra step for forming the side walls, and the manufacturing costs become expensive. Further, in such CMOS devices, the effective channel length becomes extremely short, so that the V_{th}-L_g characteristics are deterioriated.

In the IEEE Transactions on Electron Devices ED-31 (1984) No. 2, pages 205 to 214, a CMOS device including MOSFETs with gate electrodes having sidewalls and an LDD structure only on the n-channel side is shown. However, there is nothing disclosed on the material of these sidewalls and the fabrication process of the device and the role of the sidewalls therein.

From the Patent Abstracts of Japan, Volume 7, No. 40 (E-159)(1185), 1983; or the JP-A-57-192063, respectively, there is known a process for reducing the number of photomask steps in producing CMOS devices. However, the gate electrodes thereof do not have side walls, and there is used an additional photoresist mask for implanting ions in high concentration. This photoresist mask has then to be removed.

The object of the present invention is to provide a process for manufacturing a semiconductor device which exhibits good characteristics of threshold voltage (V_{th}) vs. channel length (L_g), and which, when adapted to CMOS devices, enables a simplification of the manufacturing process and a reduction of the manufacturing costs.

Starting from the above mentioned prior art described in the IEEE ED-31 paper, this object is solved by the features described in attached claim 1. In the subclaims, preferred embodiments are included.

According to the invention, the source and drain regions are so formed that the junction of the semiconductor layer is positioned close to each end of the gate electrode so that the effective channel length can be increased even when the gate is short, and so that the MOS device shows good V_{th}-L_g characteristics.

Further, the source and drain regions are formed by implanting impurity ions after the side walls have been formed on both sides of the gate electrode. Therefore, CMOS devices can be manufactured through a simplified process and at reduced manufacturing costs.

An example of the invention will be explained with reference to the accompanying drawings, in which

Figs. 1A to 1F are sectional views illustrating the steps for manufactoring CMOS devices according to an embodiment of the present invention.

As shown in Fig. 1A, first an n-type well 3 is formed by a conventional method on an n-type silicon semiconductor substrate 1, and then a p-type well 2 is formed. The substrate 1 has an impurity concentration of $5 \times 10^{14}/cm^3$, the p-type well 2 has an impurity concentration of $2 \times 10^{16}/cm^3$ with boron ions implanted and drive-in diffused, and the n-type well 3 has an impurity concentration of $4 \times 10^{16}/cm^3$ with phosphorus or arsenic ions implanted and drive-in diffused. A p-type single crystalline silicon having an impurity concentration of $1.5 \times 10^{15}/cm^3$ may be used as the substrate 1. As shown in Fig. 1A, furthermore, the substrate 1 is thermally oxidized to form a field oxide film 4 to define a region where the elements are to be formed. A p^+-type channel stopper may be formed under the field oxide film 4 in the p-type well 2. A thin gate oxide film 5 which is a silicon oxide film is formed by thermally oxidizing the substrate 1 on the region where the elements are to be formed. A polycrystalline silicon layer 7 is formed by the CVD method on the gate oxide film 5, and is doped with impurities such as phosphorus ions to a high concentration to reduce the resistance thereof. Then, a phosphosilicate glass (PSG) film 6 is formed thereon by the CVD method. Next, the PSG film 6 and the polycrystalline silicon layer 7 are subjected to etching (patterning) relying upon a conventional step of photolighography using a photoresist, in order to form a gate electrode 8

consisting of polycrystalline silicon layer 7 the upper surface of which, is masked with the PSG film 6.

Then, as shown in Fig. 1B, a p-MOSFET-forming region (region other than n-MOSFET-forming region) is masked with a resist 14, and phosphorus ions are implanted into the n-MOSFFT-forming region at a dose of 1 x $10^{13}/cm^2$ and an energy of 60 KeV, to form a shallow ion-implanted layer 15 of a low concentration. After the resist 14 is removed, annealing is effected to obtain an n^--type layer 15 having a surface concentration of about 1 x $10^{18}/cm^3$.

An SiO_2 film 16 is formed by the CVD method on the whole surface of the substrate as shown in Fig. 1C, and is then subjected to etching over the whole surface thereof by reactive ion etching (RIE) with CHF_3 gas. The SiO_2 film 16 is left as side walls 16a on both sides of the gate electrode 8.

Referring to Fig. 1D, the p-MOSFET-forming region (n-type well 3) is masked with a resist 17 by photoetching, and arsenic ions are implanted onto the n-MOSFET-forming region (p-type well 2) at a dose of 7 x $10^{15}/cm^2$, and an energy of 100 KeV to form a deep ion-implanted layer 18 of a high concentration. After the resist 17 is removed, an n^+-type layer 18 is formed by annealing so as to have a surface concentration of 8 x $10^{20}/cm^3$.

Thus, an n-MOSFET of LDD construction having a source region 19 and a drain region 20 is formed in the p-type well 2.

Then, the whole surface except the n-type well 3 is masked with a resist 21 as shown in Fig. 1E. With side walls 16a on the n-type well 3 as masks, boron ions are implanted at a dose of 2 x $10^{15}/cm^2$ and an energy of 25 KeV to form a deep ion-implanted layer 22 having a high concentration. After the resist 21 is removed, a p^+-type layer 22 is formed by annealing to have a surface concentration of 3 x $10^{20}/cm^3$. Due to annealing, the junction of the p^+-type layer 22 infiltrates into the under portion of the gate electrode 8 as shown in Fig. 1F, since boron ions have a high diffusion velocity. A source region 23 and a drain region 24 of a single diffused construction are thus formed having the effect of reducing the electric field intensity just like that of the LDD construction.

As described above, the source and drain regions 19, 20 of the n-MOSFET constituting the CMOS device comprise a shallow n^--type layer 15 and a deep n^+-type layer 18 which is formed in an offset gate construction. Therefore, even when the channel is shortened, the electric field intensity between the source and the drain can be reduced, and characteristics can be prevented from being degraded by hot carriers. Therefore, an n-MOSFET having a high breakdown voltage is formed.

Further, by ion implantation after the side walls 16a have been formed, the source and drain regions 23, 24 of p-MOSFET of the other side constituting the CMOS device are formed into a single p^+-type layer 22 (single drain construction), so that the junction at the end of the p^+-type layer 22 will penetrate into the under portion of the gate electrode 8. Therefore, even if the gate length is reduced, the effective channel length can be increased provided the side walls 16a are very thick, making it possible to obtain a p-MOSFET having good V_{th}-L_g characteristics. Further, the LDD construction of the p-MOSFET is replaced by the p^+-type layer 22 (single drain construction) only without having p^--type layer according to the embodiment of the present invention, by giving attention to the fact that when a p-MOSFET is realized in LDD construction, the difference in impurity concentration is very small at the ends of the p^--type layer and the p^+-type layer that form source and drain regions, and that boron ions have a high diffusion velocity. Accordingly, the p-MOSFET of the embodiment of the present invention exhibits the effect of reducing the electric field intensity which is substantially equal to that of the p-MOSFET of LDD construction. Thus, the p-MOSFET of this embodiment exhibits good V_{th}-L_g characteristics has the effect of reducing the electric field intensity.

According to the present invention as described above, there is obtained a p-MOSFET having good V_{th}-L_g characteristics that could not be obtained with a p-MOSFET of LDD construction.

According to the CMOS device of the above-mentioned embodiment, furthermore, the photolithography step that was required for the CMOS devices having p- and n-MOSFET's of LDD construction can be eliminated hence, manufacturing costs can be decreased. Furthermore, the CMOS device of the present invention contains a p-MOSFET having good V_{th}-L_g characteristics.

In the present invention, the effects are obtained as mentioned below:

(1) By adapting the present invention to a CMOS device having n-MOSFET and p-MOSFET, it is possible to obtain an n-MOSFET and a p-MOSFET, both having good V_{th}-L_g characteristics through a simple process and at a reduced cost.

(2) Even when the gate length is reduced, effective channel length can be increased by placing the junctions of the layer forming the source and drain regions at suitable positions close to each end of the gate electrode, thereby to obtain good V_{th}-L_g characteristics. In particular, even when the gate length is reduced, effective channel length can be increased by (increasing) the thickness of the side walls and permitting the junctions of an impurity layer that forms the source and drain regions to reach suitable posi-

close to both ends of the gate electrode, y obtaining good V_{th}-L_g characteristics.

(3) When the present invention is adapted to the p-MOSFET, the effect mentioned in (1) above is obtained as well as the aforementioned effect of reducing the electric field intensity. These two effects are not obtained with a p-MOSFET of LDD construction. With the present invention, furthermore, a p-MOSFET is obtained through a simpler process than the process of producing a p-MOSFET of LDD construction, and at a lower cost.

(4) By adapting the present invention to the p-MOSFET of a CMOS device having side walls as will be understood from the foregoing description, the manufacturing process can be simplified and the manufacturing cost can be reduced.

The above-mentioned embodiment may be modified as follows:-

For instance, the gate electrode may be composed of platinum or a high-melting metal, or silicides thereof, or may have a polycide structure in which platinum or a high-melting metal or a silicide thereof is formed on polycrystalline silicon.

In addition to a silicon oxide film, furthermore, the gate insulating film may be composed of any other insulating film (silicon nitride film or a film of a combination thereof). The present invention can further be adapted to MIS (metal insulated semiconductor) FET's.

Instead of the resist, furthermore, a silicon dioxide film or a silicon nitride film may be used as a masking material.

Further, the side wall may be made of any other insulating material, such as silicon nitride or the like, or may be made of a combination of silicon dioxide film and silicon nitride film.

The PSG film 6 need not necessarily be formed.

Further, there may not be formed a well region having the same type of conductivity as the substrate. Here, the substrate may have either n-type or p-type conductivity.

Instead of using a field oxide film, the element may be isolated by any other method, such as by burying an insulating material into grooves that are formed in the substrate by reactive ion etching (RIE) or the like.

It is also allowable to form a thin silicide layer of platinum or a high-melting metal on the surfaces of source and drain regions that are not covered by the side wall.

Claims

1. A process for fabricating a semiconductor device having p-channel and n-channel MISFETs, a first one of which is formed at a first surface region (3) that has a first type of conductivity in a semiconductor substrate (1) and a second one of which is formed at a second surface region (2) of a second type of conductivity formed in said semiconductor substrate (1), comprising:

   (a) forming a gate electrode (8) for each of said MISFETs on a gate insulating film (5), said gate electrode (8) having two sides;

   (b) forming first sub regions (15) by introducing n-type impurities into a region in which an n-channel MISFET is to be formed, using said gate electrode (8) as a mask;

   (c) forming a sidewall (16a) on each side of each gate electrode (8) by depositing an insulating film (16) on the whole surface of said semiconductor substrate (1) and etching the whole surface thereof by reactive ion etching;

   (d) forming second sub regions (18) by introducing n-type impurities into the region in which said n-channel MISFET is to be formed, using said gate electrode (8) and said sidewalls (16a) as masks, said second sub regions (18) being deeper than said first sub regions (15) and having a higher impurity concentration than said first sub regions (15), and said second sub regions (18) together with said first sub regions (15) forming source and drain regions (19, 20) of said n-channel MISFET; and

   (e) forming third sub regions (22) by introducing p-type impurities into a region in which a p-channel MISFET is to be formed, using said gate electrode (8) and said sidewalls (16a) as masks, said third sub regions (22) forming the source and drain regions (23, 24) of said p-channel MISFET.

2. The process of claim 1, wherein said first surface region (3) is an n-well region, and said second surface region (2) is a p-well region formed in said semiconductor substrate (1).

3. The process of claim 1 or 2, wherein said third sub region (22) which is formed in said first surface region (3) extends under said gate electrode (8).

4. The process of any of claims 1 to 3, wherein the impurities for forming said third sub region (22) are boron ions.

5. The process of any of claims 1 to 4, wherein said third sub region (22) is formed by implanting said impurities into said first surface region

tions close to both ends of the gate electrode, thereby obtaining good V_{th}-L_g characteristics.

(3) When the present invention is adapted to the p-MOSFET, the effect mentioned in (1) above is obtained as well as the aforementioned effect of reducing the electric field intensity. These two effects are not obtained with a p-MOSFET of LDD construction. With the present invention, furthermore, a p-MOSFET is obtained through a simpler process than the process of producing a p-MOSFET of LDD construction, and at a lower cost.

(4) By adapting the present invention to the p-MOSFET of a CMOS device having side walls as will be understood from the foregoing description, the manufacturing process can be simplified and the manufacturing cost can be reduced.

The above-mentioned embodiment may be modified as follows:-

For instance, the gate electrode may be composed of platinum or a high-melting metal, or silicides thereof, or may have a polycide structure in which platinum or a high-melting metal or a silicide thereof is formed on polycrystalline silicon.

In addition to a silicon oxide film, furthermore, the gate insulating film may be composed of any other insulating film (silicon nitride film or a film of a combination thereof). The present invention can further be adapted to MIS (metal insulated semiconductor) FET's.

Instead of the resist, furthermore, a silicon dioxide film or a silicon nitride film may be used as a masking material.

Further, the side wall may be made of any other insulating material, such as silicon nitride or the like, or may be made of a combination of silicon dioxide film and silicon nitride film.

The PSG film 6 need not necessarily be formed.

Further, there may not be formed a well region having the same type of conductivity as the substrate. Here, the substrate may have either n-type or p-type conductivity.

Instead of using a field oxide film, the element may be isolated by any other method, such as by burying an insulating material into grooves that are formed in the substrate by reactive ion etching (RIE) or the like.

It is also allowable to form a thin silicide layer of platinum or a high-melting metal on the surfaces of source and drain regions that are not covered by the side wall.

Claims

1. A process for fabricating a semiconductor device having p-channel and n-channel MISFETs, a first one of which is formed at a first surface region (3) that has a first type of conductivity in a semiconductor substrate (1) and a second one of which is formed at a second surface region (2) of a second type of conductivity formed in said semiconductor substrate (1), comprising:

   (a) forming a gate electrode (8) for each of said MISFETs on a gate insulating film (5), said gate electrode (8) having two sides;

   (b) forming first sub regions (15) by introducing n-type impurities into a region in which an n-channel MISFET is to be formed, using said gate electrode (8) as a mask;

   (c) forming a sidewall (16a) on each side of each gate electrode (8) by depositing an insulating film (16) on the whole surface of said semiconductor substrate (1) and etching the whole surface thereof by reactive ion etching;

   (d) forming second sub regions (18) by introducing n-type impurities into the region in which said n-channel MISFET is to be formed, using said gate electrode (8) and said sidewalls (16a) as masks, said second sub regions (18) being deeper than said first sub regions (15) and having a higher impurity concentration than said first sub regions (15), and said second sub regions (18) together with said first sub regions (15) forming source and drain regions (19, 20) of said n-channel MISFET; and

   (e) forming third sub regions (22) by introducing p-type impurities into a region in which a p-channel MISFET is to be formed, using said gate electrode (8) and said sidewalls (16a) as masks, said third sub regions (22) forming the source and drain regions (23, 24) of said p-channel MISFET.

2. The process of claim 1, wherein said first surface region (3) is an n-well region, and said second surface region (2) is a p-well region formed in said semiconductor substrate (1).

3. The process of claim 1 or 2, wherein said third sub region (22) which is formed in said first surface region (3) extends under said gate electrode (8).

4. The process of any of claims 1 to 3, wherein the impurities for forming said third sub region (22) are boron ions.

5. The process of any of claims 1 to 4, wherein said third sub region (22) is formed by implanting said impurities into said first surface region

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(3), followed by annealing.

6. The process of any of claims 1 to 5, wherein the impurities for forming said first sub region (15) are phosphorus ions.

7. The process of any of claims 1 to 6, wherein the impurities for forming said second sub region (18) are arsenic ions.

Revendications

1. Procédé pour fabriquer un dispositif à semiconducteurs comportant des transistors MISFET à canal p et à canal n, dont un premier est formé dans une première zone superficielle (3) qui possède un premier type de conductivité dans un substrat semiconducteur (1), et dont un second est formé dans une seconde zone superficielle (2) possédant un second type de conductivité et formée dans ledit substrat semiconducteur (1), comprenant :
   (a) la formation d'une électrode de grille (8) pour chacun desdits transistors MISFET sur une pellicule d'isolant de grille (5), ladite électrode de grille (8) possédant deux côtés;
   (b) la formation de premières sous-régions (15) moyennant l'introduction d'impuretés de type n dans une région dans laquelle un transistor MISFET à canal n doit être formé, en utilisant ladite électrode de grille (8) en tant que masque;
   (c) la formation d'une paroi latérale (16a) de chaque côté de chaque électrode de grille (8) au moyen du dépôt d'une pellicule isolante (16) sur l'ensemble de la surface dudit substrat semiconducteur (1) et la gravure de l'ensemble de la surface de ce substrat par gravure ionique réactive;
   (d) la formation de secondes sous-régions (18) moyennant l'introduction d'impuretés de type n dans la région dans laquelle ledit transistor MISFET à canal n doit être formé, en utilisant ladite électrode de grille (8) et les parois latérales (16a) en tant que masques, lesdites secondes sous-régions (18) étant plus profondes que lesdites premières sous-régions (15) et possédant une concentration en impuretés plus élevée que celle desdites premières sous-régions (15), et lesdites secondes sous-régions (18) ainsi que lesdites premières sous-régions (15) formant des régions de source et de drain (19,20) dudit transistor MISFET à canal n; et
   (e) la formation de troisièmes sous-régions (22) moyennant l'introduction d'impuretés de type p dans une région dans laquelle un transistor MISFET à canal p doit être formé, en utilisant ladite électrode de grille (8) et lesdites parois latérales (16a) en tant que masques, lesdites troisièmes sous-régions (22) formant les régions de source et de drain (23,24) dudit transistor MISFET à canal p.

2. Procédé selon la revendication 1, selon lequel ladite première zone superficielle (3) est une région de puits de type n et ladite seconde zone superficielle (2) est une région de puits de type p formée dans ledit substrat semiconducteur (1).

3. Procédé selon la revendication 1 ou 2, selon lequel ladite troisième sous-région (22), qui est formée dans ladite première zone superficielle (3), s'étend audessous de ladite électrode de grille (8).

4. Procédé selon l'une quelconque des revendications 1 à 3, selon lequel les impuretés servant à former ladite troisième sous-région (22) sont des ions de bore.

5. Procédé selon l'une quelconque des revendications 1 à 4, selon lequel ladite troisième sous-région (22) est formée par implantation desdites impuretés dans ladite première zone superficielle (3), cette implantation étant suivie par un recuit.

6. Procédé selon l'une quelconque des revendications 1 à 5, selon lequel les impuretés servant à former ladite première sous-région (15) sont des ions de phosphore.

7. Procédé selon l'une quelconque des revendications 1 à 6, selon lequel les impuretés servant à former ladite seconde sous-région (18) sont des ions d'arsenic.

Patentansprüche

1. Verfahren zur Herstellung einer Halbleitereinrichtung mit p- und n-Kanal-MISFETs, von denen ein erster an einem ersten Oberflächenbereich (3) eines ersten Leitfähigkeitstyps in einem Halbleitersubstrat (1) und ein zweiter an einem in dem Halbleitersubstrat (1) vorgesehenen zweiten Oberflächenbereich (2) eines zweiten Leitfähigkeitstyps ausgebildet werden, wobei
   (a) auf einer Gate-Isolierschicht (5) für jeden der MISFETs eine Gate-Elektrode (8) mit zwei Seiten ausgebildet wird,
   (b) erste Unterbereiche (15) erzeugt werden,

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indem in einen Bereich, in dem ein n-Kanal-MISFET ausgebildet werden soll, unter Verwendung der Gate-Elektrode (8) als Maske n-Störstoffe eingebracht werden,
(c) an jeder Seite jeder Gate-Elektrode (8) eine Seitenwand (16a) ausgebildet wird, indem auf die gesamte Oberfläche des Halbleitersubstrats (1) eine Isolierschicht (16) aufgetragen und die gesamte Oberfläche durch reaktives Ionen-Ätzen geätzt wird,
(d) zweite Unterbereiche (18) erzeugt werden, indem in den Bereich, in dem der n-Kanal-MISFET ausgebildet werden soll, unter Verwendung der Gate-Elektrode (8) und der Seitenwände (16a) als Masken n-Störstoffe eingebracht werden, wobei die zweiten Unterbereiche (18) tiefer sind und eine höhere Störstoffkonzentration aufweisen als die ersten Unterbereiche (15) und wobei die zweiten Unterbereiche (18) zusammen mit den ersten Unterbereichen (15) Source- und Drain-Bereiche (19, 20) des n-Kanal-MISFETs bilden, und
(e) dritte Unterbereiche (22) erzeugt werden, indem in einen Bereich in dem ein p-Kanal-MISFET ausgebildet werden soll, unter Verwendung der Gate-Elektrode (8) und der Seitenwände (16a) als Masken p-Störstoffe eingebracht werden, wobei die dritten Unterbereiche (22) die Source- und Drain-Bereiche (23, 24) des p-Kanal-MISFETs bilden.

2. Verfahren nach Anspruch 1, wobei der erste Oberflächenbereich (3) eine n-Wanne und der zweite Oberflächenbereich (2) eine p-Wanne in dem Halbleitersubstrat (1) ist.

3. Verfahren nach Anspruch 1 oder 2, wobei der in dem ersten Oberflächenbereich (3) erzeugte dritte Unterbereich (22) sich unter die Gate-Elektrode (8) erstreckt.

4. Verfahren nach einem der Ansprüche 1 bis 3, wobei die Störstoffe zur Erzeugung des dritten Unterbereichs (22) Bohrionen sind.

5. Verfahren nach einem der Ansprüche 1 bis 4, wobei der dritte Unterbereich (22) durch Implantieren der Störstoffe in den ersten Oberflächenbereich (3) und anschließende Wärmebehandlung erzeugt wird.

6. Verfahren nach einem der Ansprüche 1 bis 5, wobei die Störstoffe zur Erzeugung des ersten Unterbereichs (15) Phosphorionen sind.

7. Verfahren nach einem der Ansprüche 1 bis 6, wobei die Störstoffe zur Erzeugung des zweiten Unterbereichs (18) Arsenionen sind.

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