(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 May 2004 (27.05.2004)

PCT

(10) International Publication Number
WO 2004/044973 A1

Computer Entered

(51) International Patent Classification[7]: H01L 21/336, 29/423

(21) International Application Number: PCT/US2003/032655

(22) International Filing Date: 14 October 2003 (14.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/290,276 8 November 2002 (08.11.2002) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: AHMED, Shibly, S.; 350 Elan Village Lane #105, San Jose, CA 95134 (US). TABERY, Cyrus, E.; 1220 N. Fairoaks #4102, Sunnyvale, CA 94089 (US). WANG, Haihong; 34170 Donahue Terrace, Fremont, CA 94555 (US). YU, Bin; 1373 Poppy Way, Cupertino, CA 95014 (US).

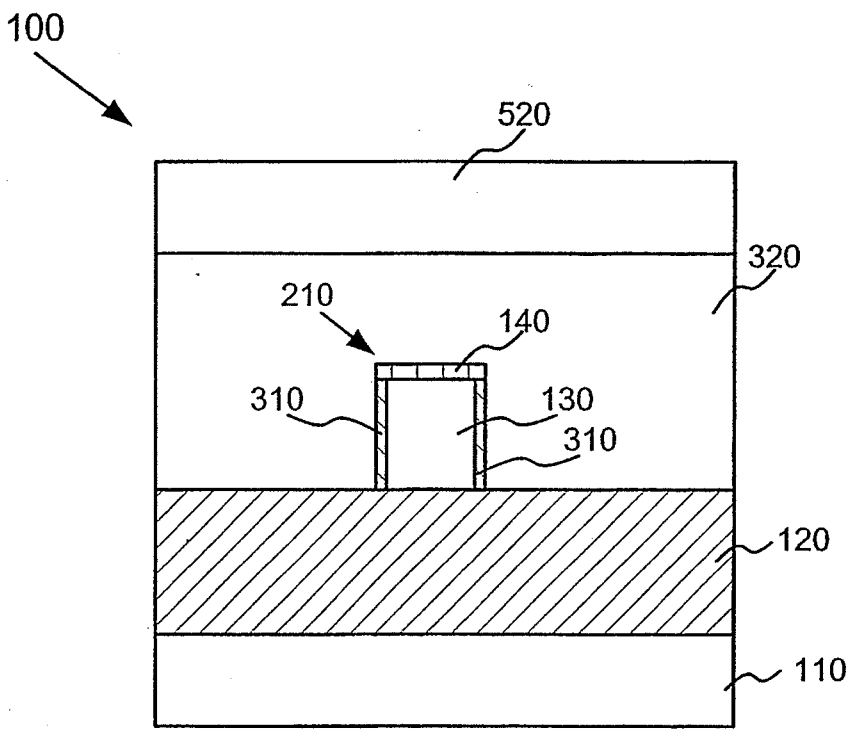
(74) Agent: COLLOPY, Daniel, R.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: PLANARIZING GATE MATERIAL TO IMPROVE GATE CRITICAL DIMENSION IN SEMICONDUCTOR DEVICES



(57) Abstract: A method of manufacturing a semiconductor device (100) may include forming a fin structure (210) on an insulator (120). The fin structure (210) may include side surfaces and a top surface. The method may also include depositing a gate material (320) over the fin structure (210) and planarizing the deposited gate material (320). An antireflective coating (520) may be deposited on the planarized gate material (320), and a gate structure (510) may be formed out of the planarized gate material (320) using the antireflective coating (520).

WO 2004/044973 A1

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.